TriP-T production version Testing Report

Paul Rubinov and Leo Bellantoni

As the first test, we carried out a test of the linearity of the A-pulse, to test the fix that is the major difference between the prototype and production versions of the TriP-t. The relevant plots from the original "TriP-t Report" (using the prototype version of the chip) are reproduced here for the convenience of the reader.

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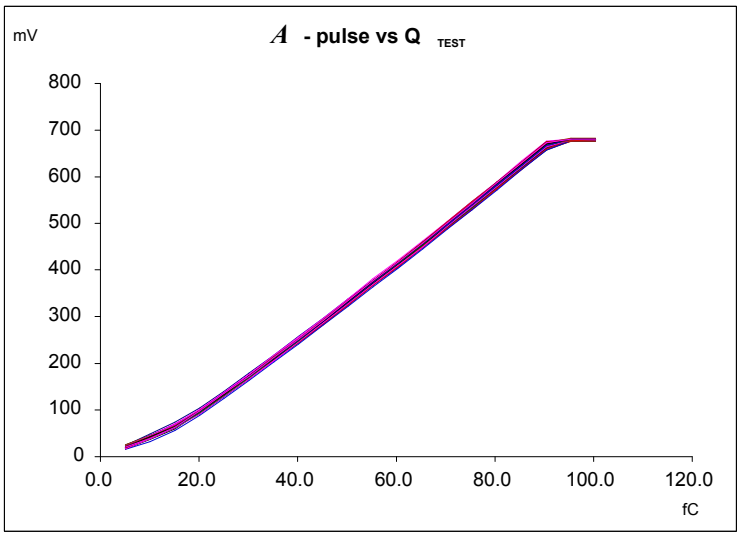

Figure 7 from original "TriP-t Report"

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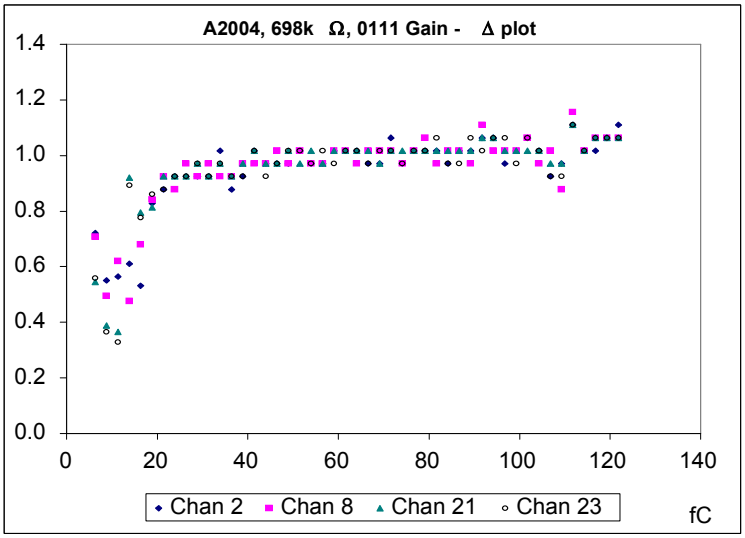

Figure 8 from original "TriP-t Report"

Now compare these with very similar plots from the production version of the TriP-t. Where there are more than one point for the same Qin, the points were measured using different attenuators. This gives an estimate of the systematic error.

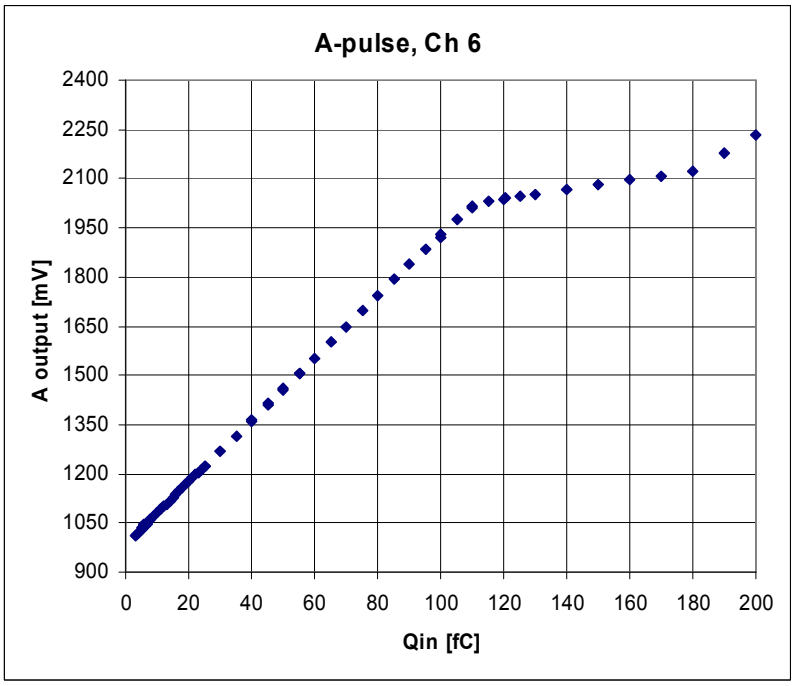

Fig 3. Analog output vs Qin, max gain

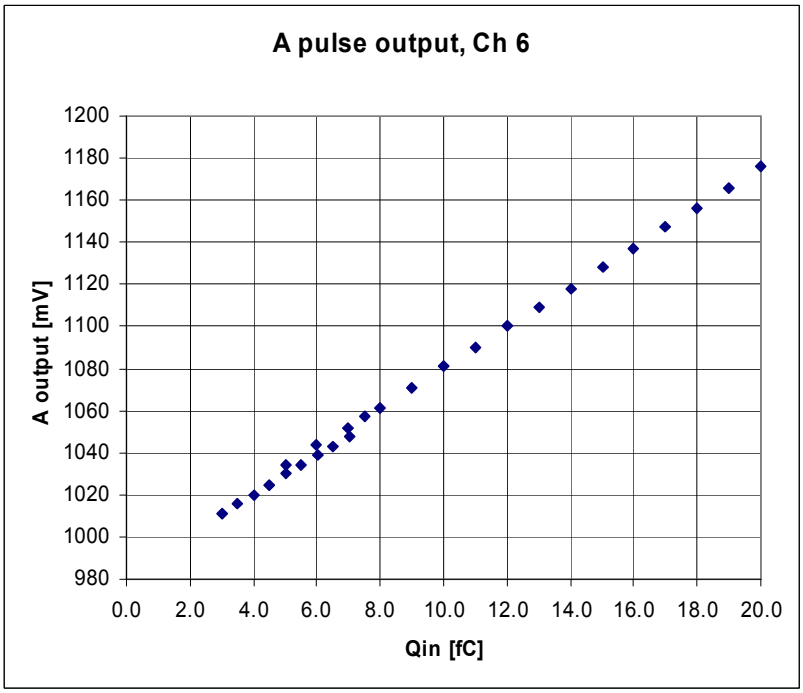

Fig 4. Same data as Fig 3, but showing only the low charge region.

The next plot, Figure 5, is identical to the Figure 8 in Leo's report. It uses the same channels and similar chip settings. The only difference is that in this case the gain is not normalized. It is shown in units of mV out per fC in.

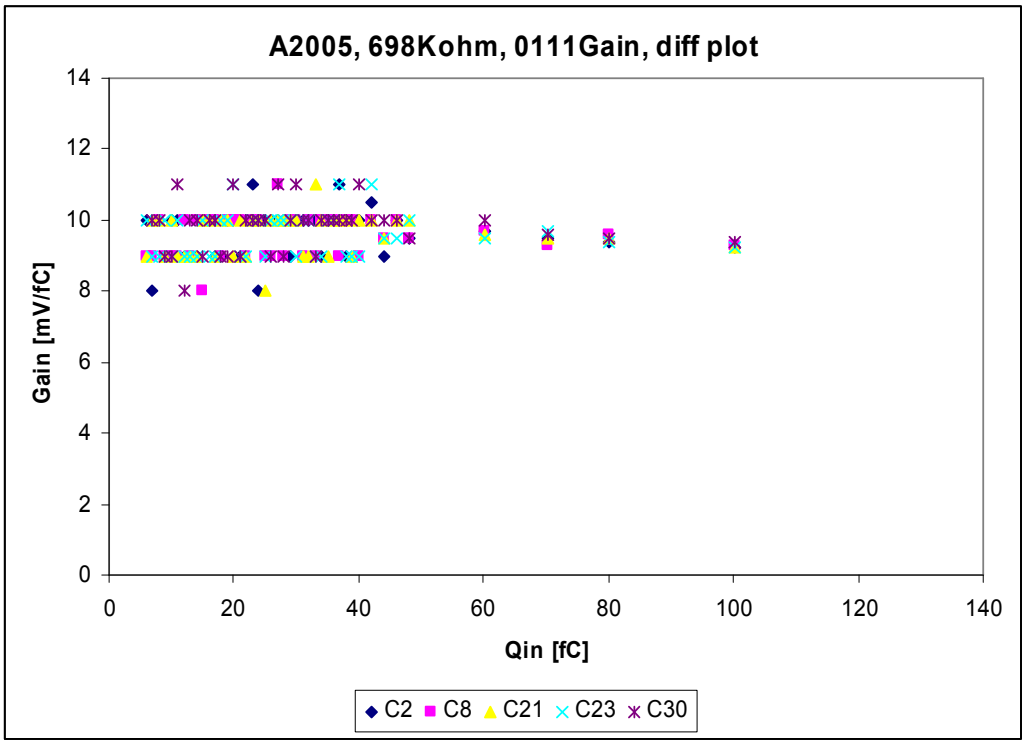

Fig 5. Same as original report Figure 8.

To study the turn on efficiency of the discriminators on the TriP-t, we set the threshold as low as possible with no channels firing on noise- in any crossing. This corresponds to a reasonable threshold, because it must be many sigma above noise to satisfy the condition that a hit is never seen. (Probably at least 5, since we check several thousand turns, looking at all crossing within a turn). Then we inject 4 channels with varying amounts of charge, measuring the fraction of the time the injected channels fired within the crossing with the injected charge. The is plotted in Fig 6 below. The register setting used for this test are given in Table 1. If a register is not shown, it was left at default.

Register	Name	Default value	Comment
1	IBP	130	Preamp drive current
2	IBBNFoll		Preamp feedback control
3	IFF	0	Preamp feedback control
4	IBPIFF1REF		Preamp reset strength
5	IBOPAMP	255	Opamp drive current
6	IB_T		Time circuit current source
7	IFFP2	0	Opamp feedback control
8	IBCOMP	10	Comparator drive current
9	V_REF	180	Ref voltage for opamps 2 & 3
10	V_TH	253	Ref voltage for comparator
11[5:0]	PIPEDELAY	6	Pipeline depth
11[9:6]	GAIN	0111	Gain; high bit is negative logic
12	IRWSEL		Drive currents for pipeline R/W
			NA
14	INJECT	Varies	Which channels to test-pulse

Table1. Register settings used for the discriminator turn on tests.

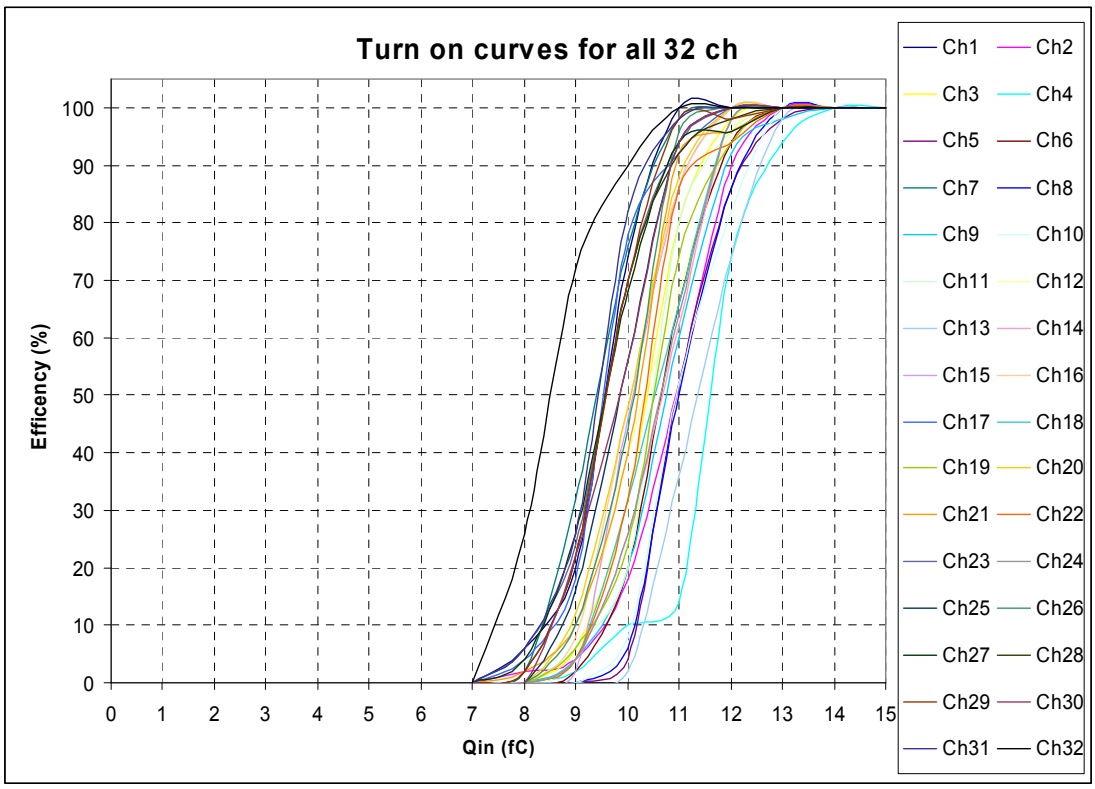

Fig 6. Turn on curve for the 32 discriminators on one TriP-t chip (production version)

For the convenience of the reader, we also reproduce the equivalent plot for the prototype version of the TriP-t here. The was Figure 4 in the original report.

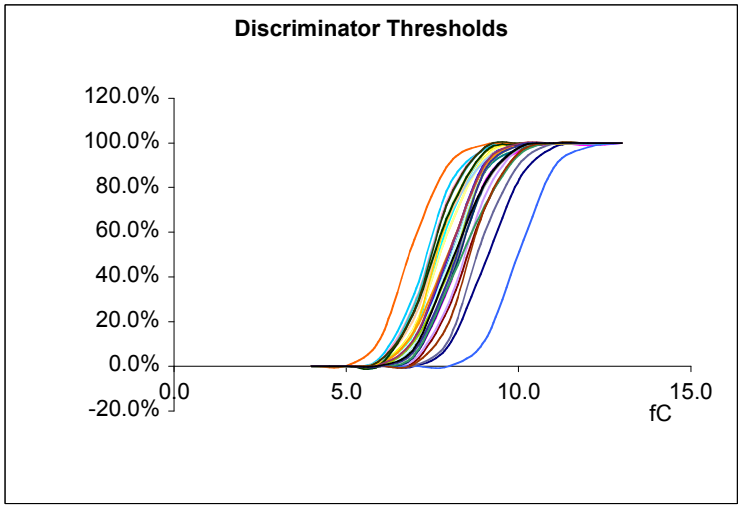

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Figure 4 from the TriP-t prototype testing report.

We also measure the time required to integrate a certain fraction of the injected charge. This is done with a slightly different technique then was use by Leo in the previous version, but I believe this is a more straightforward way to address the relevant question, which is- "how wide must an integration gate be in order to collect all the charge?". The answer to this question is dictated by the risetime of the preamp (and possibly the second stage op-amp) on the TriP-t. To measure this risetime, we rearrange the clocking waveforms fro the normal situation to a case where the injection occurs some time after the integration window has opened, but the closing of the window (which corresponds to the rising edge of the PIPELINE CLOCK signal) is moved around. The amplitude of the integrated pulse is then plotted as a function of the time between the charge injection and the closing of the integration window. This plot is shown in Fig 8 below. As can be seen from the results, in order to achieve 7 bit accuracy, the signal must come in at least 55ns before the closing of the window. This implies that in order to allow a fully efficient window of about 75ns for VLPC signals, the integration window should be at least 130ns wide.

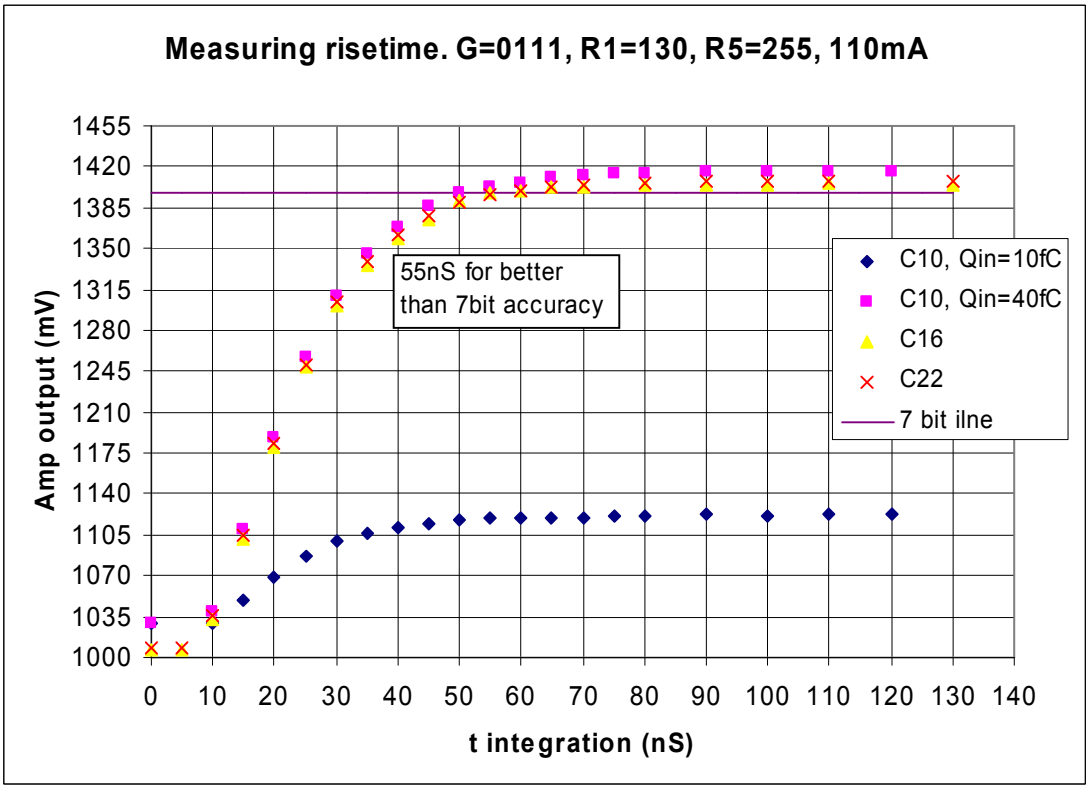

Fig 8. The measurement of the TriP-t integrator rise time.

Next we proceed to measure the T-pulse. This is the TAC output. We measure the output of the TAC at a Qin of 40fC and we set the TAC gain register, R6=50, to give a FS range of about 150ns. This is for consistency, since we determined that in order to integrate the full charge, the latest a charge pulse should arrive is 55ns before the closing of the gate. If we use a value of R6=80, as in the previous report, we can see that the linear range extends only up to about 100ns before the closing of the integration window. With R6=50, we are be able to achieve a linear range of more than 150ns, which would allow a integration window for VLPC signals of about 90ns- from 150ns to 60ns before the rising edge of the pipeline clock (which defines the closing o the window).

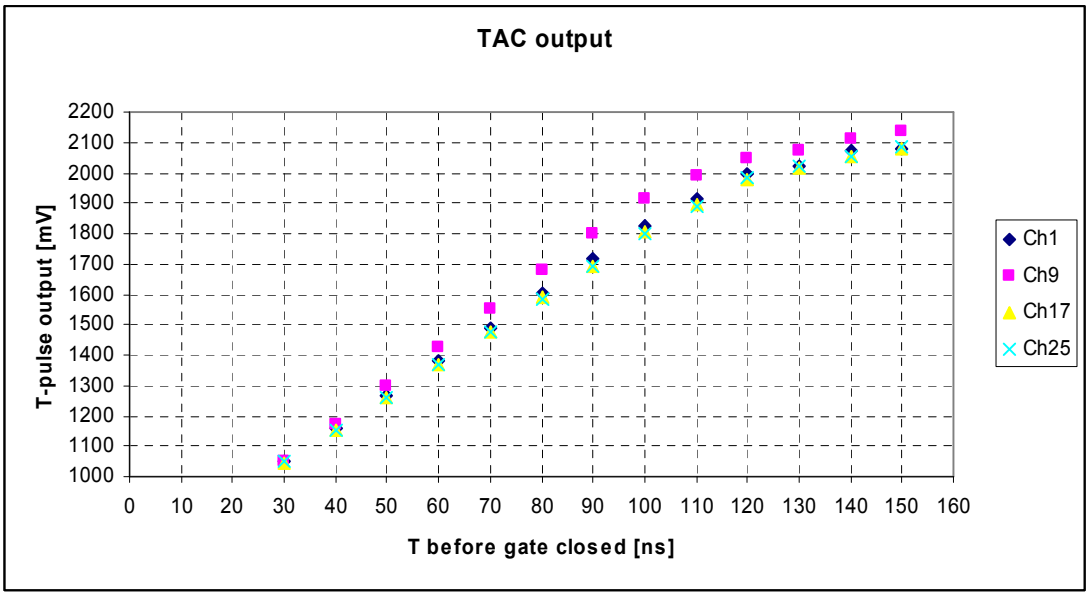

Fig 9. TAC output with R6=80. This gives a too short window.

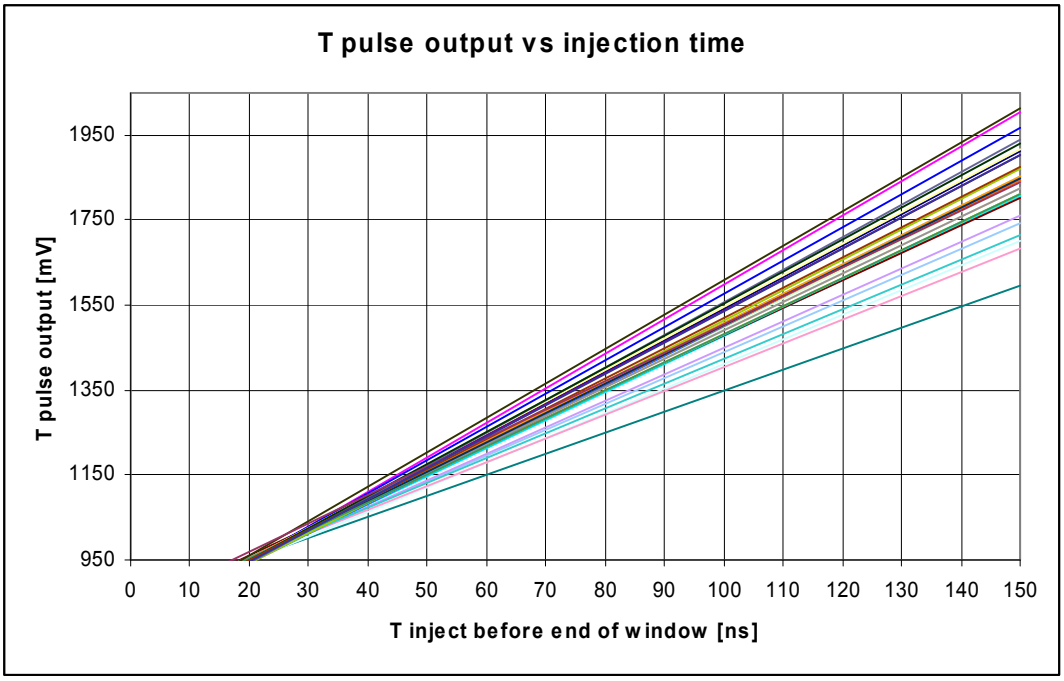

Fig 10. TAC output with R6=50. This gives a window of the desired size.

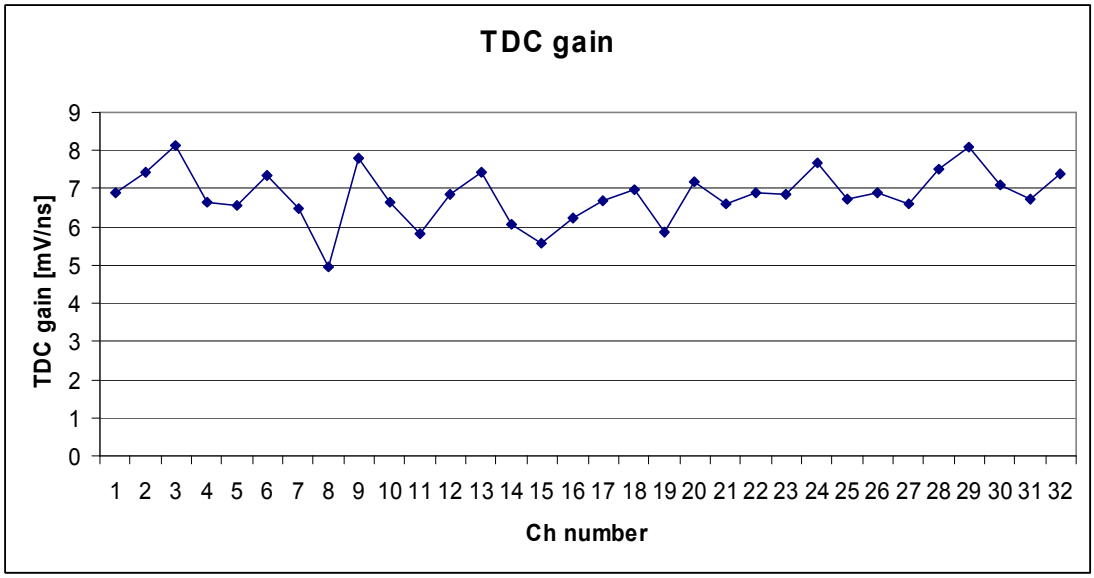

Fig 11. TAC gain for all 32ch. The lowest gain is Ch8. The highest gain is Ch3.

The TAC is also sensitive to the amount of charge in the pulse because the simple discriminators used on the TriP-t are not corrected for time walk effects. We measure the time walk by injected pulses of varying amplitude at the same point in time and measuring the response of the TAC. The results of this study are shown in Fig 12 and Fig 13. Fig 12 is the raw output of the TAC for 4 channels. There is clearly time walk when charges not much larger than the nominal threshold charge of 10fC are injected. Fig 12 shows the same data, but in converting the TAC amplitude to time using the calibration derived from previous measurements. This is also a double check of the calibration- the result should be 140ns. The results are clearly acceptable as for charges only 1pe above the nominal threshold, the time walk is less than 10ns, and for charges at least 2pe above threshold the error is about 3ns.

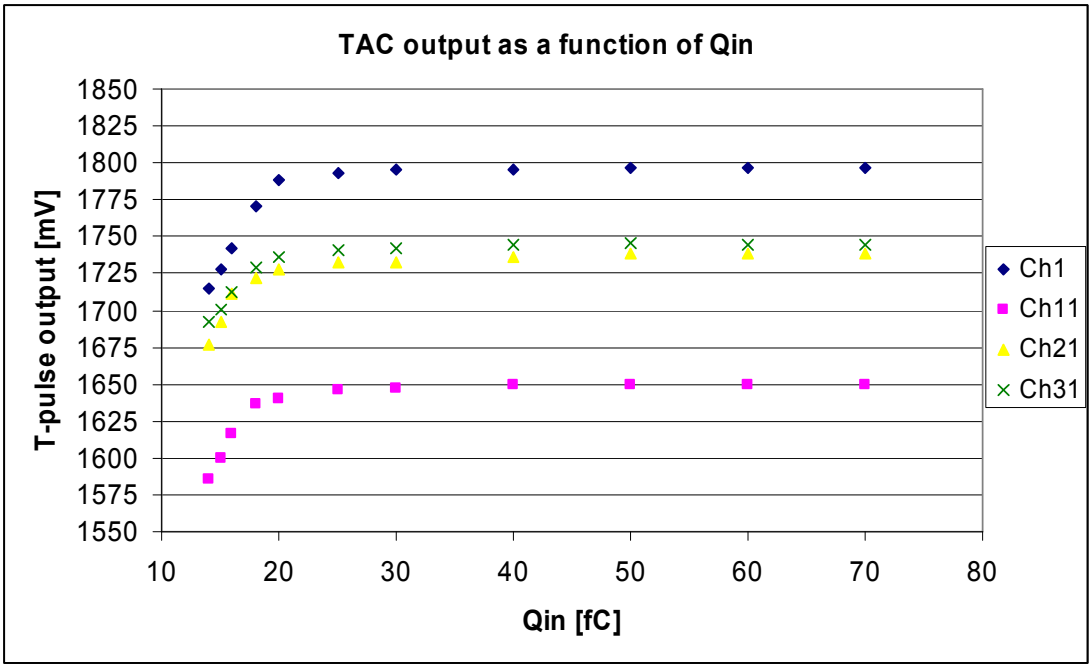

Fig 11. TAC output, as a function of injected charge.

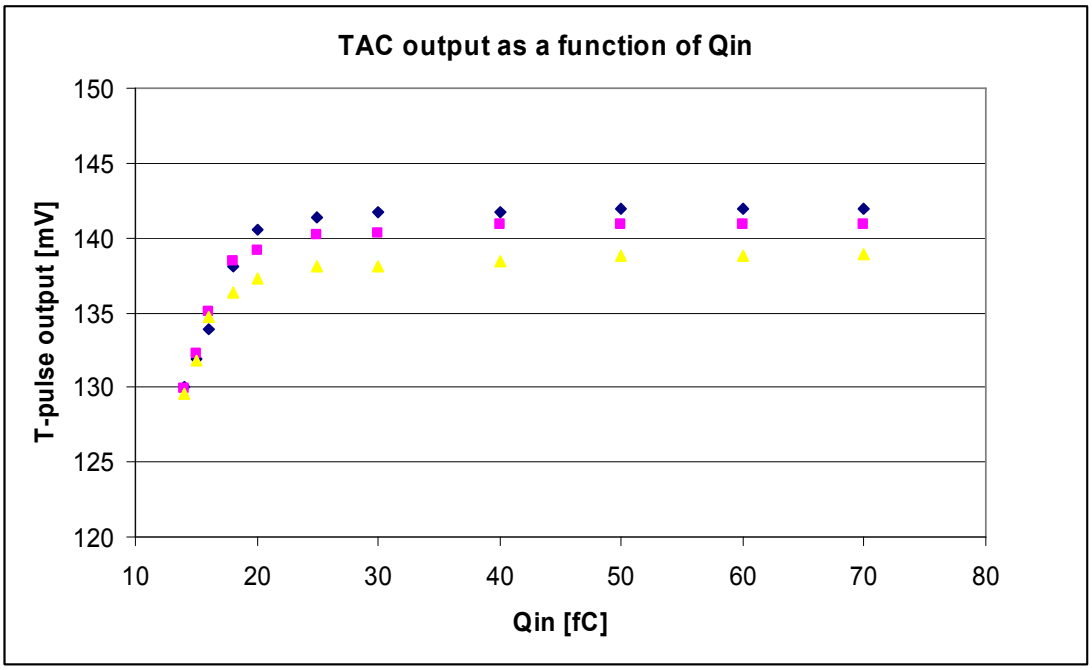

Fig 12. TAC output converted to time, as a function of injected charge.