



**AFEII-t
Platform Test
Handoff**

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FTG

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Schedule for platform test

- “Platform” test schedule
 - ◆ Boards to JW before Nov15
 - ◆ Need answer from Dzero by ~mid Feb
 - work backwards:
 - ▲ All 200 boards ready to install by end of May
 - ▲ Test about 20 boards/week
 - ▲ So 1st boards mid March
 - ▲ About a 1 month lag between “go” and first boards
 - ▲ So “go” mid Feb.
 - ▲ Need to have checked preproduction boards. 1Month?
 - ▲ So preproduction by mid Jan
 - ▲ So “go” mid Dec
 - ▲ So give JW some boards NOW



the platform test

- The platform test
 - ◆ Need to start moving stuff from “Excel” to “online”
 - ◆ Basically, the same interface as for AFEI
 - ▲ Command que
 - ▲ Parameter address space
 - ◆ Different commands, different parameters, different functions



the platform test

- How the AFEIIIt differs from AFEI

- ◆ AFEI:

- ▲ Power on command, set clockgen, set VSVX,
- ▲ SVX through sequencer
- ▲ 1 analog threshold per MCM, 4 disc thresholds per MCM

- ◆ AFEII:

- ▲ FPGAs are volatile- power cycle means new download.
- ▲ Power on, set clockgen, set collector
- ▲ Firmware to DFPGAs, AFPGAs
- ▲ 256 bytes personality/DFPGA
- ▲ 64 bytes/AFPGA peds, 64 bytes/AFPGA thresholds
- ▲ 2 discriminator thresholds/slice
- ▲ EVERYTHING is through 1553



the platform test

- We have FLASH memory to store FPGA firmware and parameters
 - ◆ Exists for the firmware
 - ◆ Needs work for parameters
 - ▲ Bob and I have started work on this, but will require more feedback from Dimitri, Jadwiga and Geoff



the platform test

- Next steps for AFEII-t in the CTS (time scale <2 weeks)
 - ◆ Check heartbeat
 - ◆ Check board temperature
 - ◆ Power up FPGAs
 - ◆ Program FPGAs
 - ◆ Load test data into collector
 - ◆ Read test data from Seq