

AFEII-t Status

May 4, 2006 PMG

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Outline

- **Past**
 - ◆ TriP-t testing
 - ◆ Tests of the pre - production boards on platform
 - ◆ Production Readiness Review
- **Present**
 - ◆ Production status
 - ◆ Schedule
 - ◆ Platform testing
- **Future**
 - ◆ Testing
 - ◆ Installation and Commissioning



Past

Trip-t testing

DONE :

350 boards + 9.2% spares (6115)

**Direct your gratitude to
Leo Bellantoni
for making this slide so short!**



Past

Testing of AFEI-t boards on platform

- ◆ **Some done, more to do**

1. Took data with one AFEI-t prototype AND one pre-production before shutdown. (3 stores in all)

https://plone4.fnal.gov/P1/AFEIUpgrade/offline/gtr_afe_eff_215635_fix.html

2. LED spectra, calibrations, readout testing during shutdown.

<https://plone4.fnal.gov/P1/AFEIUpgrade/meeting.minutes/>

- ◆ **Summary so far:**

Every part of the AFEI-t is known to “work”

Now it all needs to work at the same place at the same time



Past

AFEL-t boards known to work

✓ **Mechanical:**

Interface to cassette, backing bars, alignment pins, springs, handles, [air dams]

✓ **Backend:**

Interface to Sequencer readout (a.k.a. grey cable), interface to Central Track Trigger (a.k.a. LVDS), power supplies, 1553

✓ **Bottom:**

Analog performance (big signals and small signals, analog and discriminators), bias, temperature control

✓ **Front:**

Firmware (readout format, personality), software, calibration, reliability, stability



Is it safe?

- To make 350 AFEII-t ?

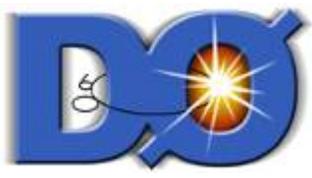




Still past

- **Production Readiness Review**

- ◆ **A collection of EEs and Phys from Dzero**
- ◆ **Most of the presentation focused on the readout problems**
- ◆ **Asked some tough questions**
 - **Readout issues**
 - **Test for CPS dynamic range**
 - **Test for CTT link diagnostics and timing**
 - **Reliability, manufacturability: lead free issues, via issues**



Almost the present

- **Production Readiness Review bottom line**
 - ◆ **Boards approved**
 - ◆ **Boards ordered**
 - ◆ **Johnny Green and Tom Fitzpatrick sent to scout out the facility**
 - ◆ **Extra \$7K spent to accelerate production as much as possible**
 - (which as usual just covered schedule slippage)



Present

- **First 4 bare boards delivered to Millennium (our assembler) on May 2nd**
 - ◆ These will be used to profile the ovens and debug the pick and place programs
 - ◆ Expect to be ready to start rolling the boards 3rd week of May
 - ◆ Expect 100 more boards to ship from Merix to Millennium 3rd week of May

Only the finest “Just In Time” for us!



Present

- **Schedule**

My top 3 priorities:

- 1. Meet the schedule**
- 2. Meet the milestone**
- 3. Meet the milestone on schedule**

“203 AFEL-t boards fully tested, working and ready to install”



Schedule

- **First bare boards – 1st week May**
- **First stuffed boards – 2nd week of June**
- **Millennium to make minimum 40 boards/week:
9 weeks – 2nd week of Aug project complete.**
 - ◆ **Tested good means:**
 - **Flash/FPGAs programmed**
 - **EVERY channel injected with 2 amplitudes and peds and checked for ped, noise, gain**
 - **EVERY discriminator fires/doesn't fire for the correct threshold**
 - **LVDS links checked**
 - **Temperature control circuitry checked and calibrated**
 - **Bias setting and readback checked and calibrated**



Present platform testing

- **3 objectives for shutdown remain**
 - ◆ **Run temperature control on platform using the automatic calibration procedure**
 - ☑ as of May 3rd
 - ◆ **Tune the AFEII to CTT timing**
 - ◆ **Take cosmic ray data with CPS so we have a MIP calibration before beam returns**



Future

- **Testing**

- ◆ **Testing personnel accounted for – tests are fairly fast and automated, so not an issue.**
- ◆ **General outline of the testing plan worked out, software nearly done, procedures being developed.**
- ◆ **1 bench top test stands 100% ready to go – being used to develop testing procedures**
- ◆ **2 bench top test stands ready except for LVDS (waiting for cables)**
- ◆ **Phase V now able to calibrate AFEII-t for temperature and bias at the push of a button!**



Future

- **Testing Plan**

1. **Inspect and do the final board assembly, enter into tracking database. (1hr)**
2. **Program board and run it through automated bench top test procedure. (30 min)**
3. **Run board through Phase V. (30 min)**
4. **Install board into Combined Test Stand for burn in (24 hrs, but there are 16 slots)**

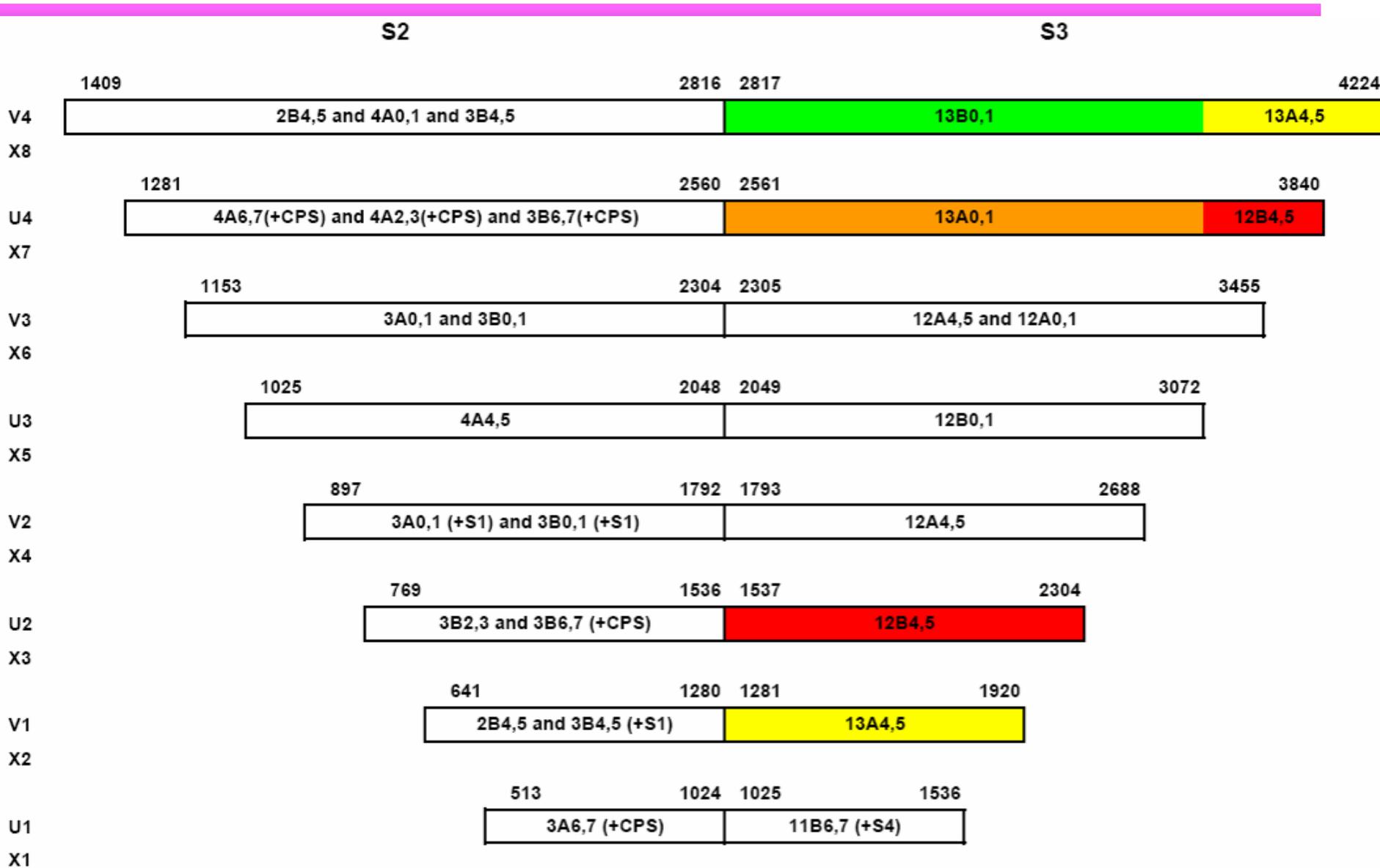


Future

- **Installation and commissioning plans for the boards are currently being refined.**
 - ◆ **General strategy:**
 - Put them where we know they work, study them there (e.g. use the stereo boards to study the performance and calibration of the discriminators)
 - Put them where they will do the most good (CPS because of saturation problems, sectors with longest wave guides = smallest signals)
 - Put them where it will be easy to see the effect (so concentrate in one sector)



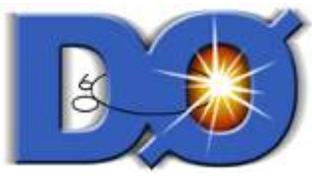
First batch





Crate locations

VRB_5116	VRB_5116 1	SEQ_05A08	SEQ_05A08 1	SVXs: on AFE_11B4	SVXs: on AFE_11B5	AFE_11B4	AFE_11B5
	VRB_5117 1		SEQ_05A09 1	SVXs: on AFE_11B6	SVXs: on AFE_11B7	AFE_11B6	AFE_11B7
VRB_5117	VRB_5117 2	SEQ_05A09	SEQ_05A09 2	SVXs: on AFE_12A0	SVXs: on AFE_12A1	AFE_12A0	AFE_12A1
	VRB_5117 3		SEQ_05A09 3	SVXs: on AFE_12A4	SVXs: on AFE_12A5	AFE_12A4	AFE_12A5
	VRB_5117 4		SEQ_05A09 4	SVXs: on AFE_12B0	SVXs: on AFE_12B1	AFE_12B0	AFE_12B1
	VRB_5118 1	SEQ_05A10	SEQ_05A10 1	Collector AFE_12B4	SVXs: on AFE_12B5	AFE_12B4	AFE_12B5
VRB_5118	VRB_5118 2		SEQ_05A10 2	Collector AFE_13A0	SVXs: on AFE_13A1	AFE_13A0	AFE_13A1
	VRB_5118 3		SEQ_05A10 3	SVXs: on AFE_13A4	SVXs: on AFE_13A5	AFE_13A4	AFE_13A5
	VRB_5118 4		SEQ_05A10 4	Collector AFE_13B0	SVXs: on AFE_13B1	AFE_13B0	AFE_13B1



Conclusion

- **Prototype phase is done**
- **Pre production phase is (almost) done**
- **Production has started**
- **Testing is being setup**
- **Project completion projected for mid August**

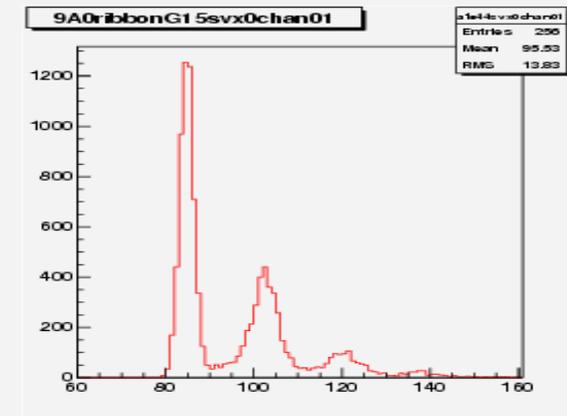
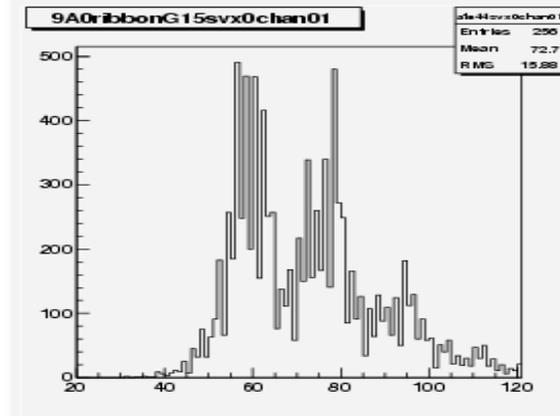
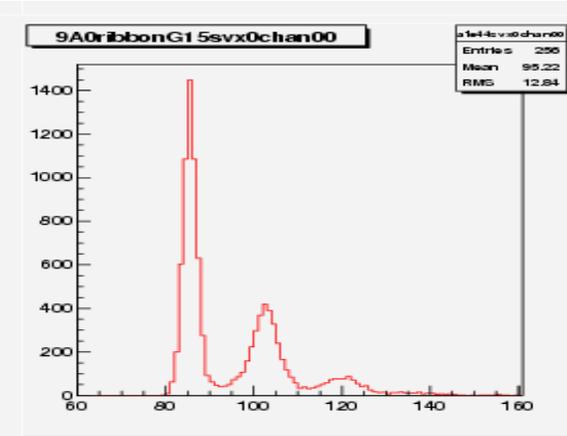
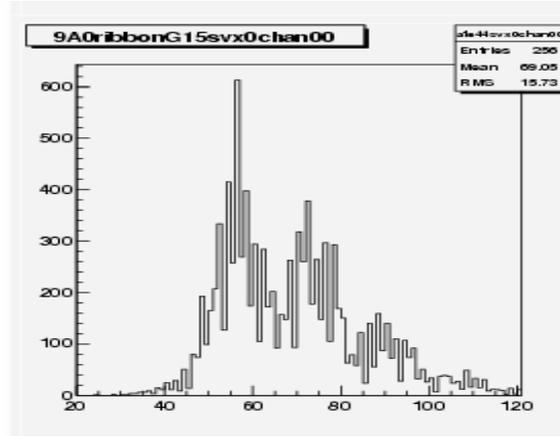


Pretty pictures

Same spot on
detector pulsed by
LED

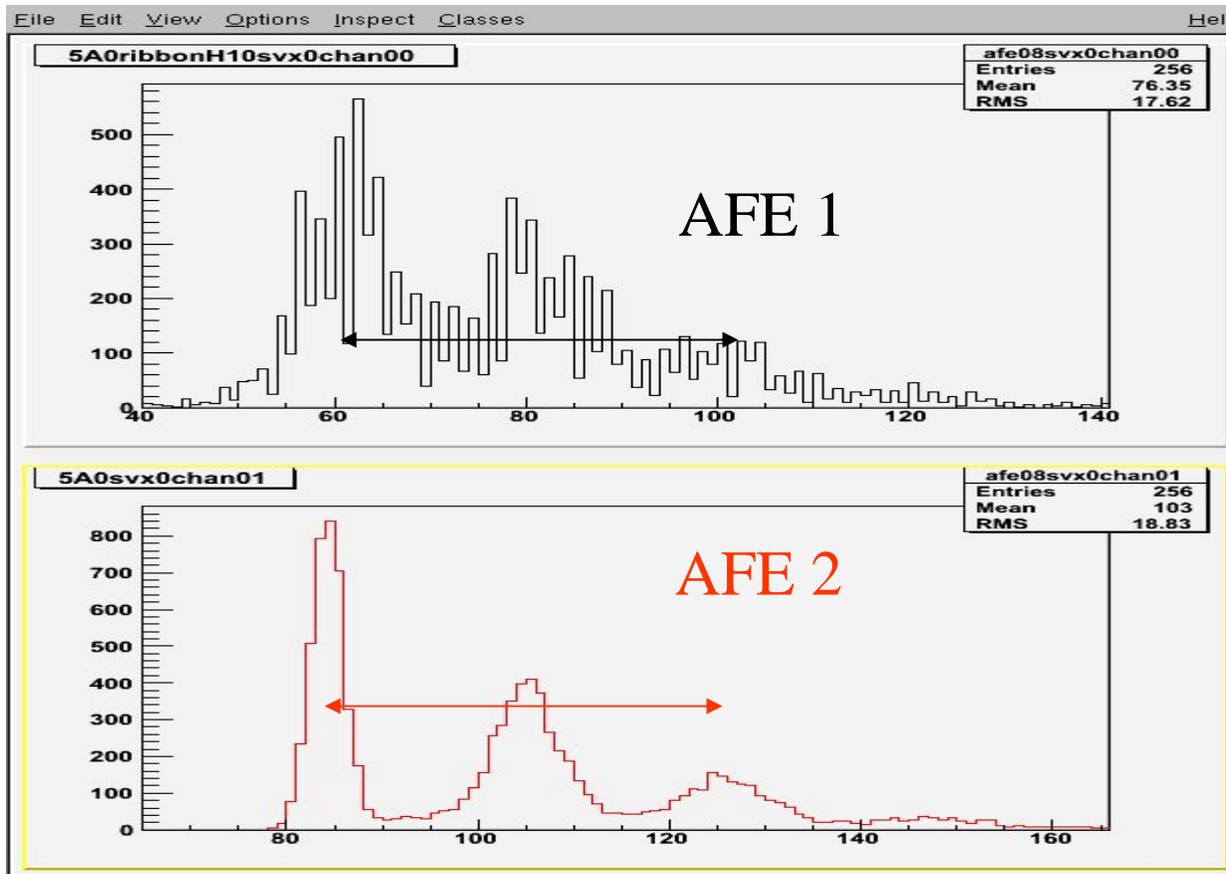
AFE1 – left plot
AFEII – right plot

(2 out of 64 plots
shown)



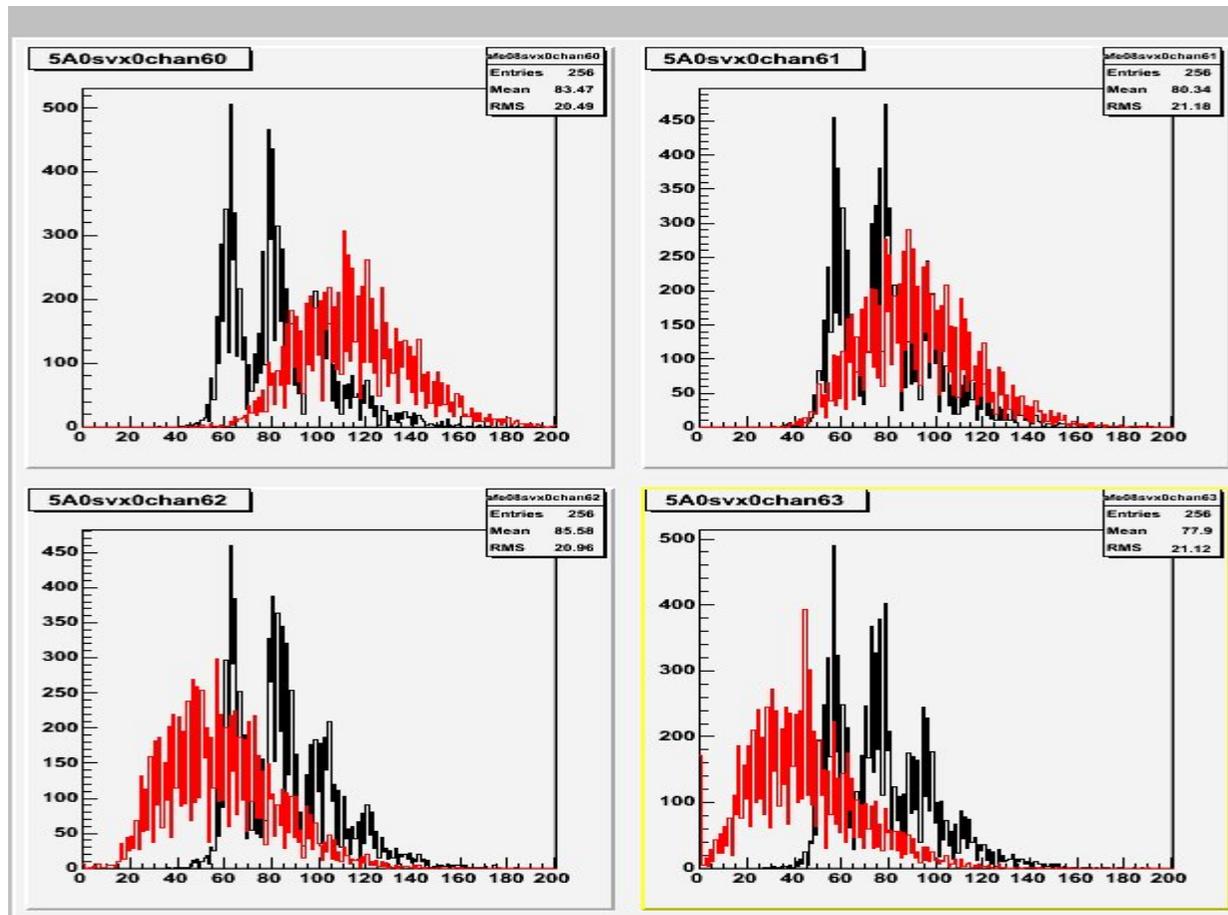
AFE 1 and AFE 2 have the same analog gain

Run 216593 (AFE1), 216622(AFE2)



AFE 1, CFT axial discriminator off, discriminator on

Runs 216879, 216881



4 May 2006

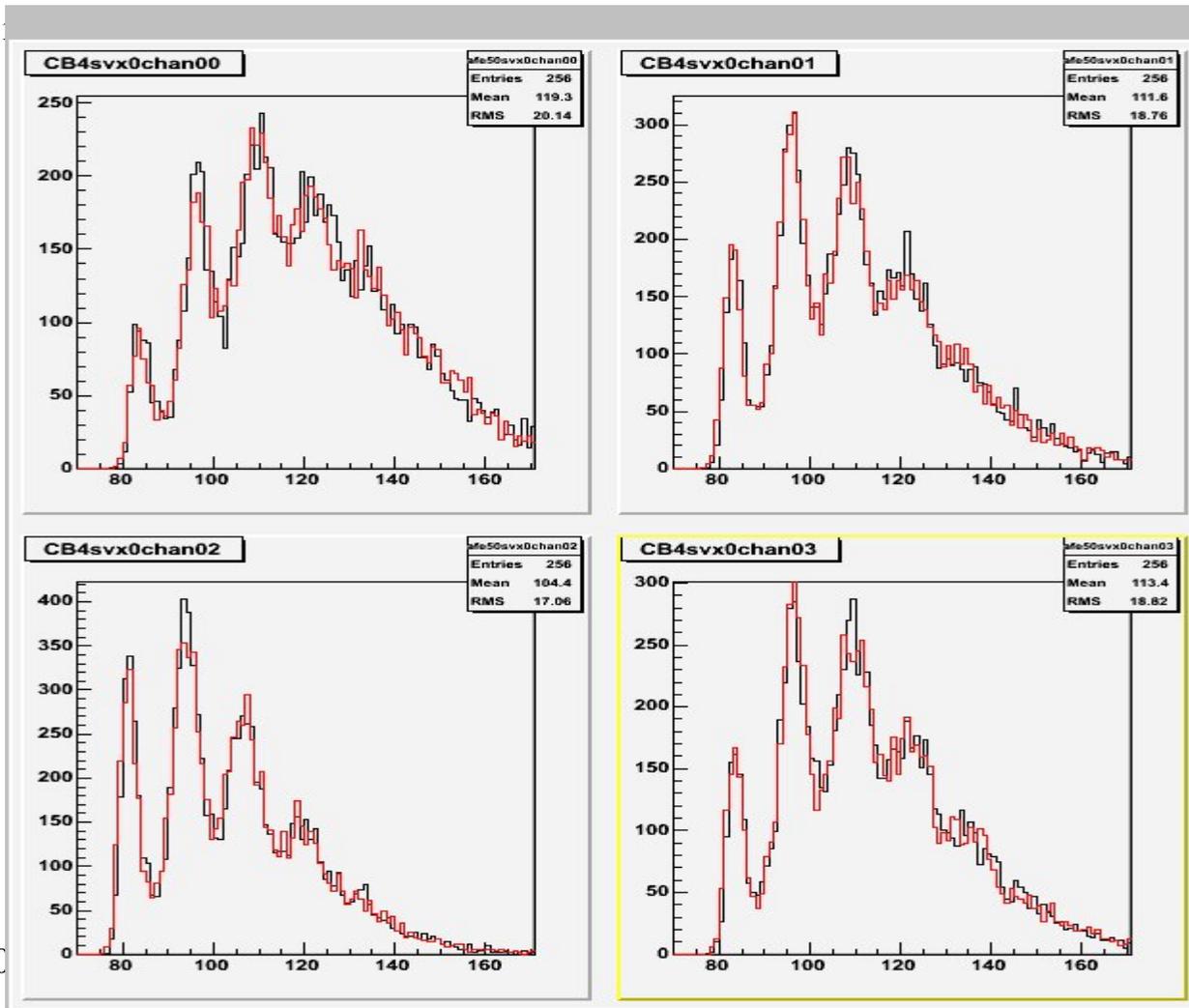
May 06 PMG - Paul R
J. Warchol

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AFE 2, CFT stereo

discriminator off, discriminator on

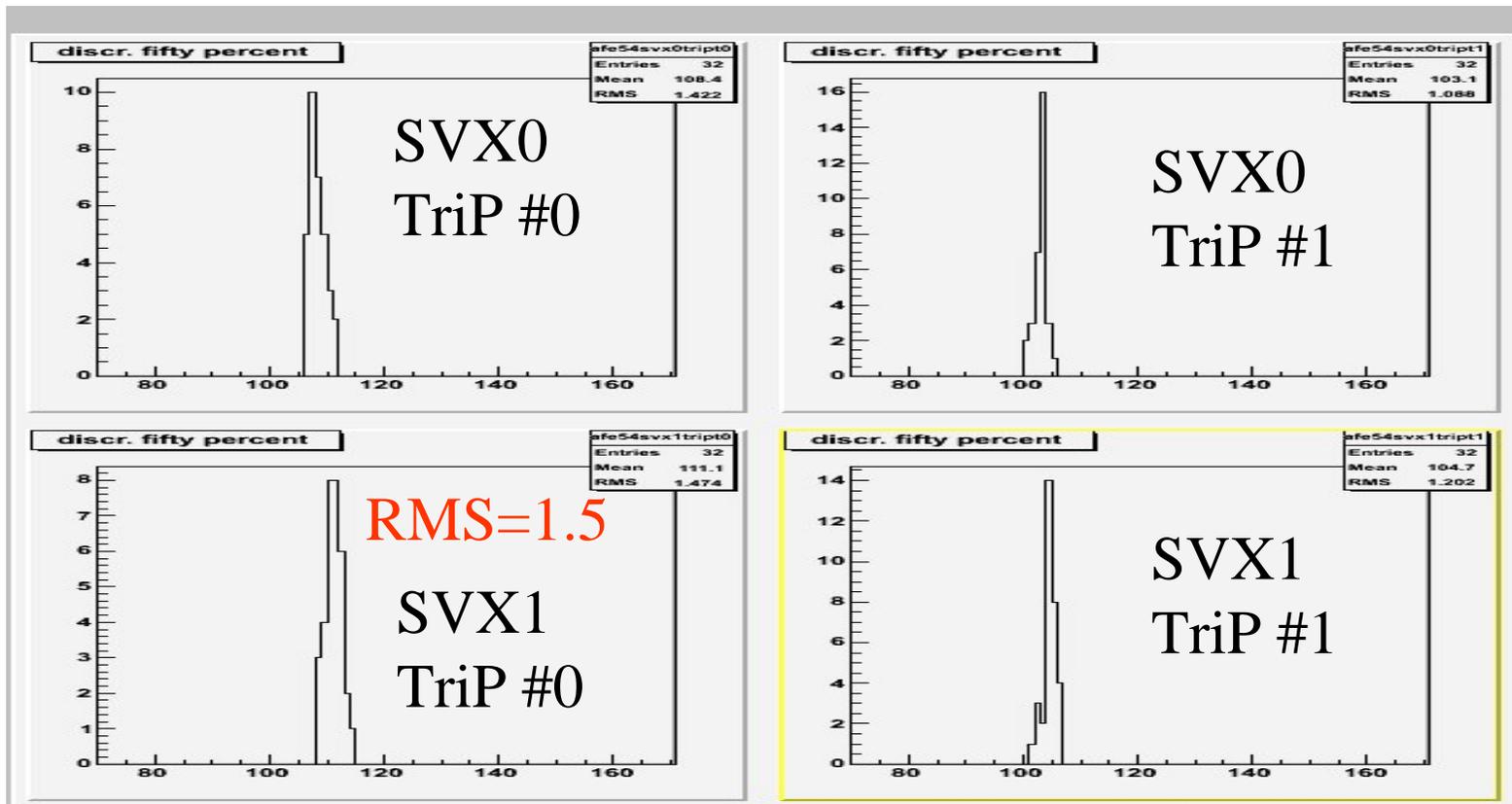
Run 216928,2



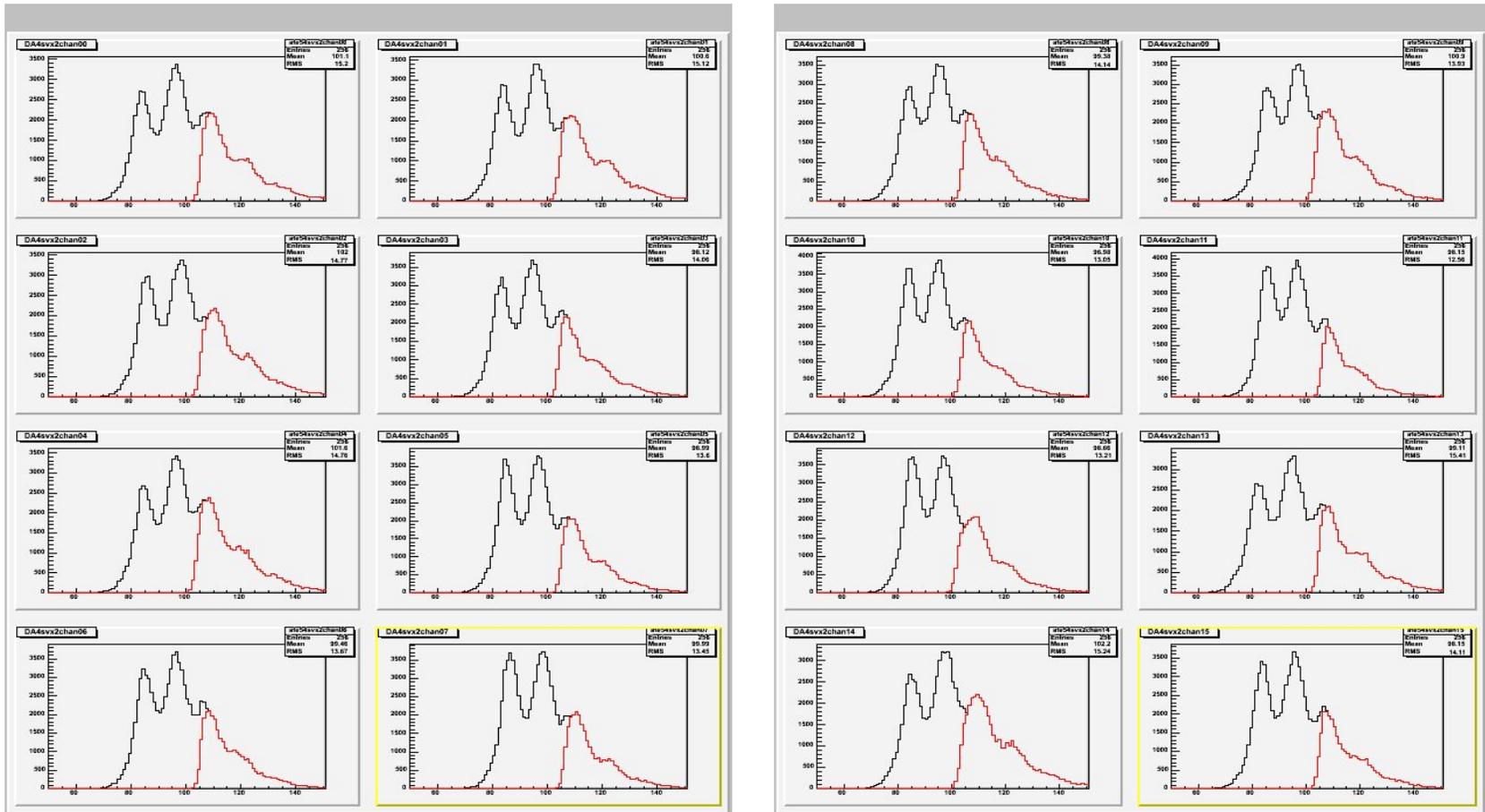
4 May 200

Discriminator Study: 50 % point distribution

New firmware, board 13A4

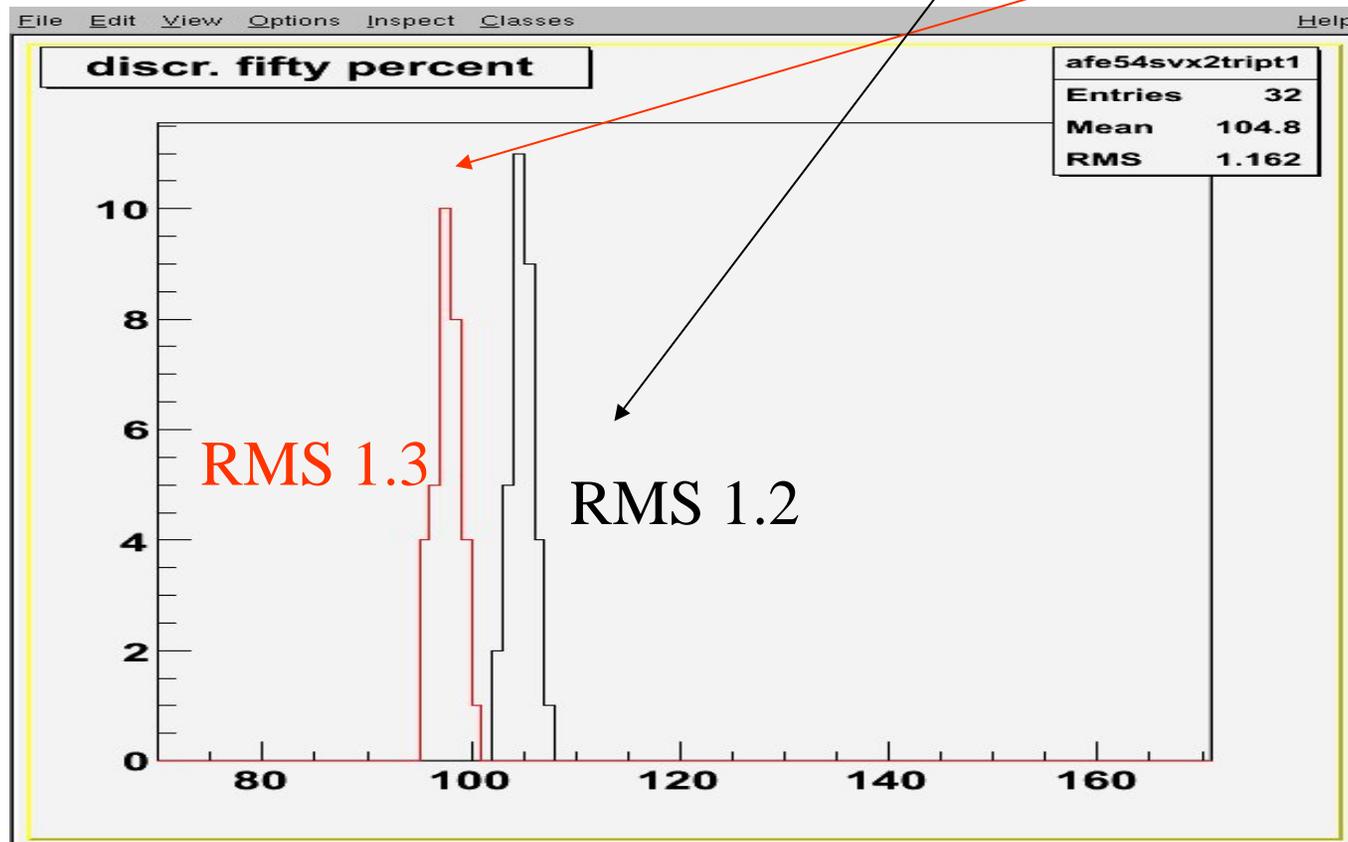


New firmware, board 13A4, SVX2, TriP #1



New firmware, board 13A4, SVX2, TriP #1

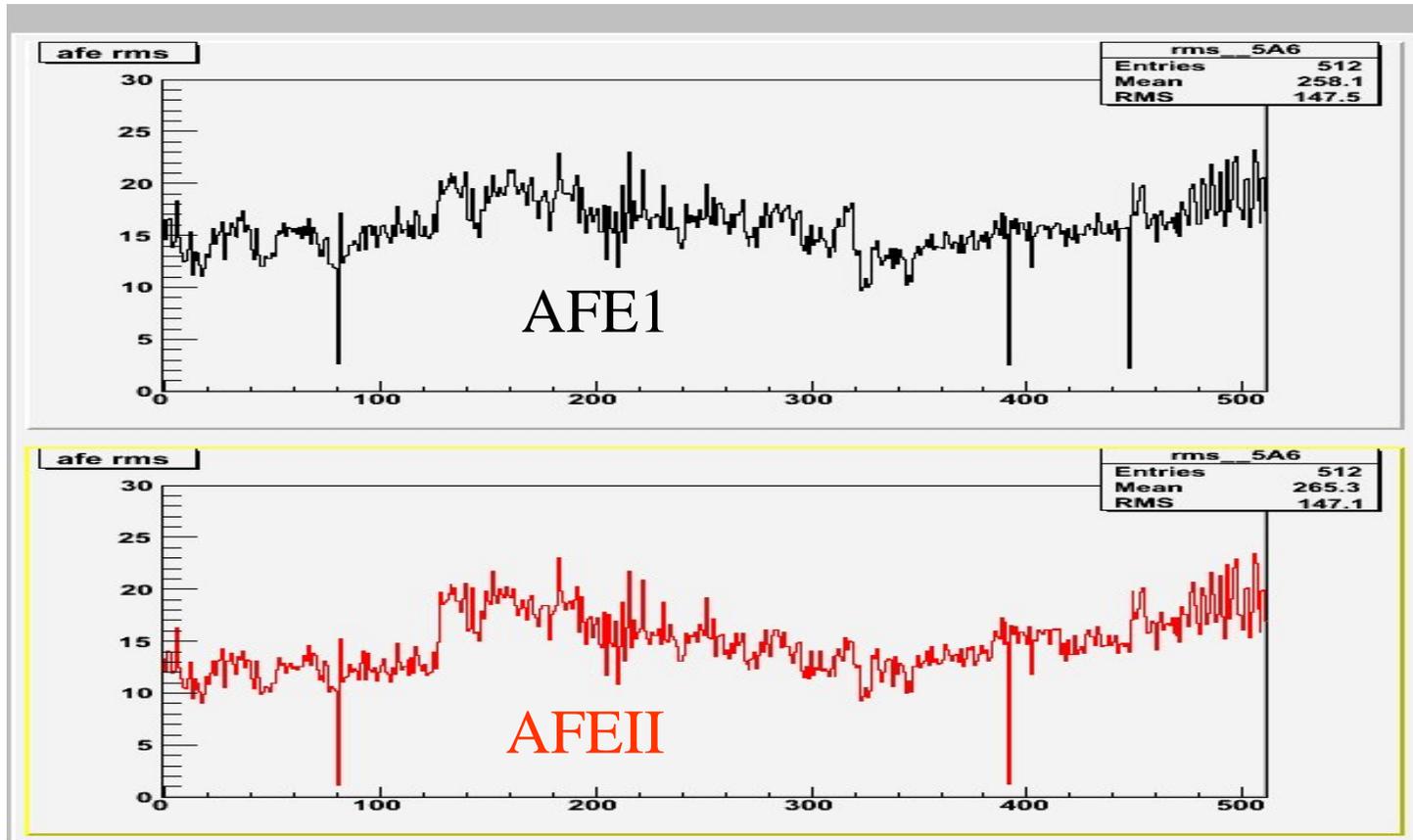
Fifty % point, discr threshold 250 or **255**

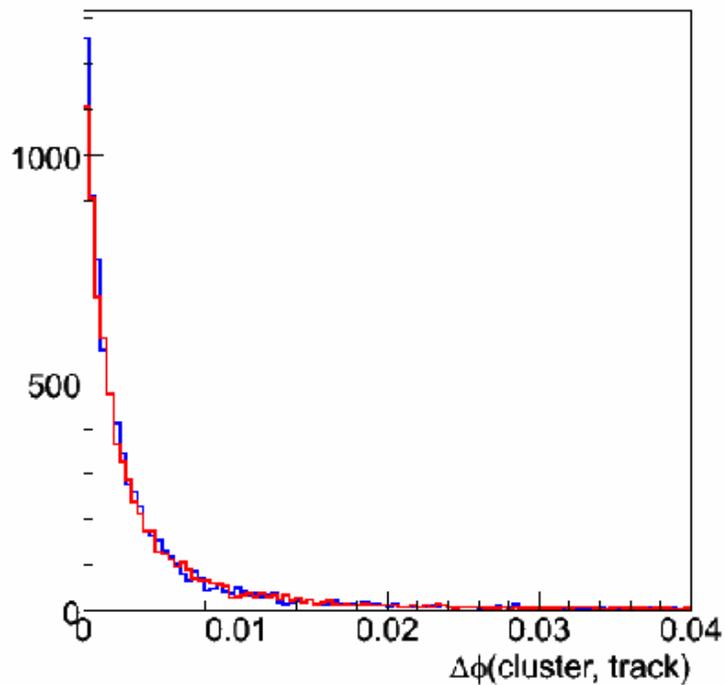


LEDs on, rms of pulse height distribution vs VLPC pixel #

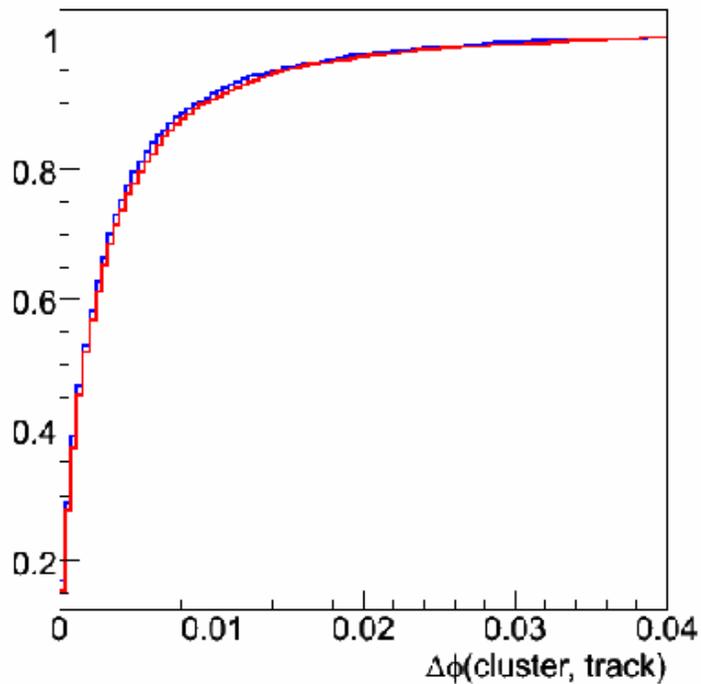
AFEII #20 in 5A6

This proves AFEII readout mapping is correct





The distance (in radians) from the track to the cluster associated with this track in radians. A loose cut on $z < 30\text{cm}$ is applied. The histograms are not normalized and the phi of clusters is recalculated as a function of track's z .



The cumulative distribution of the one above. From the given plot one can read the probability of having the cluster closer to the track than the given distance in radians. One can claim that for the AFEII board it is a little bit more probable to have clusters closer to the track than for the AFEI board.