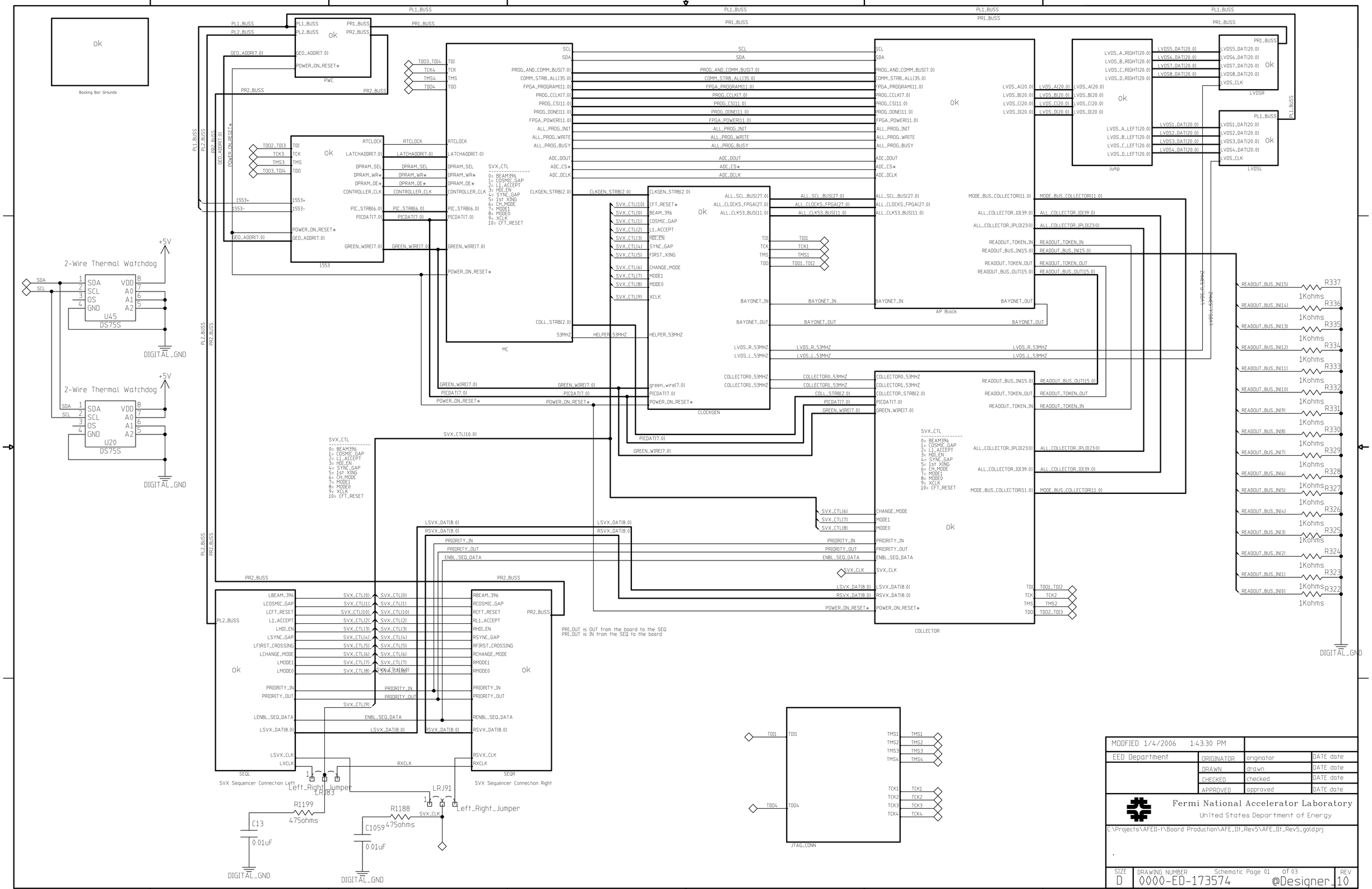

MODIFIED 1/4/2006 1:43:30 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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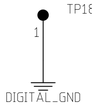
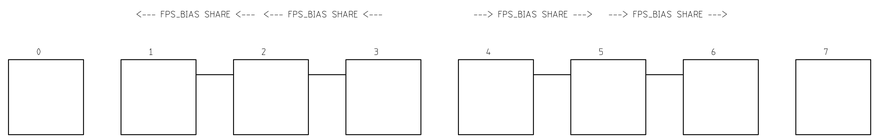
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer	10

H:8ND, V:4LA

Comments go here





Left to right:
CLOCKGEN
COLLECTOR
1553
HELPER

MODFIED 1/4/2006 1:43:30 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_1	0

H=8ND, V=4LA

MODFIED 1/4/2006 1:43:30 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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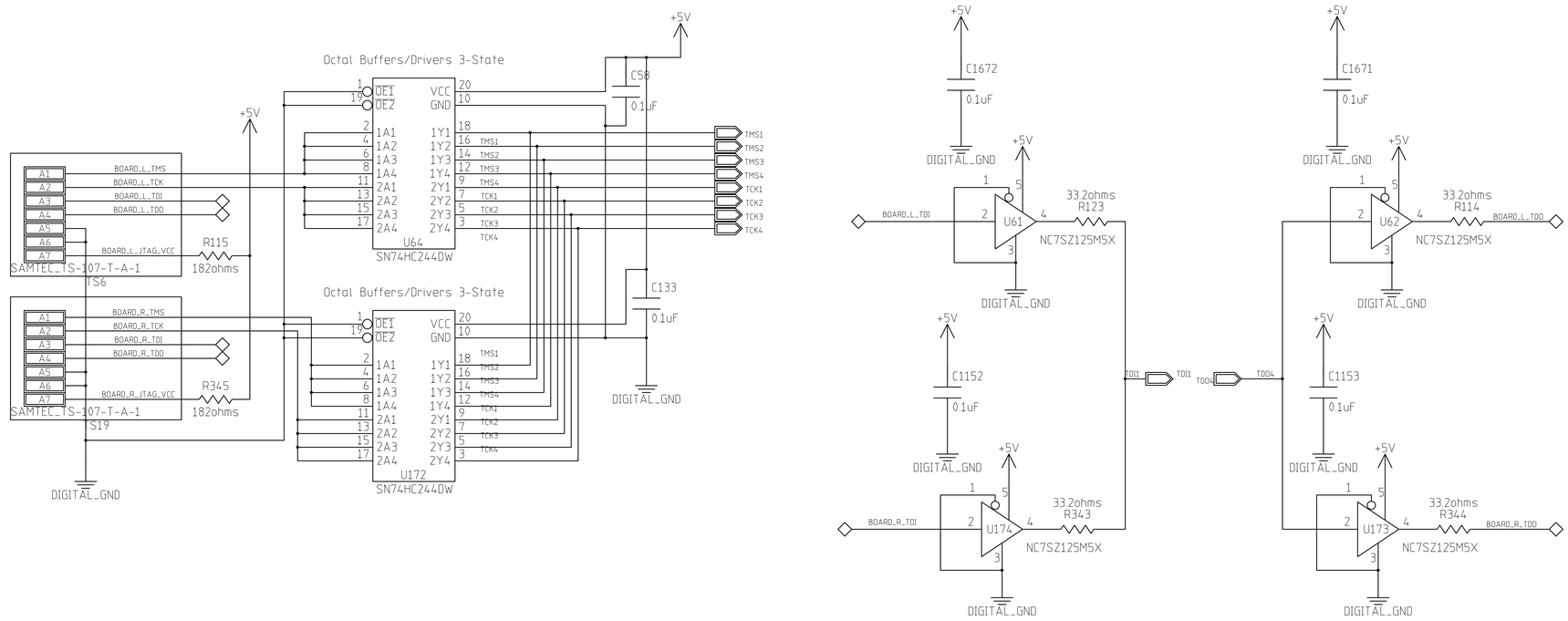
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 03 of 03 @Designer_1	0

H=8ND, V=4LA



MODFIED 12/28/2005 2:50:32 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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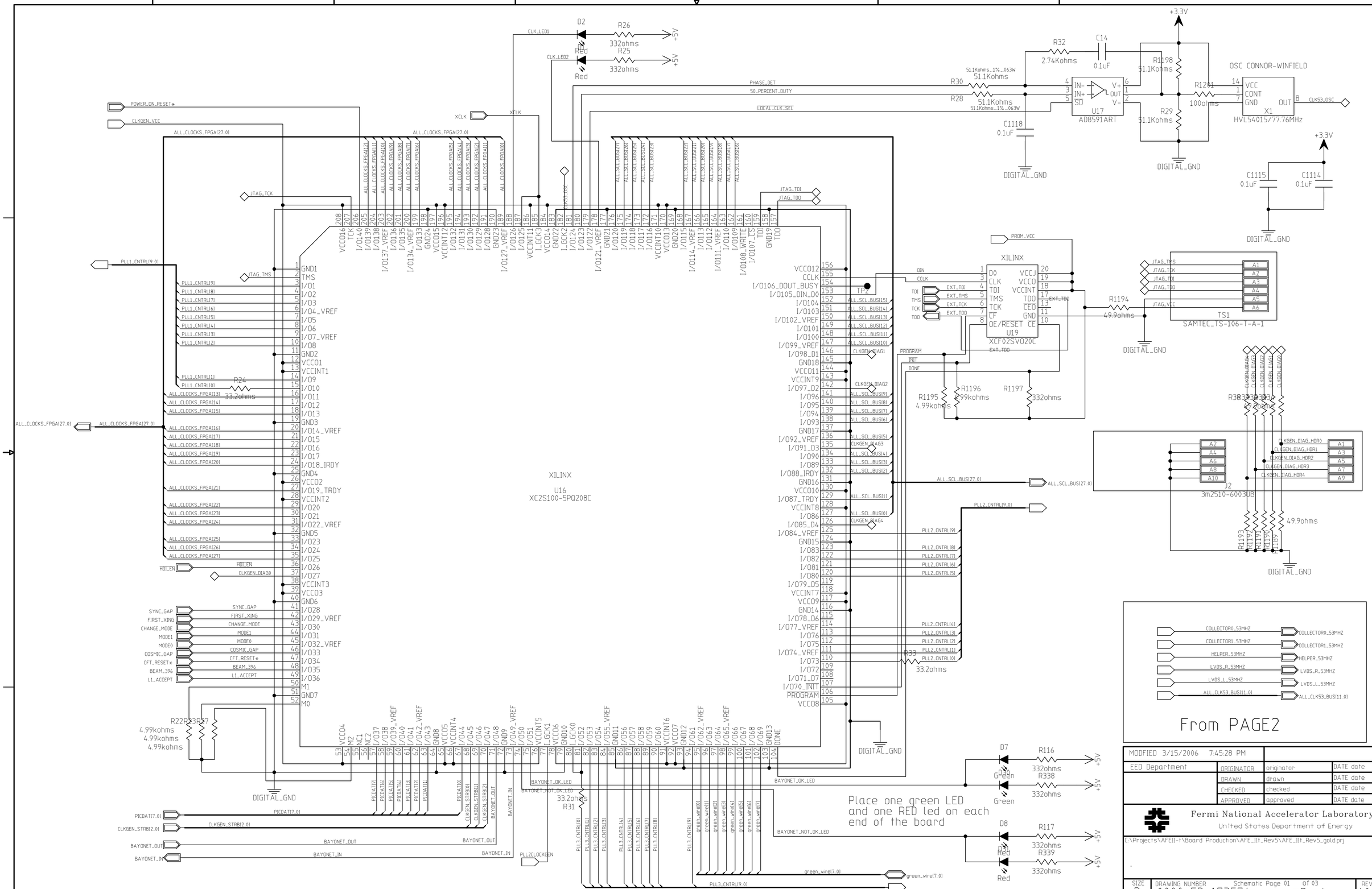
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H:8ND, V:4LA


XILINX
U16
XC2S100-5PQ208C
XILINX
U19
XCF02SVO20C
OSC CONNOR-WINFIELD
X1
HVL54015/77.76MHz
U17
AD8591ART
SAMTEC_TS-106-1-A-1
TS1
3M2510-6003UB
J2
From PAGE2
Place one green LED and one RED led on each end of the board
DIGITAL_GND
+3.3V
+5V
MODIFIED 3/15/2006 7:45.28 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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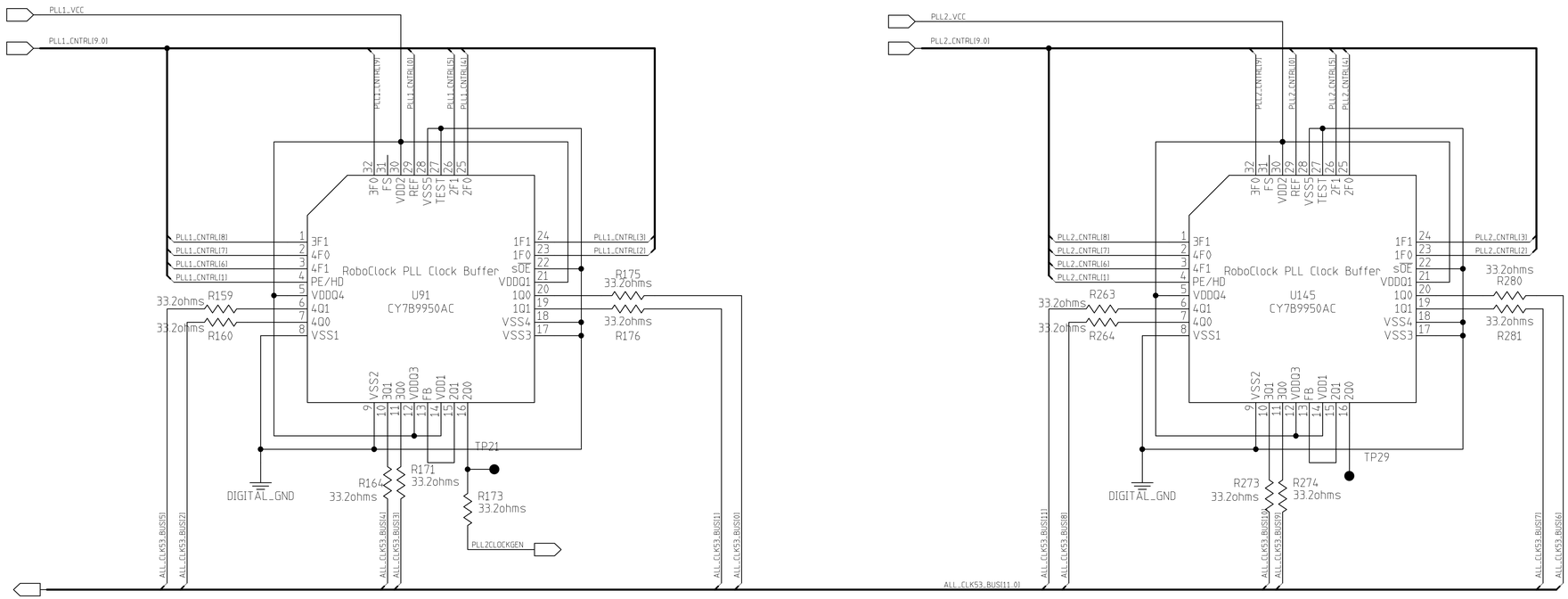
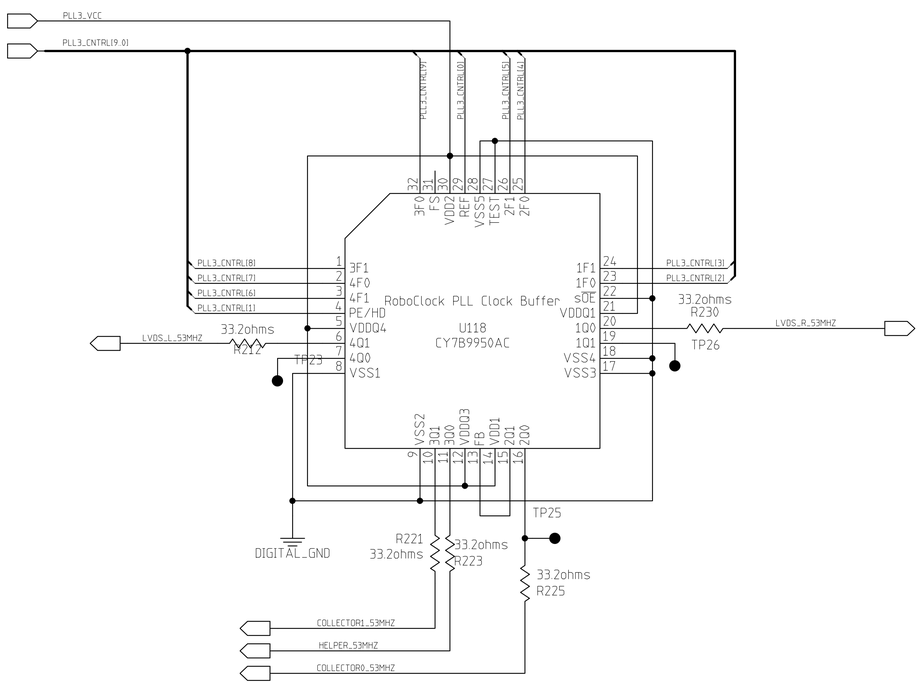
C:\Projects\AFEII-1\Board Production\AFE_II1_Rev5\AFE_II1_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV





ALL_CLK53_BUS[11..0]

0 = AFPGA0 CLK53
1 = AFPGA1 CLK53
2 = DFPGA01 CLK53
3 = AFPGA2 CLK53
4 = AFPGA3 CLK53
5 = DFPGA23 CLK53
6 = AFPGA4 CLK53
7 = AFPGA5 CLK53
8 = DFPGA45 CLK53
9 = AFPGA6 CLK53
10 = AFPGA7 CLK53
11 = DFPGA67 CLK53

MODFIED 3/15/2006 7:45:28 PM			
EED Department	ORIGINATOR	originator	DATE date
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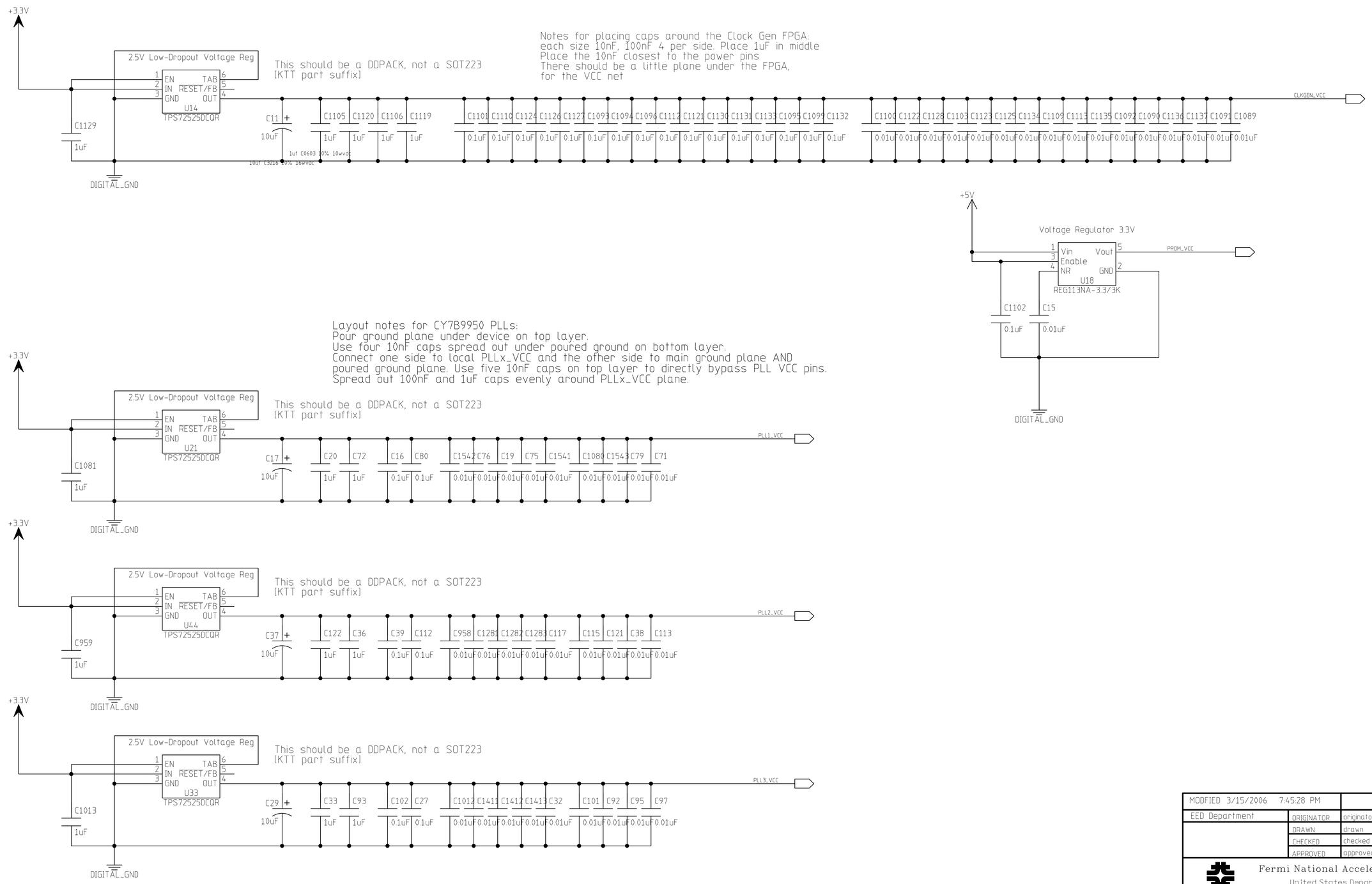
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_	10

H:8ND, V:4LA



MODFIED 3/15/2006 7:45:28 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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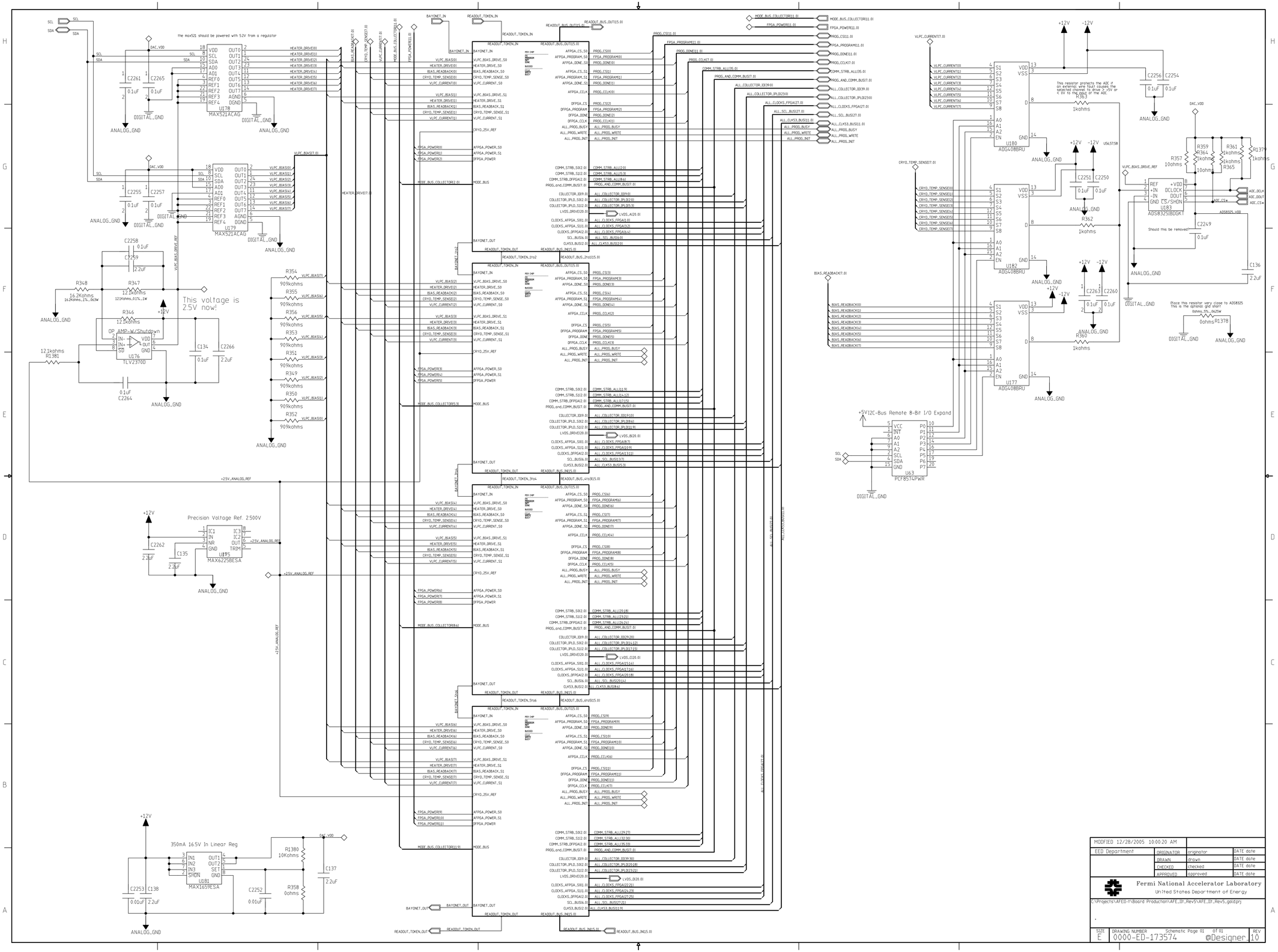
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 03 of 03 @Designer_10	

H=8ND, V=4LA


the max521 should be powered with 5.2V from a regulator
U178 MAX521ACAG
U179 MAX521ACAG
This voltage is 2.5V now!
U176 TLV2370D
Precision Voltage Ref. 2.500V
U175 MAX6225BESA
350mA 16.5V In Linear Reg
U181 MAX1659ESA
+5V I2C-Bus Remote 8-Bit I/O Expand
U63 PCF8574PWR
U180 ADG408BRU
U182 ADG408BRU
U177 ADG408BRU
U183 ADS8325IBDGKT
This resistor protects the ADC if an external wire fault causes the selected channel to drive >-5V or < 0V to the input of the ADC
Should this be removed?
Place this resistor very close to ADS8325 This is the optional gnd short
MODIFIED 12/28/2005 10:00:20 AM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
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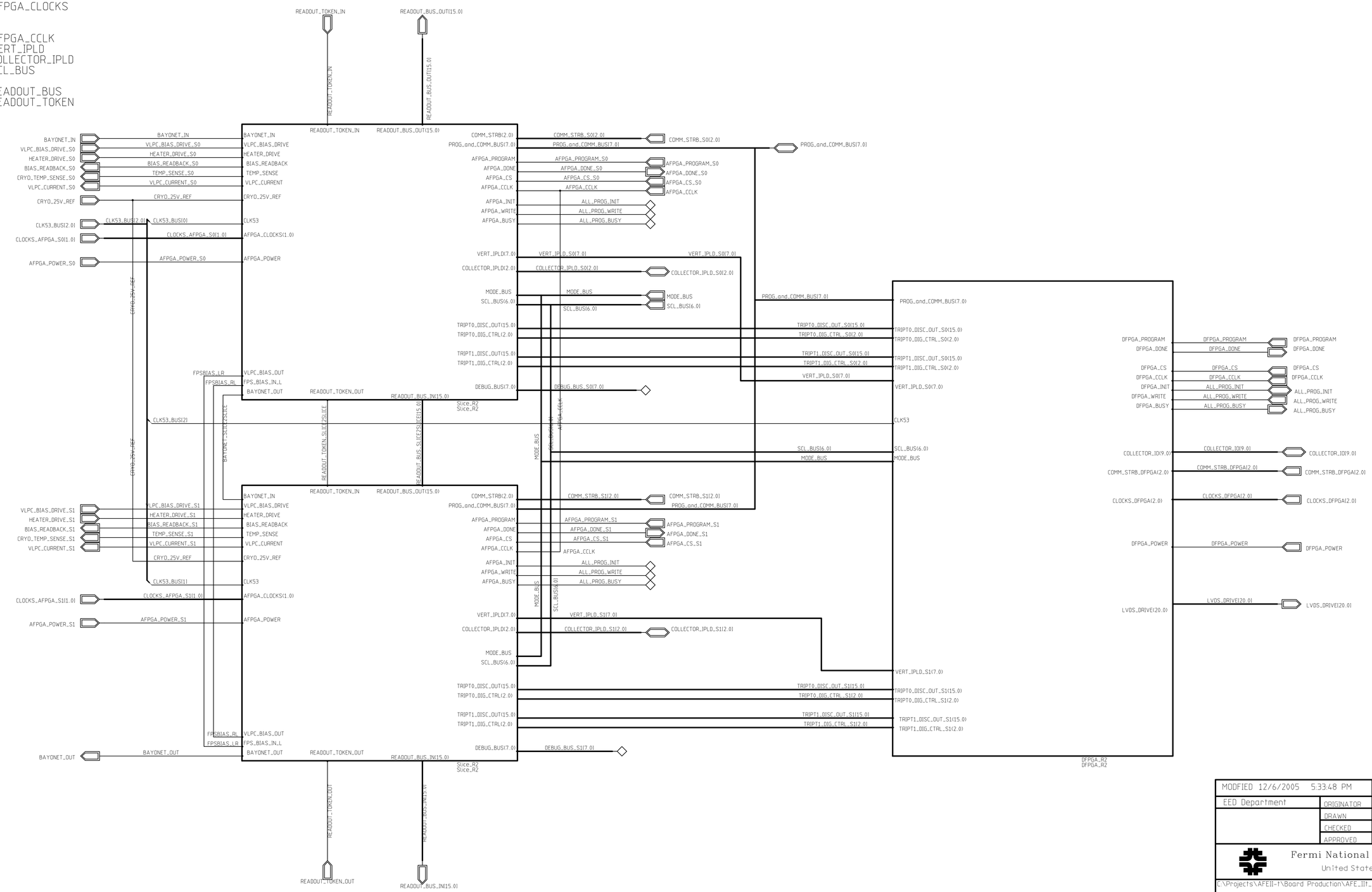
C:\Projects\AFEII-1\Board Production\AFE_III_Rev5\AFE_III_Rev5_gold.prj
SIZE E
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 01
REV @Designer_10

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



MODIFIED 12/6/2005 5:33:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	10

H:8ND, V:4LA

These go to page2 of this schematic

DFPGA_VCC → DFPGA_VCC
DFPGA_POWER → DFPGA_POWER_EN
TRIPT0_DIG_CTRL_S0(2.0) → TRIPT0_DIG_CTRL_S0(2.0)
TRIPT1_DIG_CTRL_S0(2.0) → TRIPT1_DIG_CTRL_S0(2.0)
TRIPT0_DIG_CTRL_S1(2.0) → TRIPT0_DIG_CTRL_S1(2.0)
TRIPT1_DIG_CTRL_S1(2.0) → TRIPT1_DIG_CTRL_S1(2.0)
DIG_CTRL(0) = DIG_RSTB
DIG_CTRL(1) = DIG_ENU
DIG_CTRL(2) = DIG_ENL
ALL_DIG_CTRL0
ALL_DIG_CTRL1
ALL_DIG_CTRL2

TRIPT0_DISC_OUT_S1(15.0) → DISC(63:48)
TRIPT1_DISC_OUT_S1(15.0) → DISC(47:32)
TRIPT0_DISC_OUT_S0(15.0) → DISC(31:16)
TRIPT1_DISC_OUT_S0(15.0) → DISC(15.0)

CLOCKS_DFPGA(2) → R156 1kohms → DIGITAL_GND
CLOCKS_DFPGA(1) → R133 1kohms → DIGITAL_GND
CLOCKS_DFPGA(0) → R132 1kohms → DIGITAL_GND
CLK53 → R155 1kohms → DIGITAL_GND

R153 1kohms
R152 1kohms
R154 1kohms
DIGITAL_GND

CLOCKS_DFPGA(2)
CLOCKS_DFPGA(1)
CLOCKS_DFPGA(0)
VERT_IPLD_S0(7.0) → VERT_IPLD_S0(7.0)
CLOCKS_DFPGA(2.0) → CLOCKS_DFPGA(2.0)
COLLECTOR_ID(9.0) → COLLECTOR_ID(9.0)

TS8
SAMTEC_TS-106-T-A-1
TMS, TCK, TDI, TDO, JTAG_VCC
A1, A2, A3, A4, A5, A6
R21 49.9ohms → DIGITAL_GND

XILINX
U78
XC2S150-5PQ208C

DFPGA_CCLK → DFPGA_CCLK
DFPGA_BUSY → DFPGA_BUSY
LVDS_DRIVE(20.0) → LVDS_DRIVE(20.0)
SCL_BUS(6.0) → SCL_BUS(6.0)
DFPGA_INIT → DFPGA_INIT
DFPGA_PROGRAM → DFPGA_PROGRAM
PROG_and_COMM_BUS(7.0)
DFPGA_DONE → DFPGA_DONE
MODE_BUS → MODE_BUS
VERT_IPLD_S1(7.0) → VERT_IPLD_S1(7.0)
COMM_STRB_DFPGA(2.0) → COMM_STRB_DFPGA(2.0)

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	APPROVED	approved	DATE date

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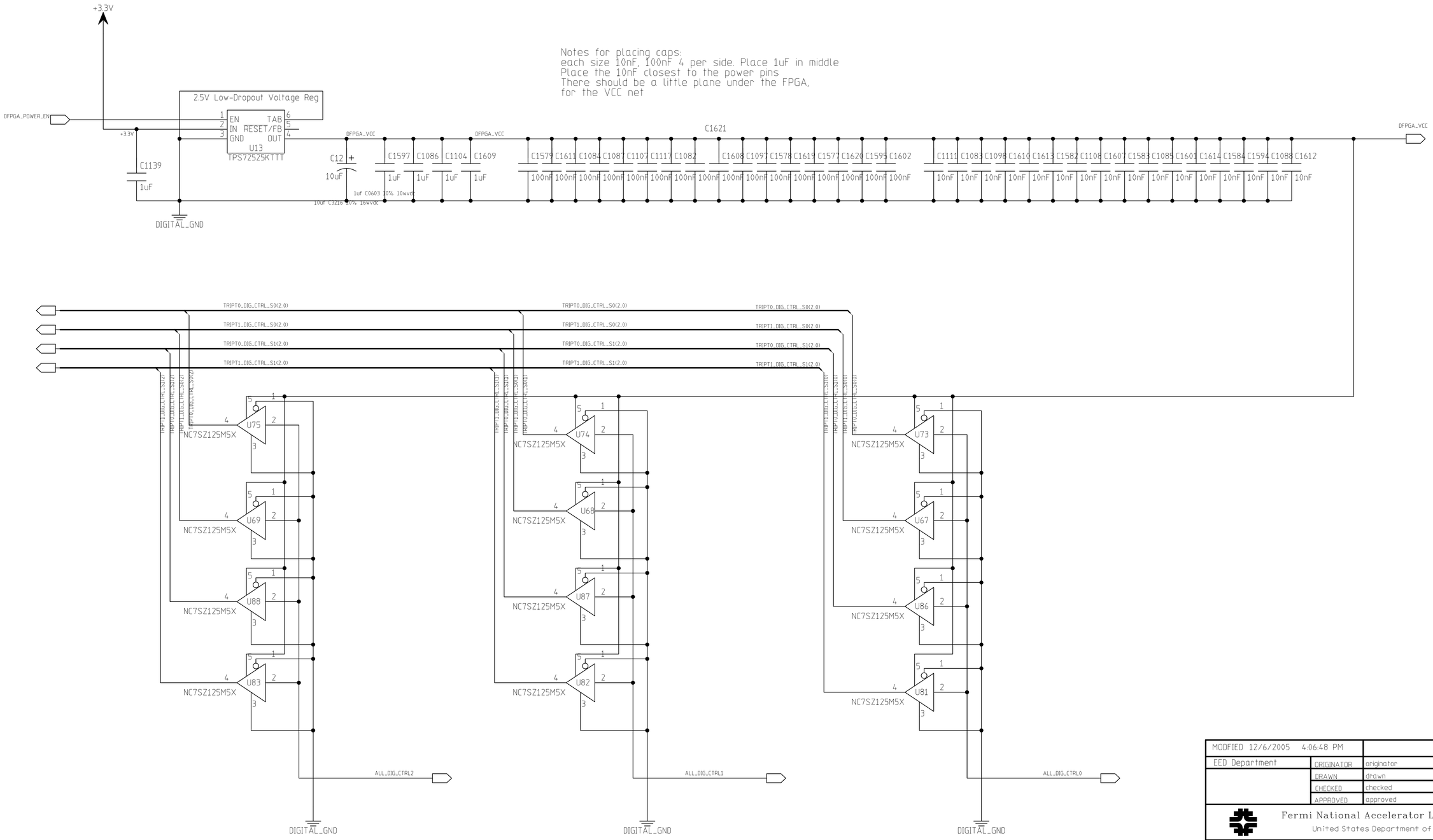
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_1	10

H:8ND, V:4LA



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

MODFIED 12/6/2005 4:06:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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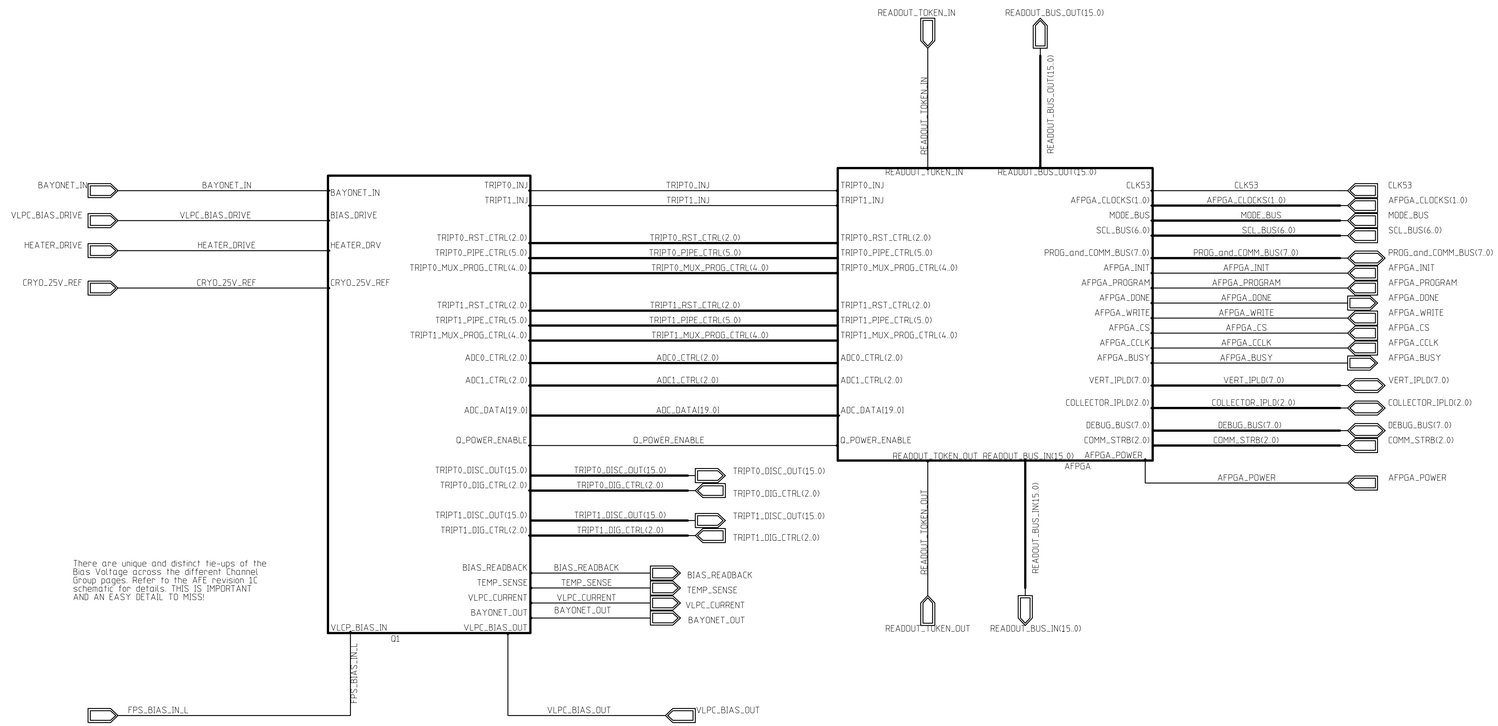
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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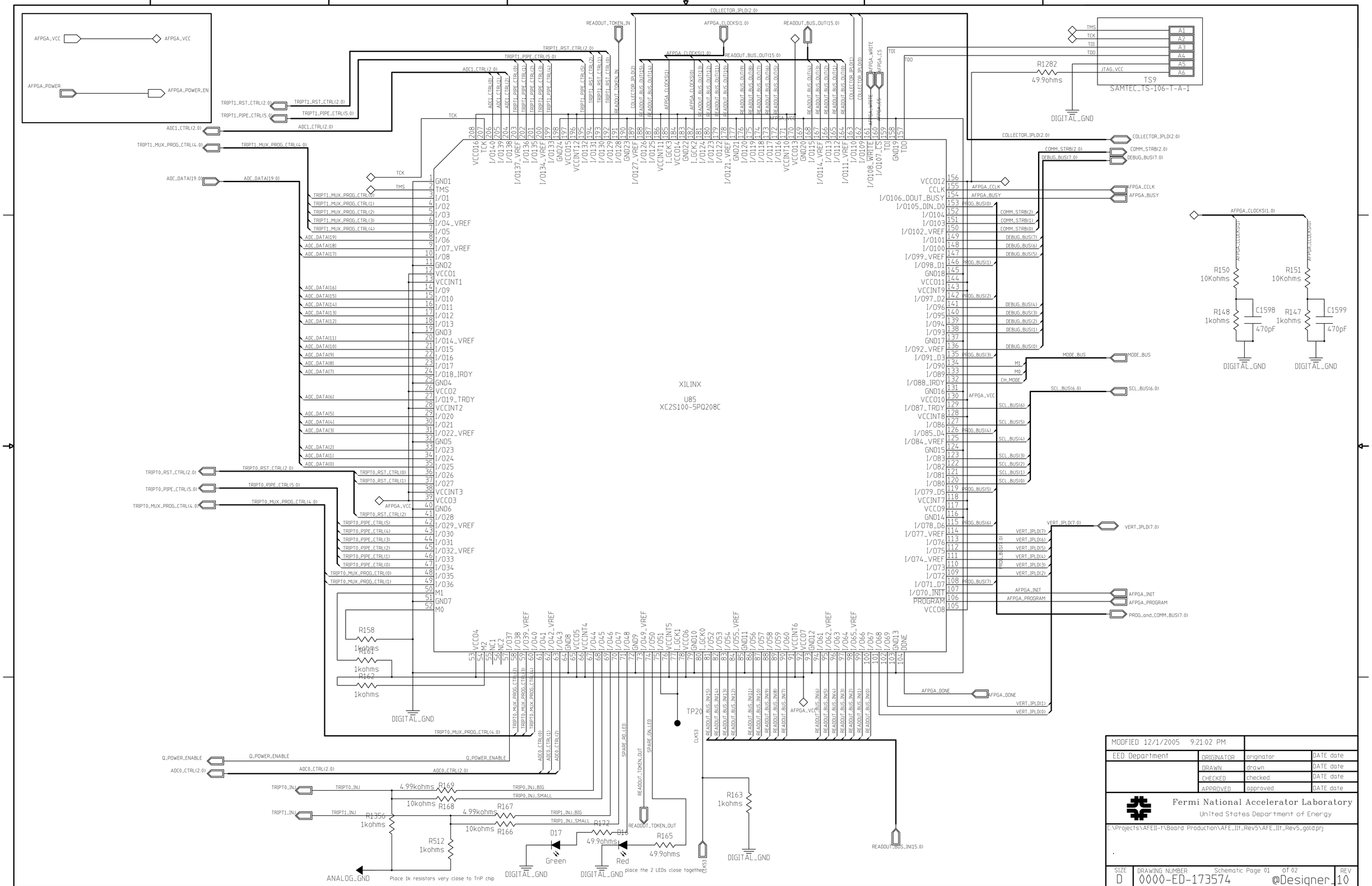
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA


XILINX
U85
XC2S100-5PQ208C
TS9
SAMTEC_TS-106-T-A-1
R1282
49.9ohms
R150
10Kohms
R151
10Kohms
R148
1kohms
R147
1kohms
C1598
470pF
C1599
470pF
R158
1kohms
R161
1kohms
R162
1kohms
R169
4.99kohms
R168
10kohms
R167
4.99kohms
R166
10kohms
R1356
1kohms
R512
1kohms
R172
49.9ohms
R165
49.9ohms
R163
1kohms
D17
Green
D16
Red
TP20
DIGITAL_GND
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
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ORIGINATOR
DRAWN
CHECKED
APPROVED
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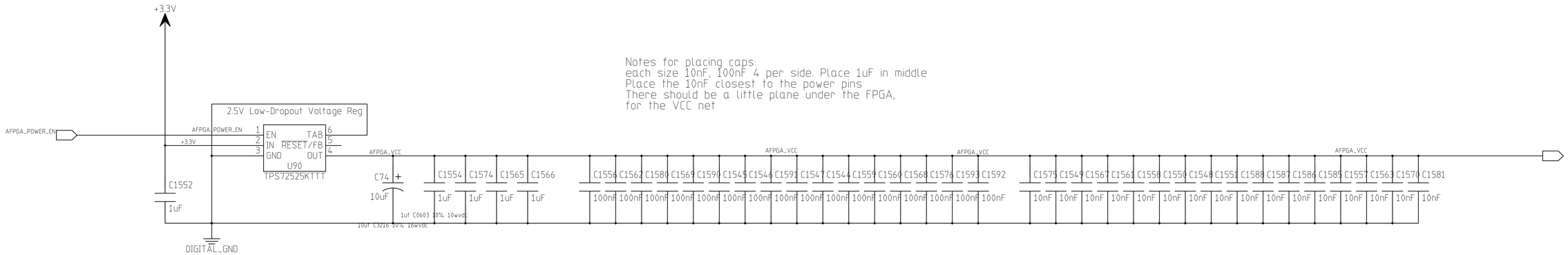
SIZE
D
DRAWING NUMBER
0000-ED-173574
Schematic Page 01 of 02
@Designer
REV
10



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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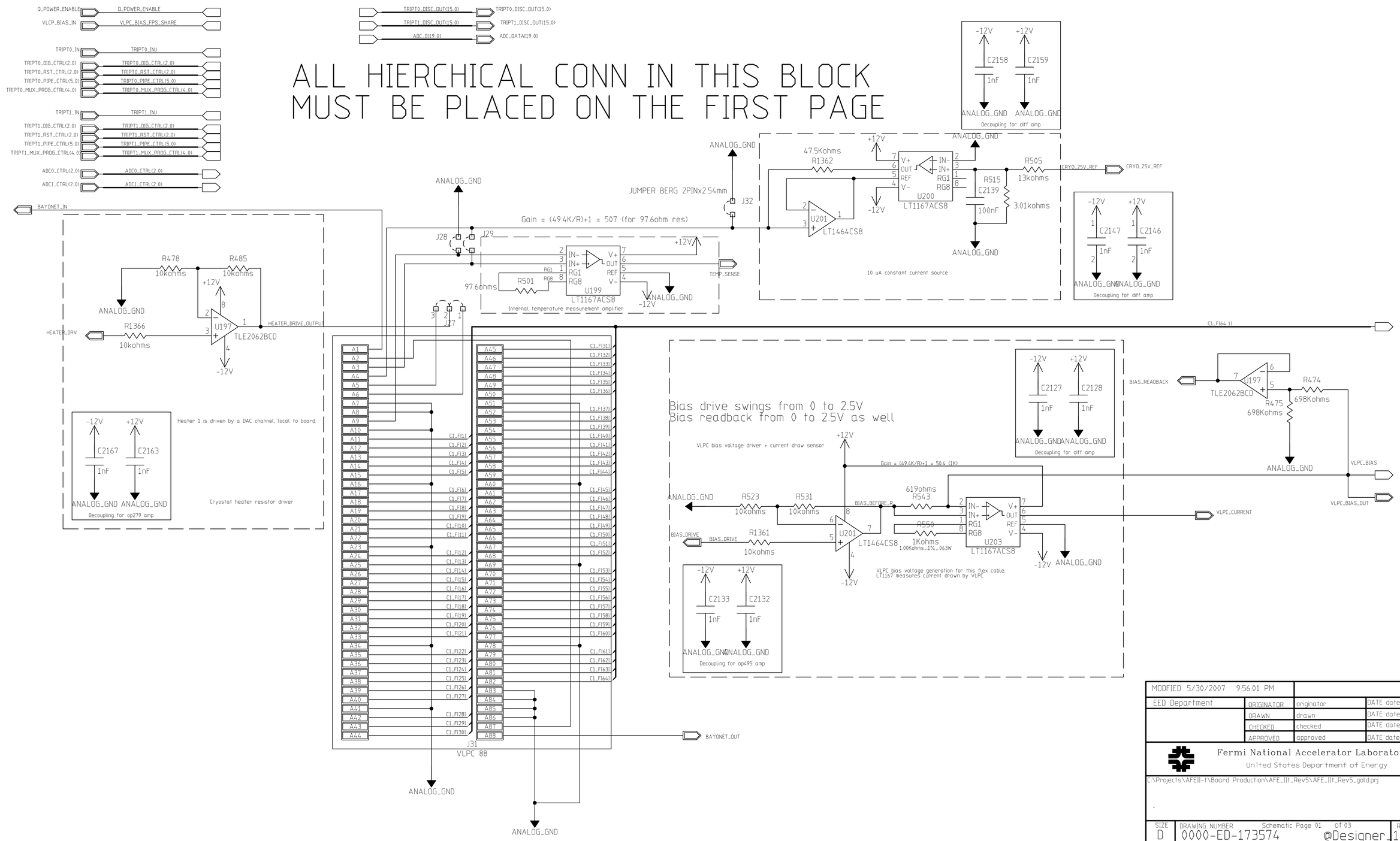
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H=8ND, V=4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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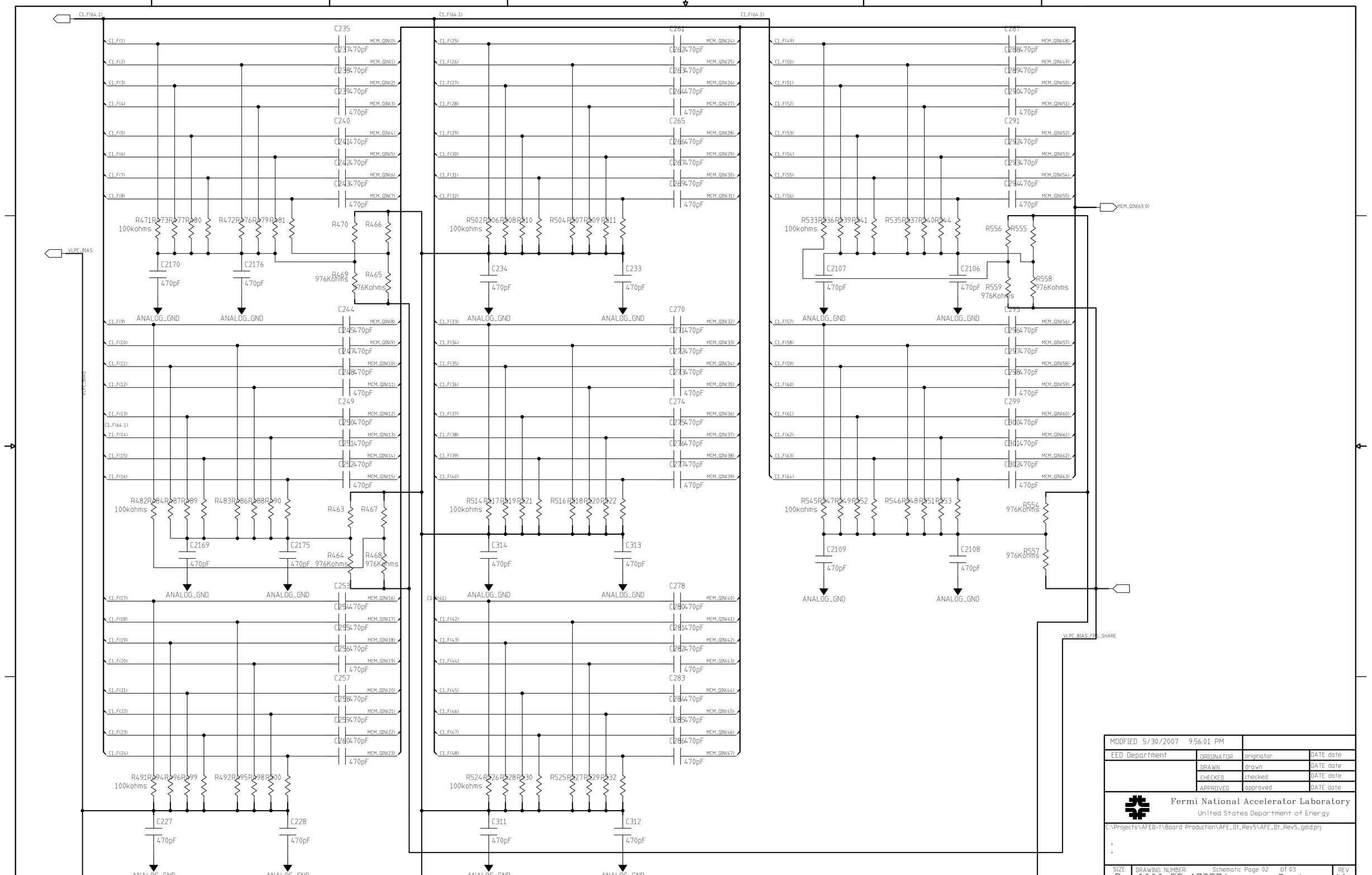
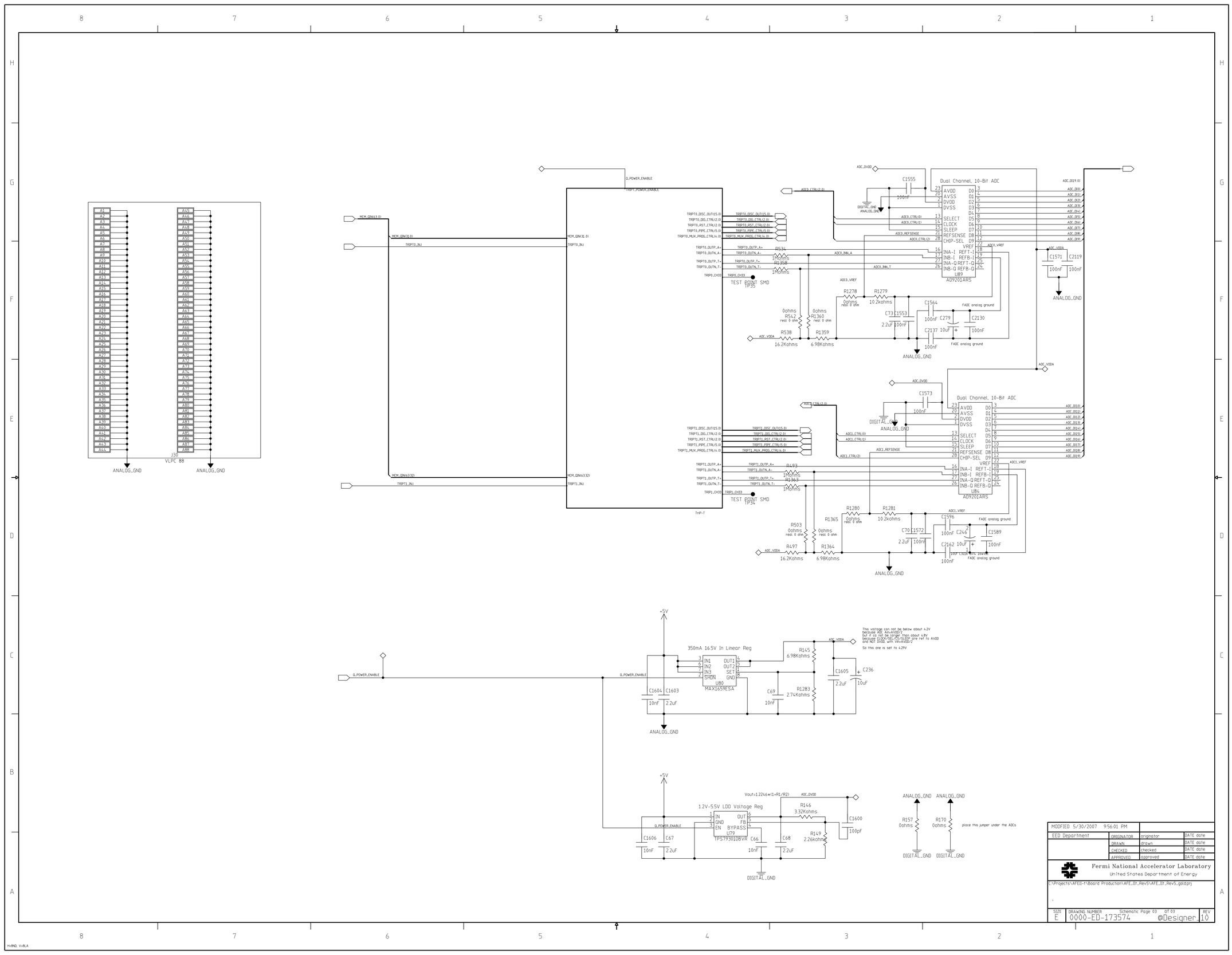
C:\Projects\AFEII-1\Board Production\AFE_II1_Rev5\AFE_II1_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer_1	0

H:8ND, V:4LA


C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
470pF
100kohms
976Kohms
MODFIED 5/30/2007 9:56:01 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H:8ND, V:4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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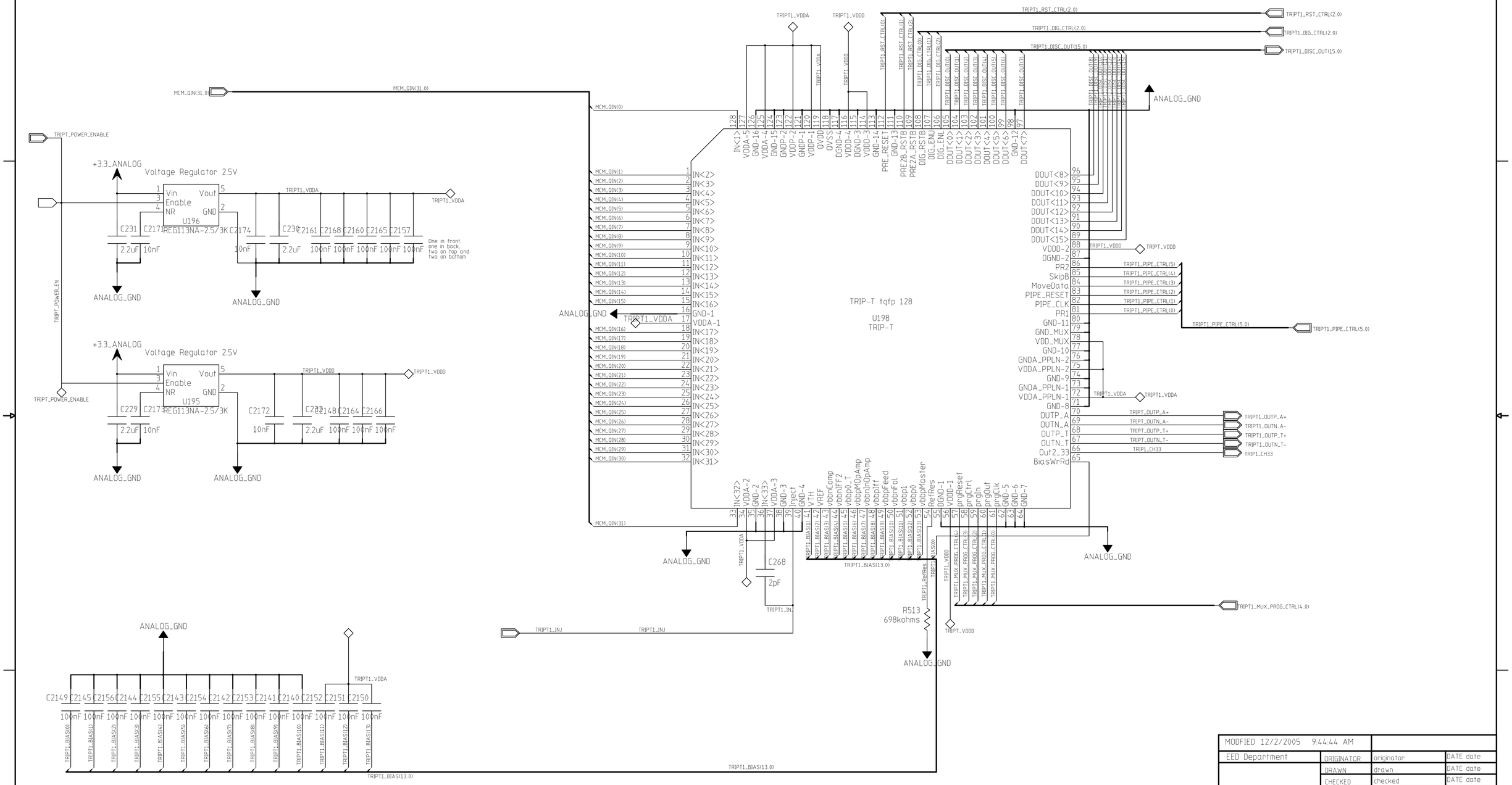
SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

H:\BND, V:\BLA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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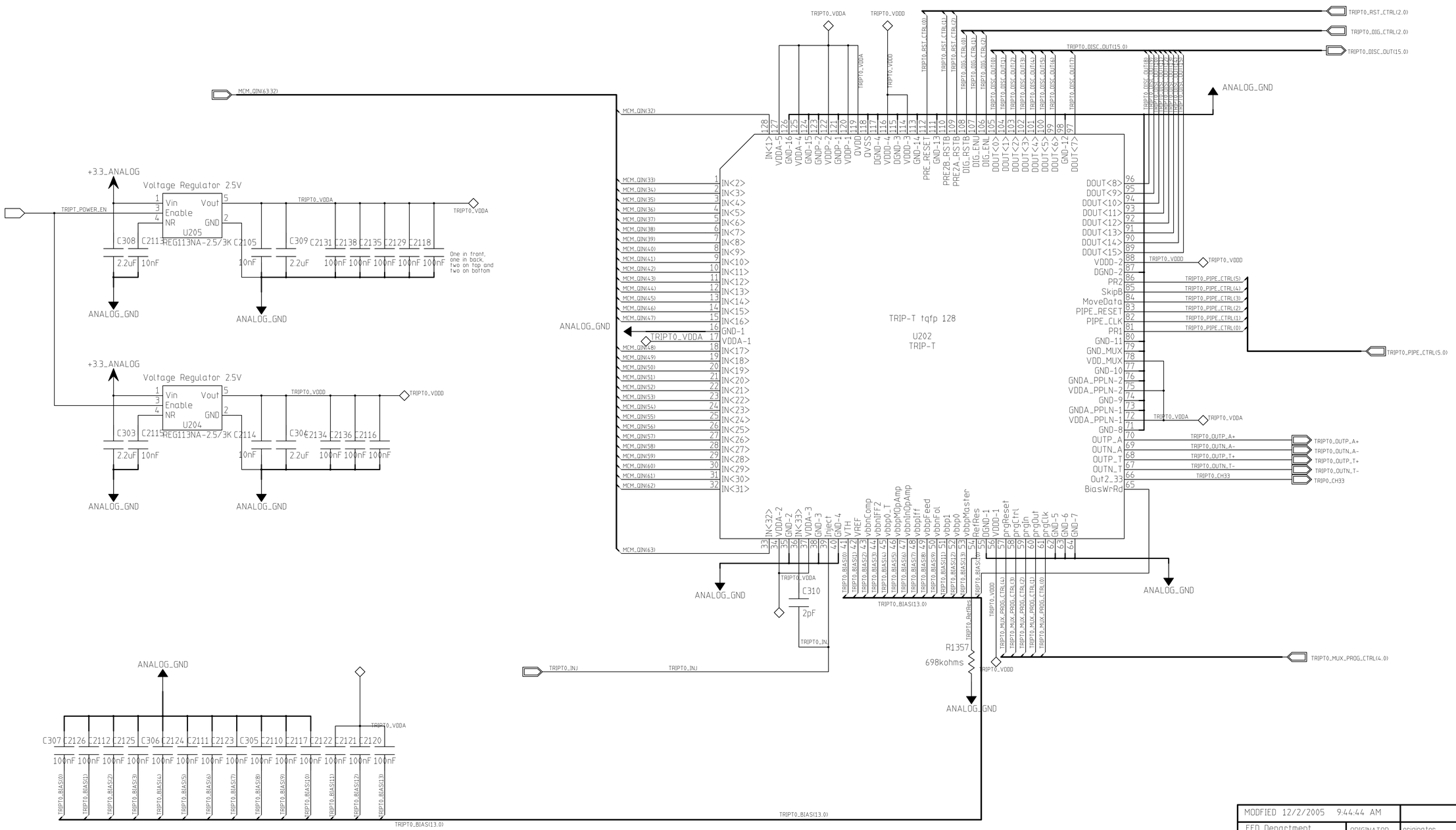
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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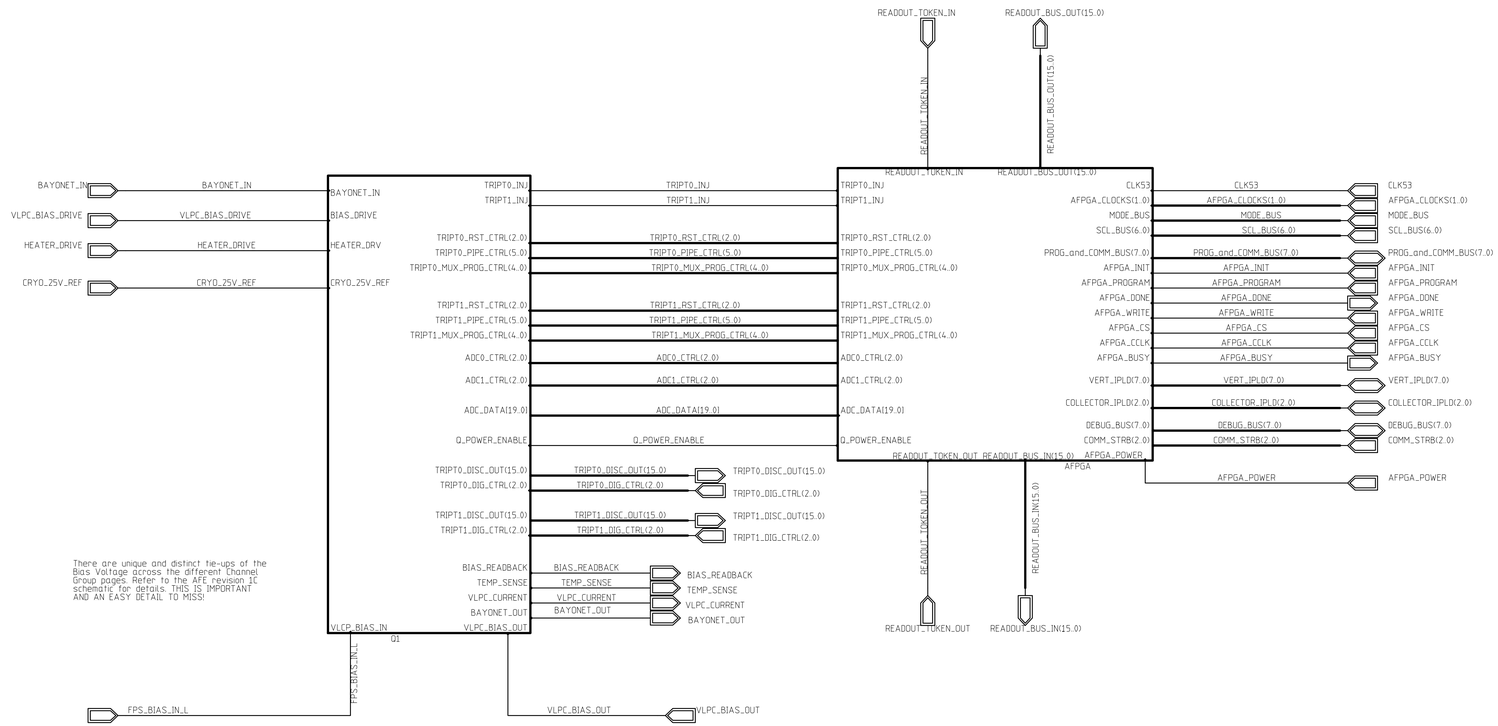
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H=8ND, V=4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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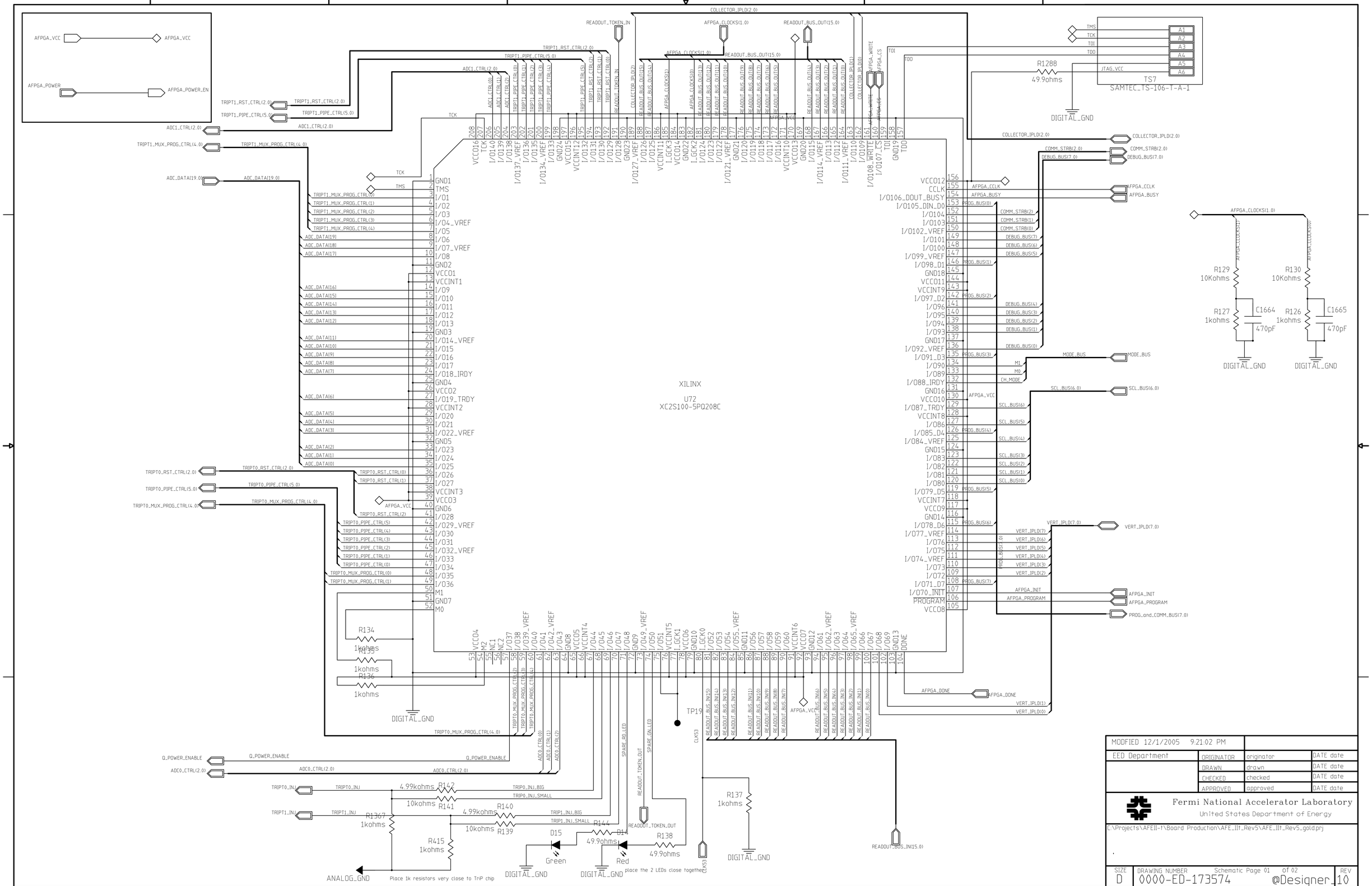
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA


XILINX
U72
XC2S100-5PQ208C
TS7
SAMTEC_TS-106-T-A-1
R1288
49.9ohms
R129
10Kohms
R130
10Kohms
R127
1kohms
R126
1kohms
C1664
470pF
C1665
470pF
R134
1kohms
R135
1kohms
R136
1kohms
R142
4.99kohms
R141
10kohms
R140
4.99kohms
R139
10kohms
R1367
1kohms
R415
1kohms
R144
49.9ohms
R138
49.9ohms
R137
1kohms
D15
Green
D14
Red
TP19
DIGITAL_GND
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
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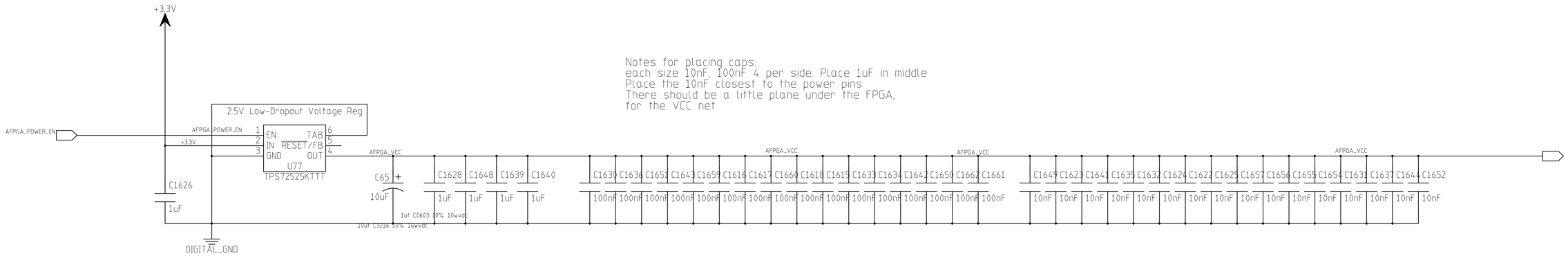
0000-ED-173574
Schematic Page 01 of 02
@Designer
REV
10



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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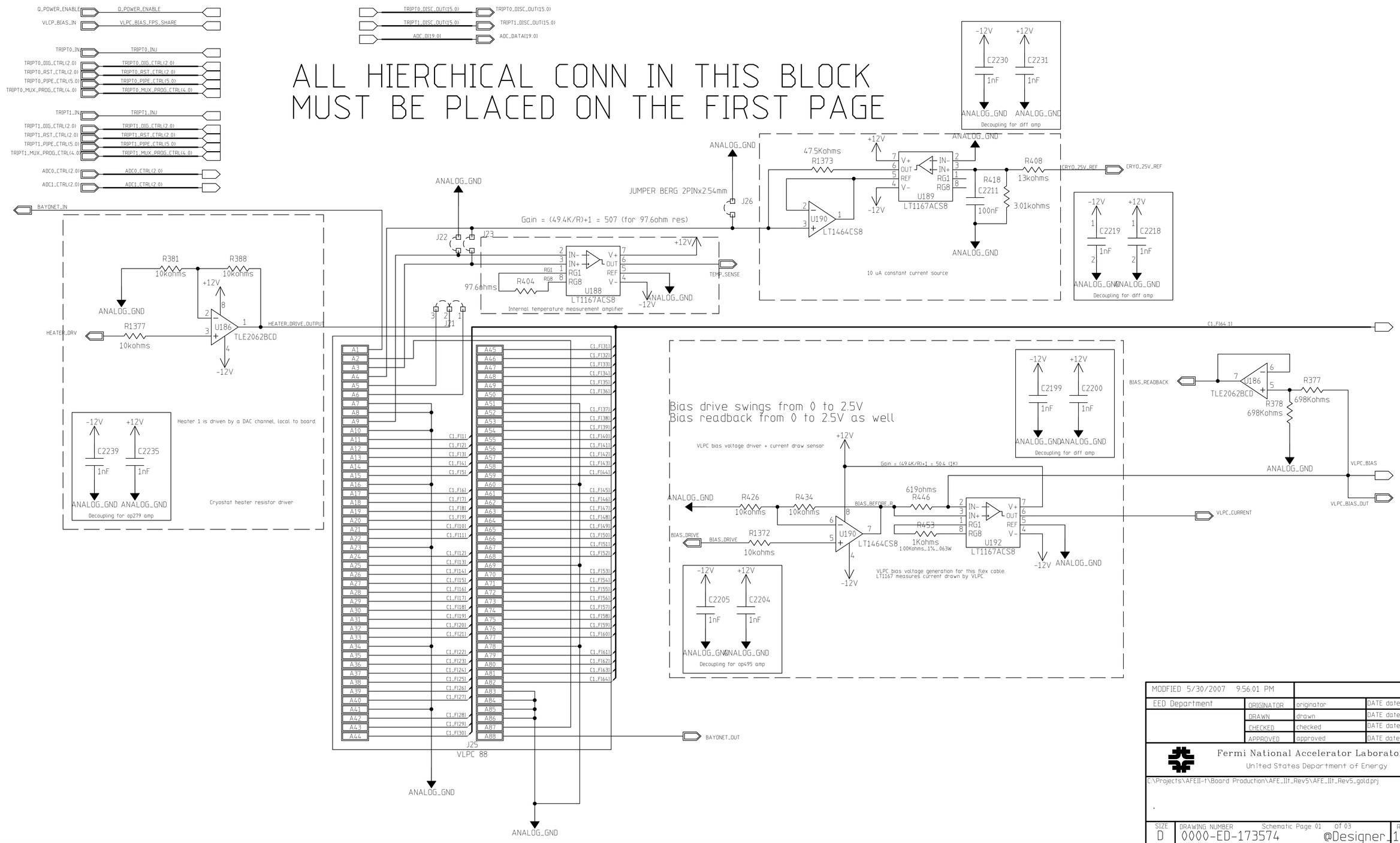
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H:8ND, V:4LA



MODIFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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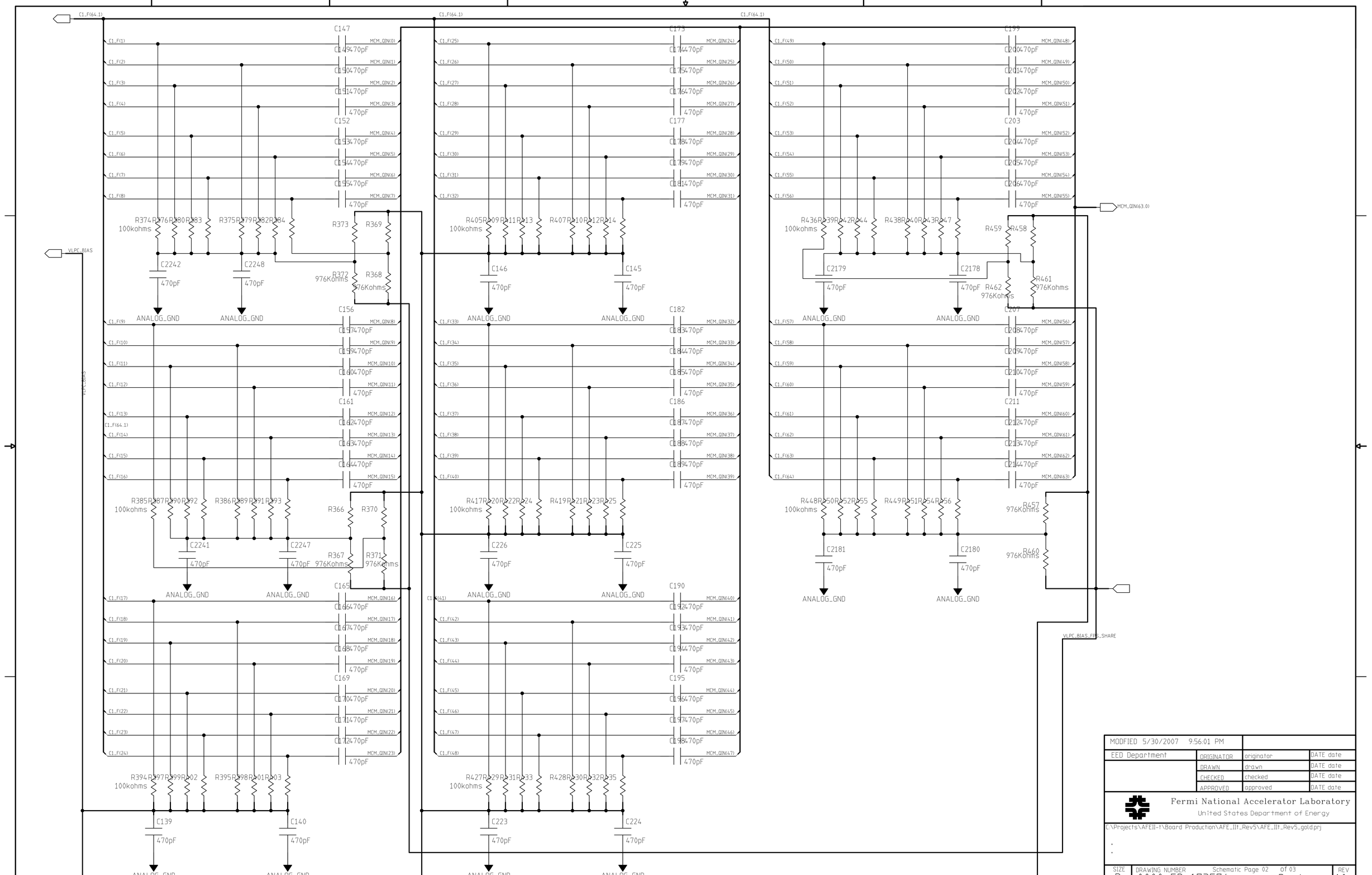
C:\Projects\AFEII-1\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer_1	0

H:8ND, V:4LA


C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
R374 R376 R380 R383 R375 R379 R382 R384
100kohms
R373 R369 R372 R368
976Kohms
C2242 C2248 C146 C145
470pF
R405 R409 R411 R413 R407 R410 R412 R414
R436 R439 R442 R444 R438 R440 R443 R447
R459 R458 R461 R462
C2179 C2178
R385 R387 R390 R392 R386 R389 R391 R393
R366 R370 R367 R371
C2241 C2247
R417 R420 R422 R424 R419 R421 R423 R425
R448 R450 R452 R455 R449 R451 R454 R456
R457 R460
C2226 C2225 C2181 C2180
R394 R397 R399 R402 R395 R398 R401 R403
R427 R429 R431 R433 R428 R430 R432 R435
C139 C140 C223 C224
C147 C149 C150 C151 C152 C153 C154 C155 C156 C157 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C170 C171 C172
C173 C174 C175 C176 C177 C178 C179 C181 C182 C183 C184 C185 C186 C187 C188 C189 C190 C192 C193 C194 C195 C196 C197 C198
C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211 C212 C213 C214
470pF
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ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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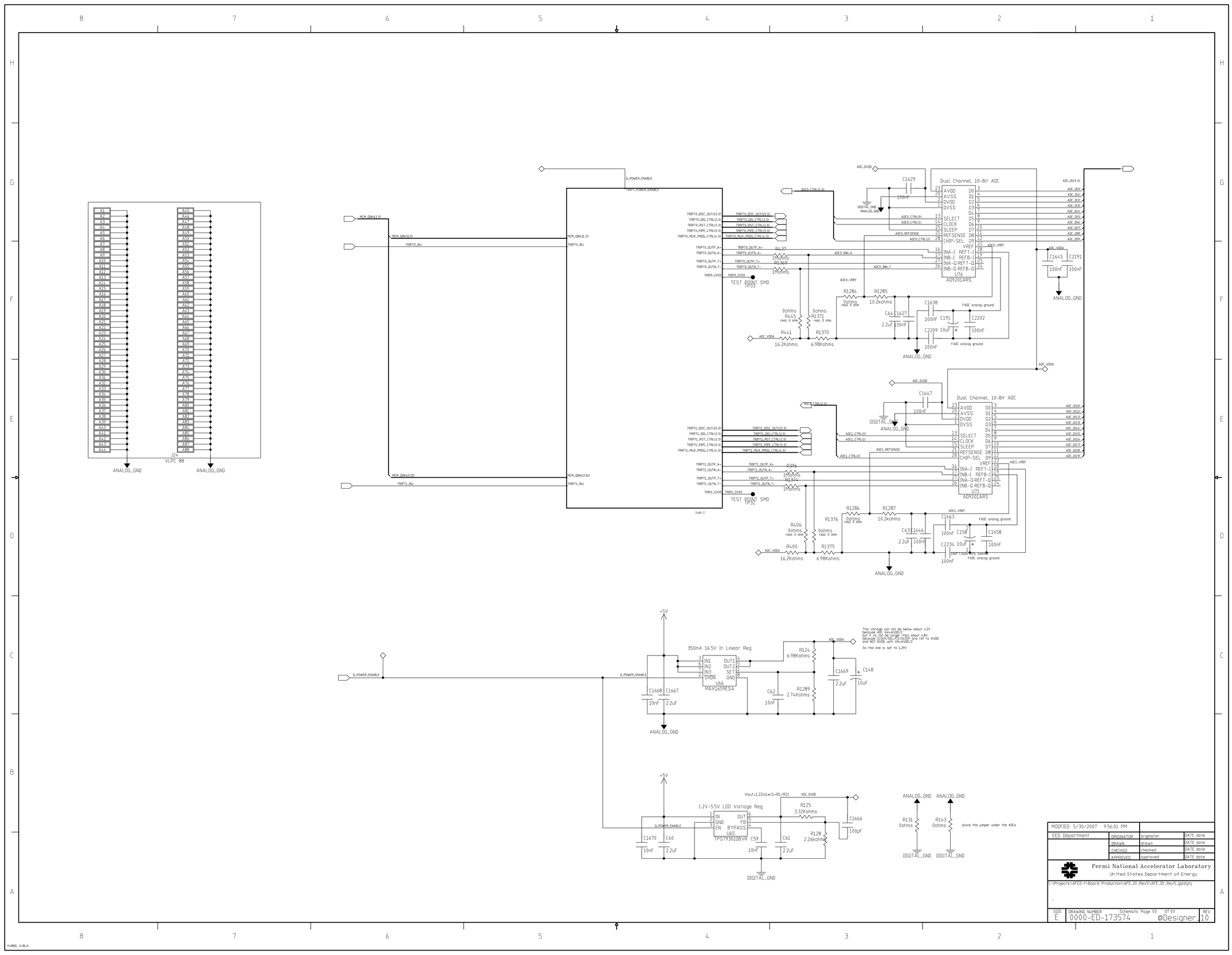
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H=8ND, V=4LA



MODFIED 5/30/2007 9:56:01 PM

EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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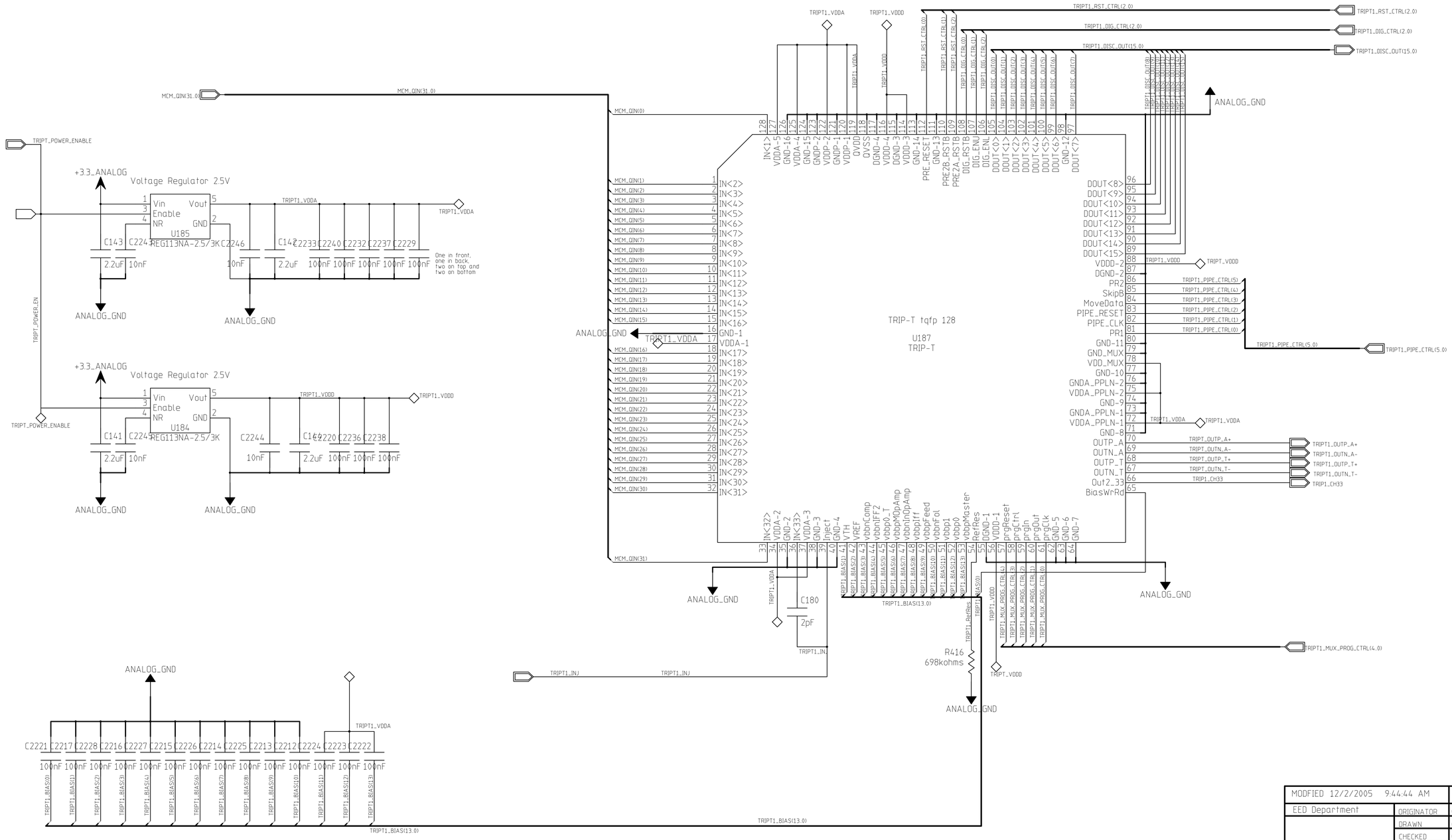
SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

H:\BND, V:\BLA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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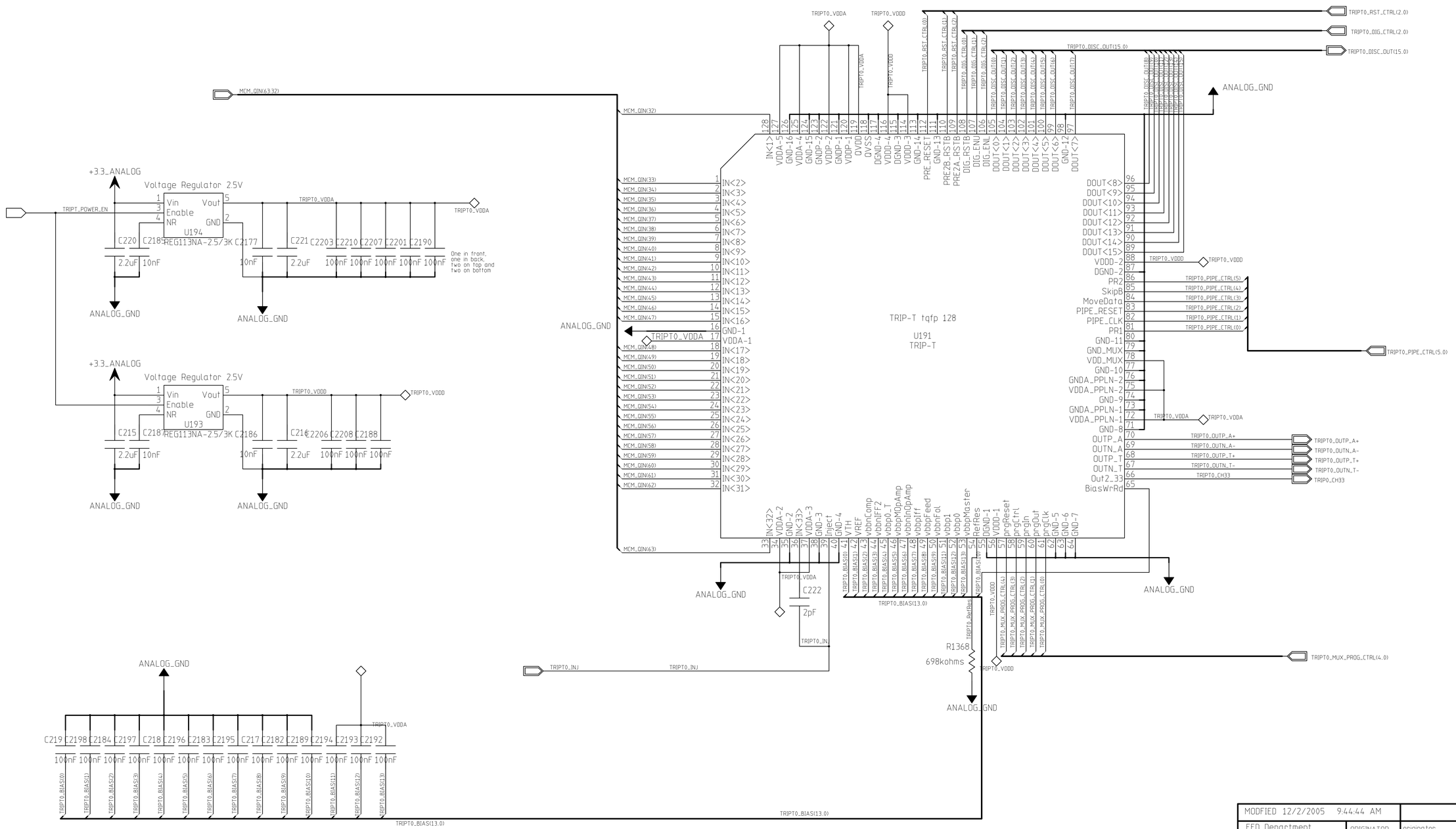
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

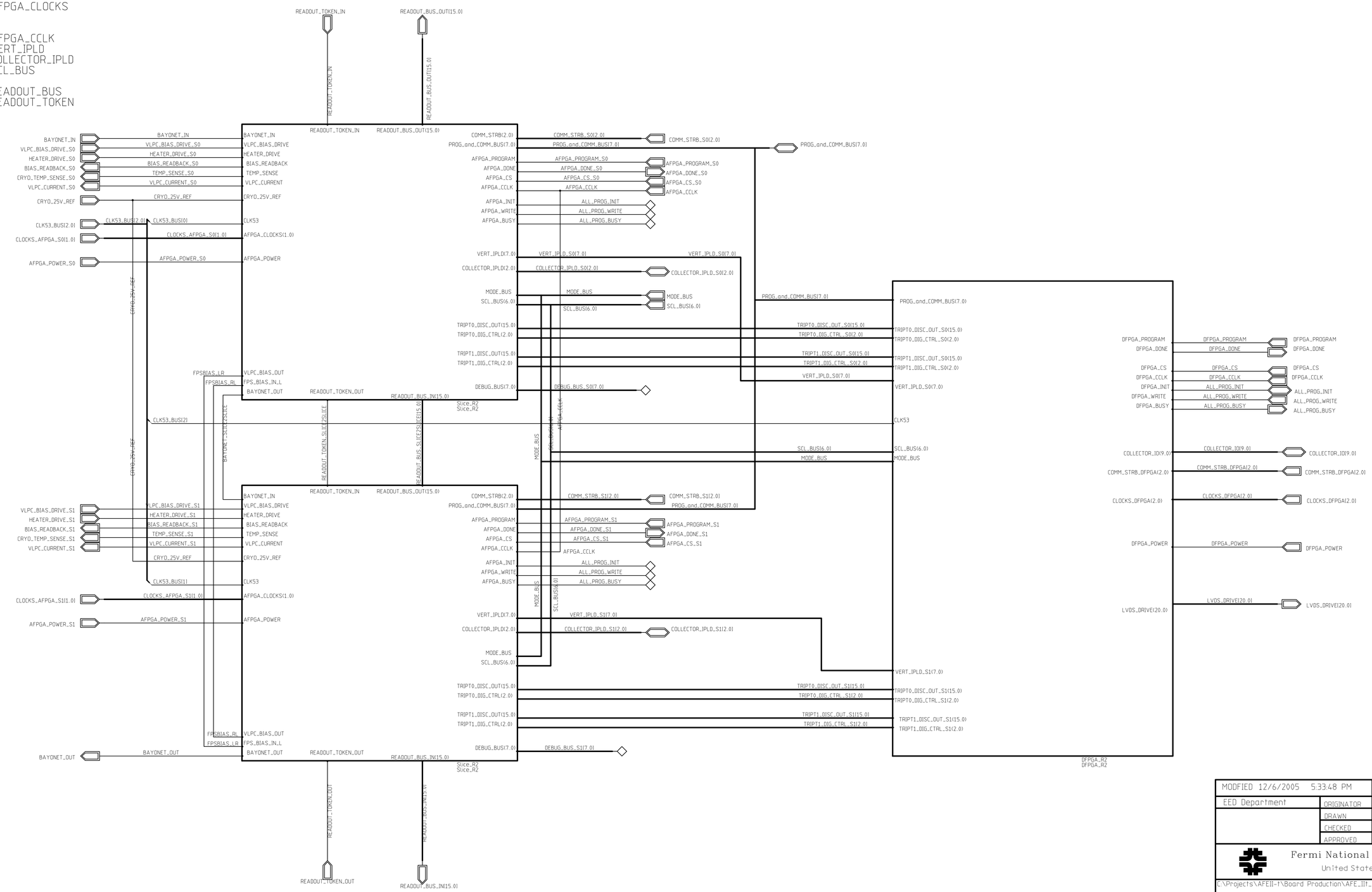
H=8ND, V=4LA

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



MODIFIED 12/6/2005 5:33:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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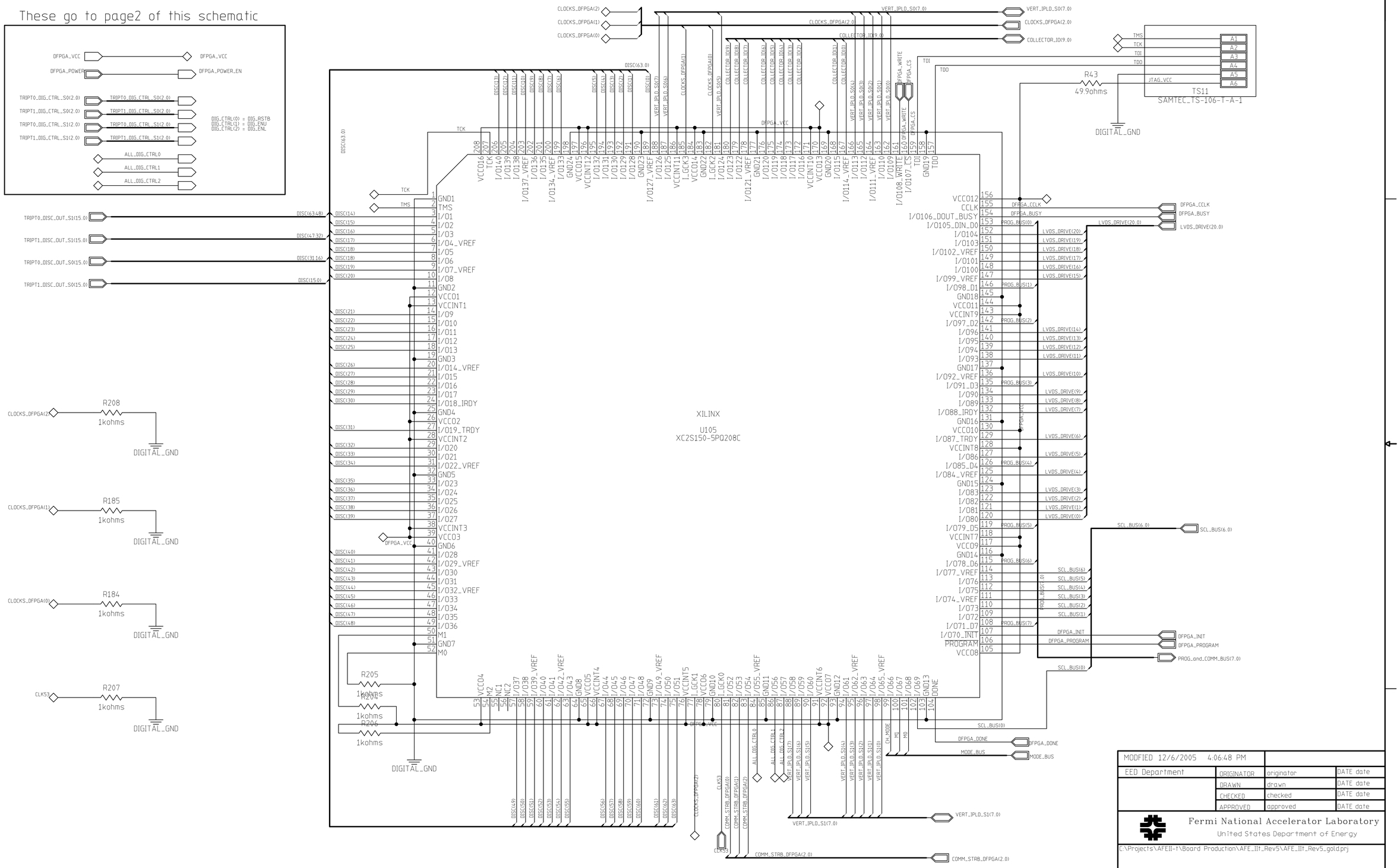
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	10

H:8ND, V:4LA



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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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SIZE D | DRAWING NUMBER 0000-ED-173574 | Schematic Page 01 of 02 | REV 10

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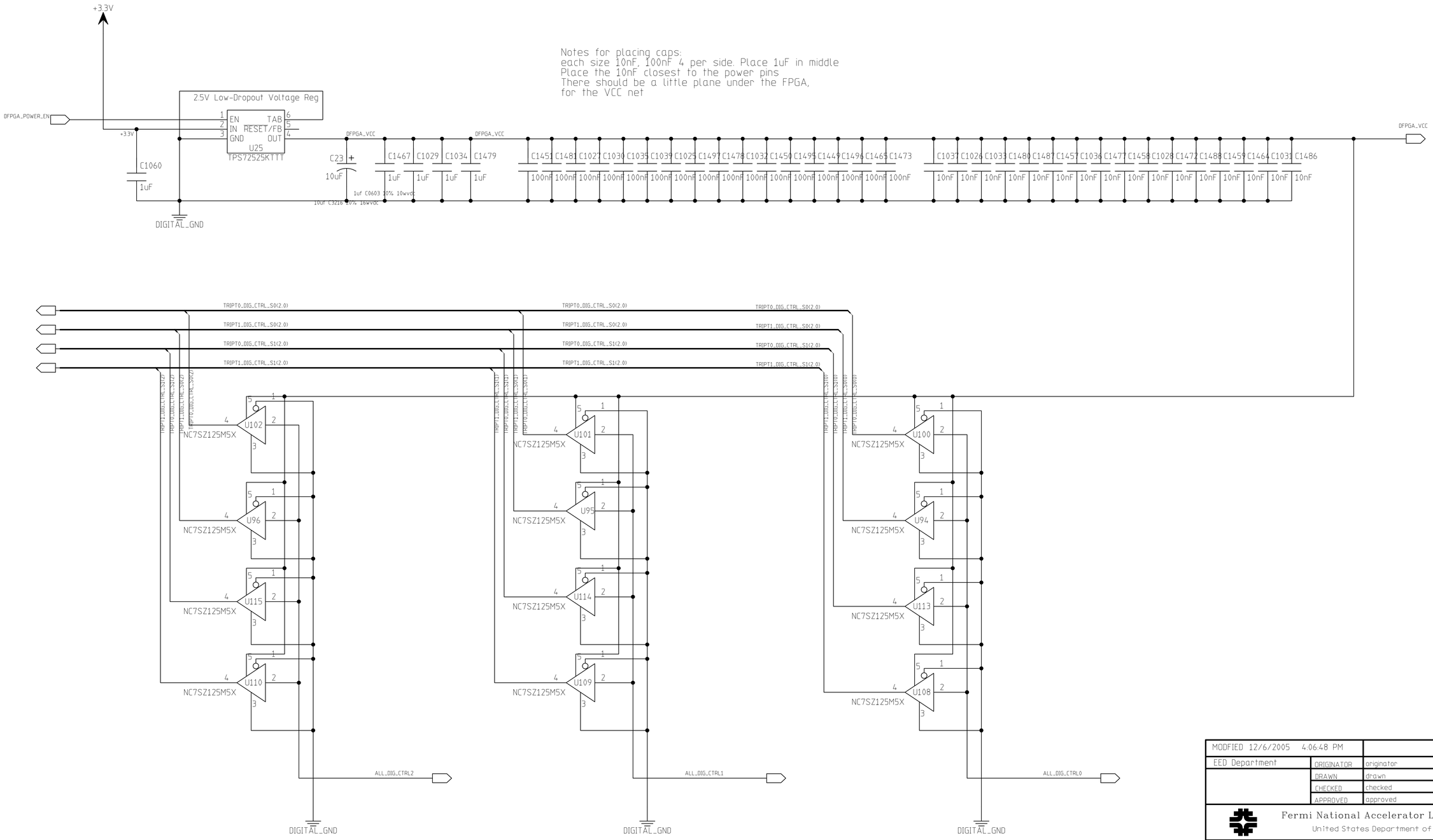
H:8ND, V:4LA



MODFIED 12/6/2005 4:06:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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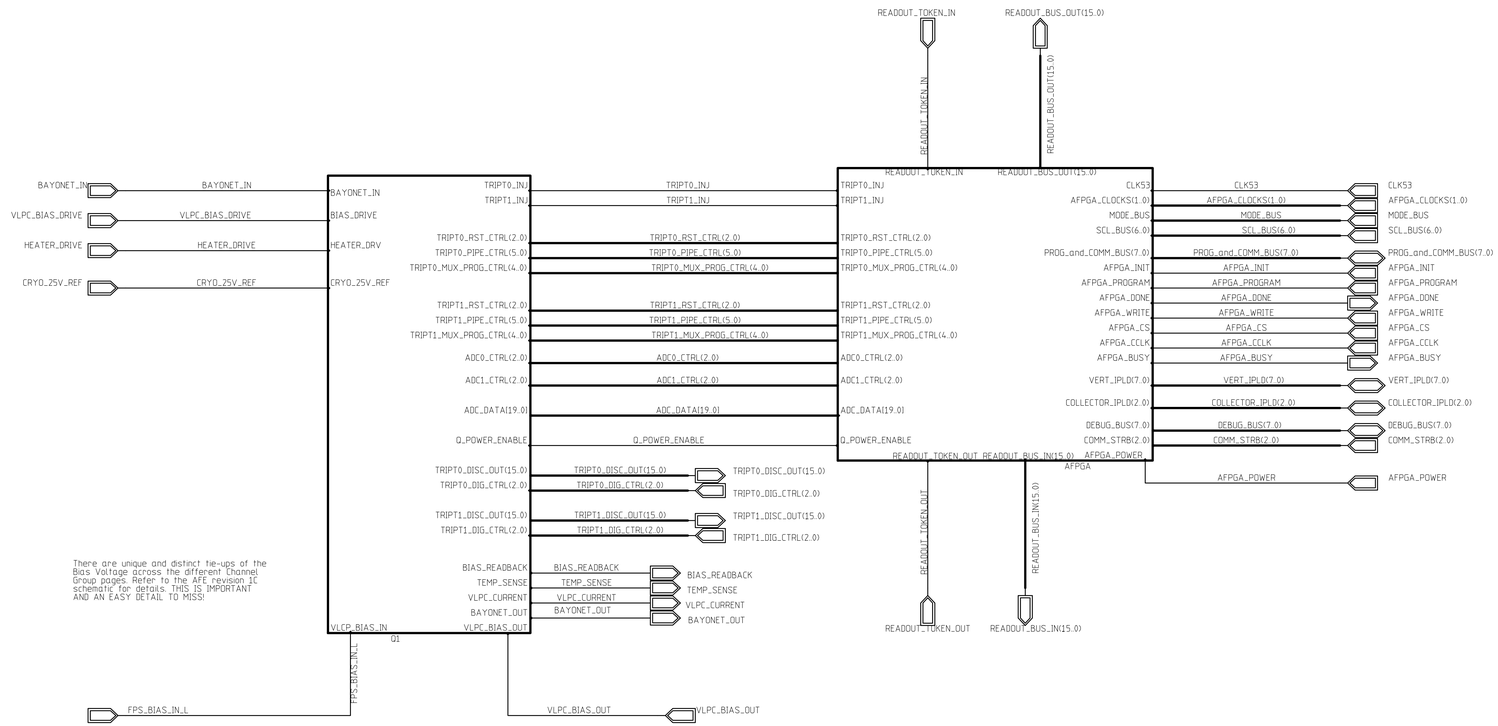
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H=8ND, V=4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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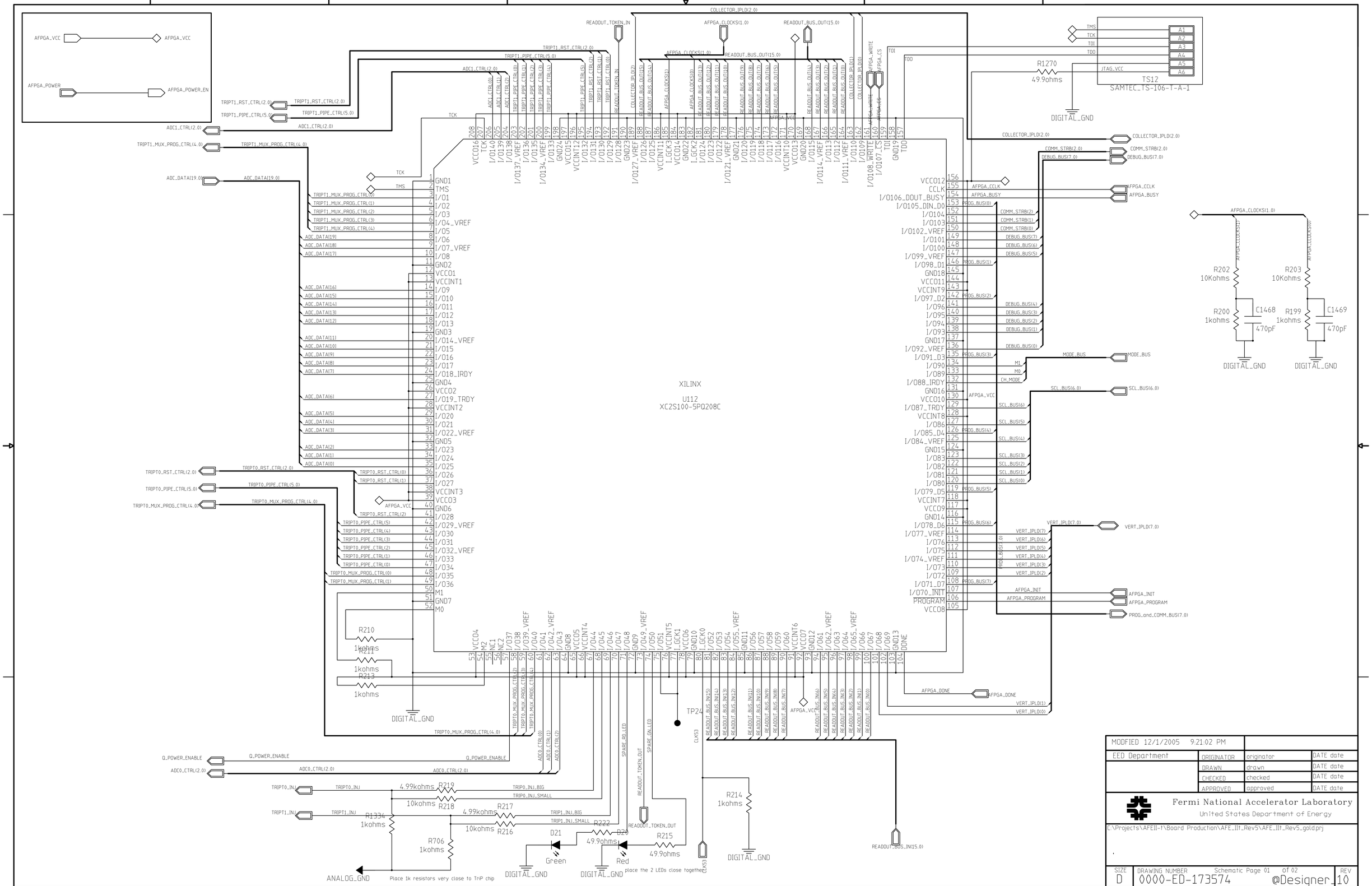
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA


XILINX
U112
XC2S100-5PQ208C
SAMTEC_TS-106-T-A-1
TS12
R1270
49.9ohms
DIGITAL_GND
R202
10Kohms
R203
10Kohms
R200
1kohms
R199
1kohms
C1468
470pF
C1469
470pF
R210
1kohms
R211
1kohms
R213
1kohms
R219
4.99kohms
R218
10kohms
R217
4.99kohms
R216
10kohms
R1334
1kohms
R706
1kohms
R222
49.9ohms
R215
49.9ohms
R214
1kohms
D21
Green
D20
Red
TP24
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
EED Department
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APPROVED
Fermi National Accelerator Laboratory
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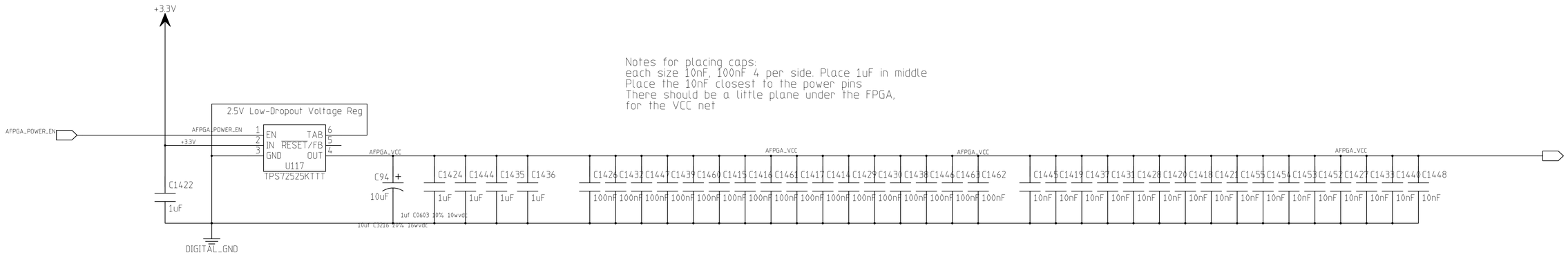
C:\Projects\AFEII-1\Board Production\AFE_II_Rev5\AFE_II_Rev5_gold.prj
SIZE
D
DRAWING NUMBER
0000-ED-173574
Schematic Page 01 of 02
REV
10
@Designer



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

MODFIED 12/1/2005 9:21:02 PM			
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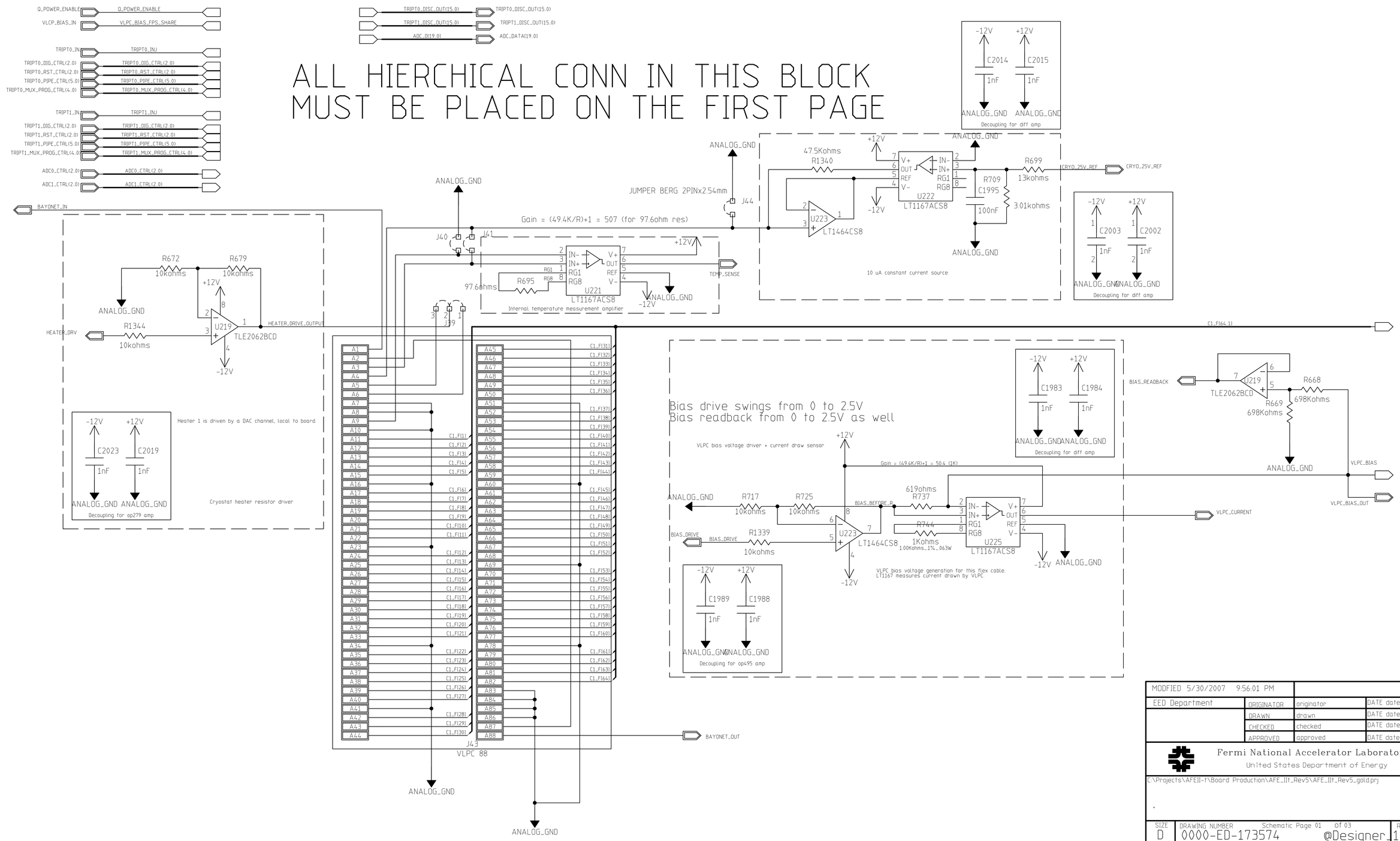
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H=8ND, V=4LA


ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
BAYONET_IN
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
ANALOG_GND
JUMPER BERG 2PINx2.54mm
J44
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
J40
J41
R672
10kohms
R679
10kohms
+12V
U219
TLE2062BCD
HEATER_DRIVE_OUTPUT
HEATER_DRV
R1344
10kohms
-12V
C2023
C2019
1nF
Decoupling for op279 amp
Heater 1 is driven by a DAC channel, local to board
Cryostat heater resistor driver
97.6ohms
R695
U221
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
J39
J43
VLPC 88
BAYONET_OUT
C1_FI64.1
47.5Kohms
R1340
U223
LT1464CS8
U222
LT1167ACS8
R709
C1995
100nF
3.01kohms
R699
13kohms
CRYO_25V_REF
10 uA constant current source
C2014
C2015
Decoupling for diff amp
C2003
C2002
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R717
10kohms
R725
10kohms
BIAS_BEFORE_R
619ohms
R737
R744
1Kohms
1.00Kohms_1%_.063W
R1339
10kohms
BIAS_DRIVE
U225
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
C1989
C1988
Decoupling for op495 amp
C1983
C1984
BIAS_READBACK
U219
TLE2062BCD
R668
698Kohms
R669
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
VLPC_CURRENT
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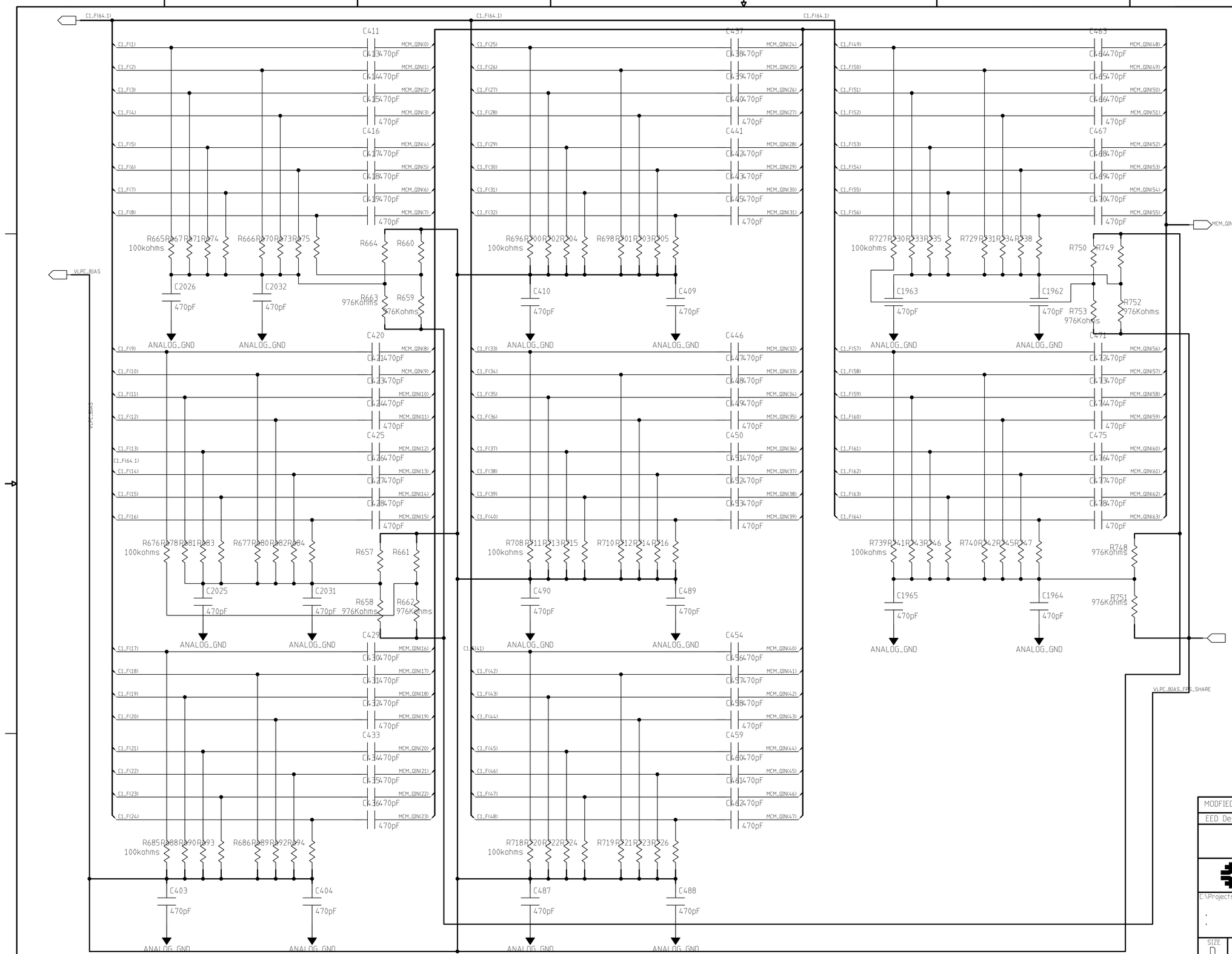
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV
H=8ND, V=4LA


C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
R665 R667 R671 R674 R666 R670 R673 R675
100kohms
R664 R660
R663 R659
976Kohms
C2026 C2032
470pF
R696 R700 R702 R704 R698 R701 R703 R705
R727 R730 R733 R735 R729 R731 R734 R738
R750 R749
R753 R752
C1963 C1962
R676 R678 R681 R683 R677 R680 R682 R684
R657 R661
R658 R662
C2025 C2031
R708 R711 R713 R715 R710 R712 R714 R716
R739 R741 R743 R746 R740 R742 R745 R747
R748 R751
C1965 C1964
R685 R688 R690 R693 R686 R689 R692 R694
C403 C404
R718 R720 R722 R724 R719 R721 R723 R726
C487 C488
C490 C489
C410 C409
MODFIED 5/30/2007 9:56:01 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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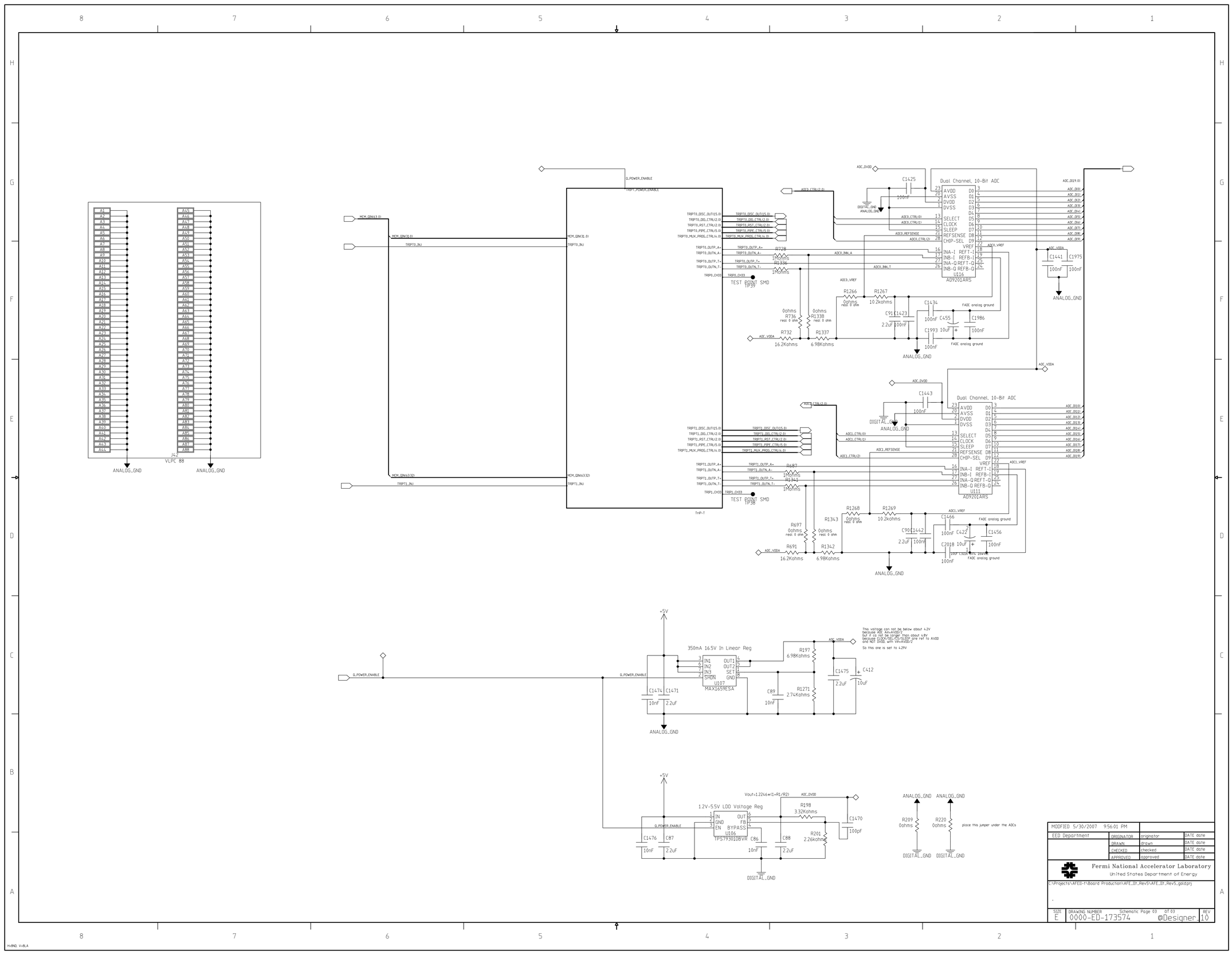
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H=8ND, V=4LA



MODIFIED 5/30/2007 9:56:01 PM

EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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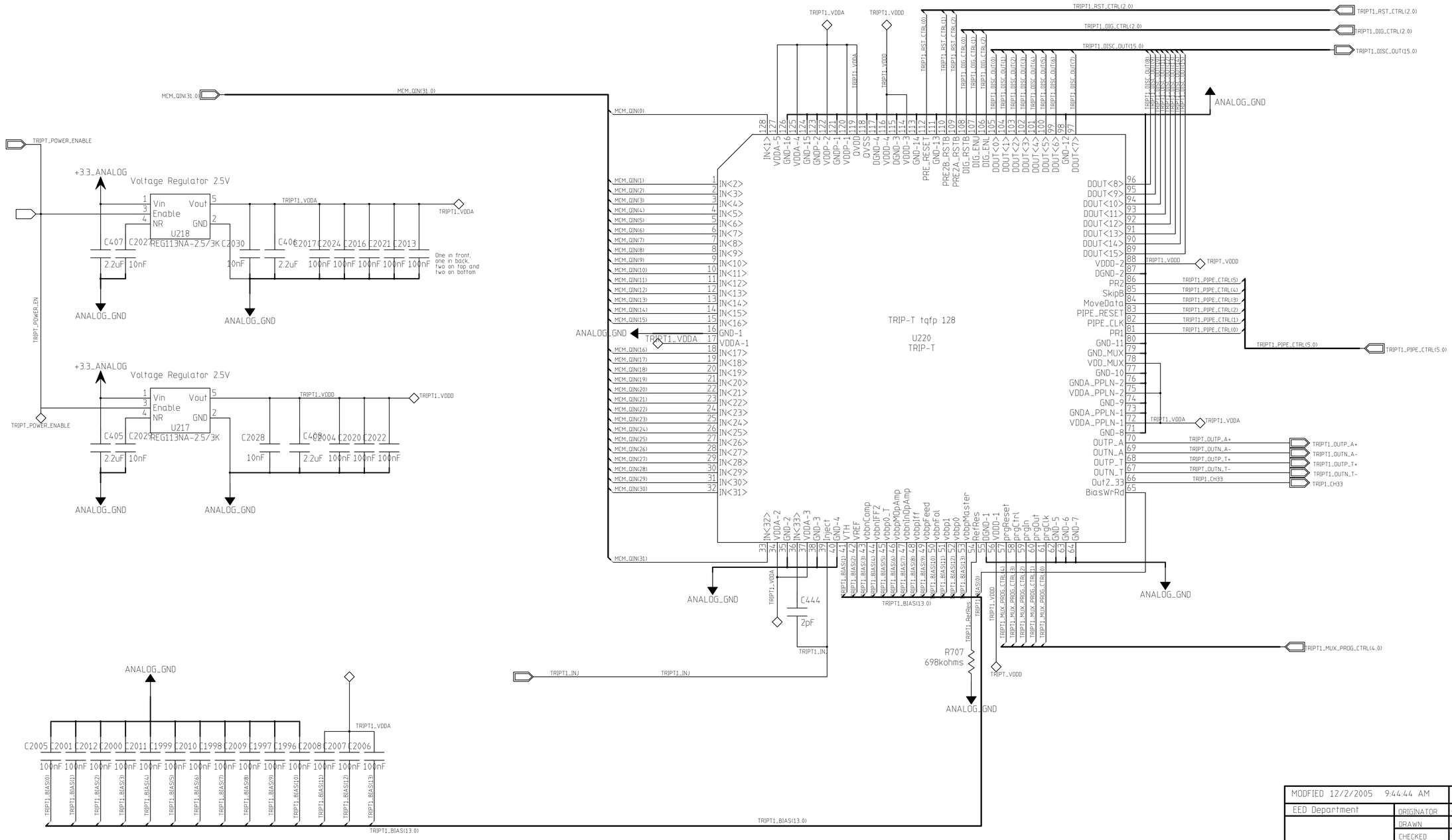
SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

H:\BND, V:\BLA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
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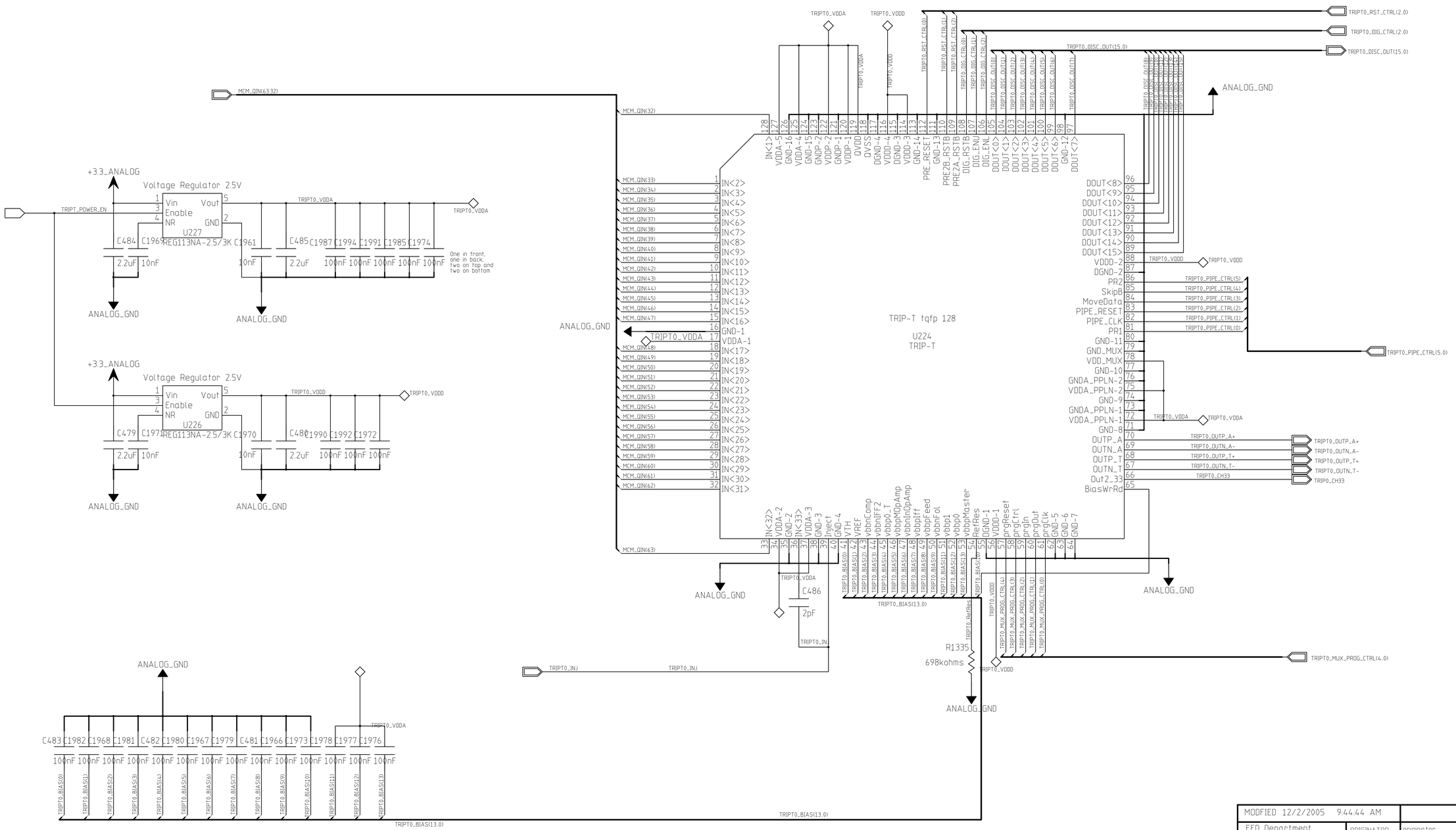
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

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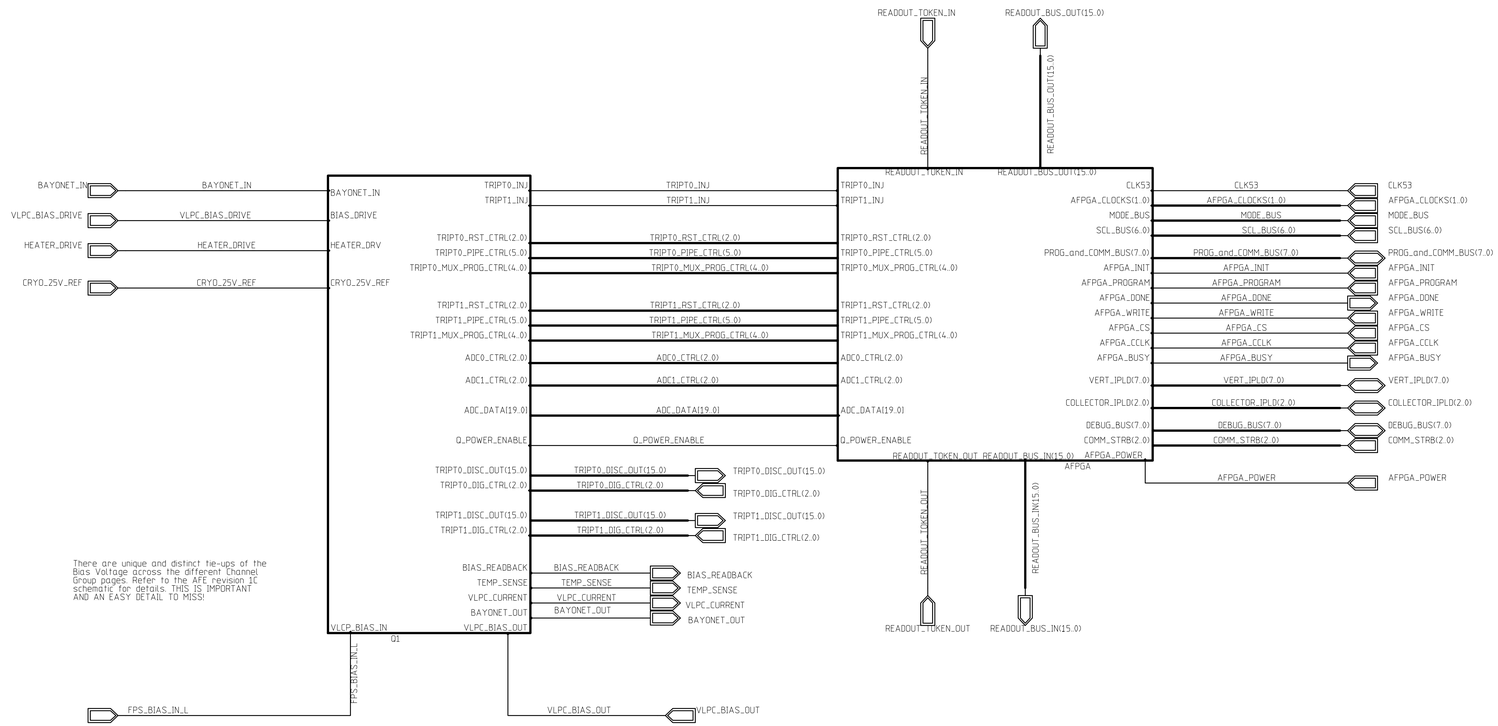

MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
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	CHECKED	checked	DATE date
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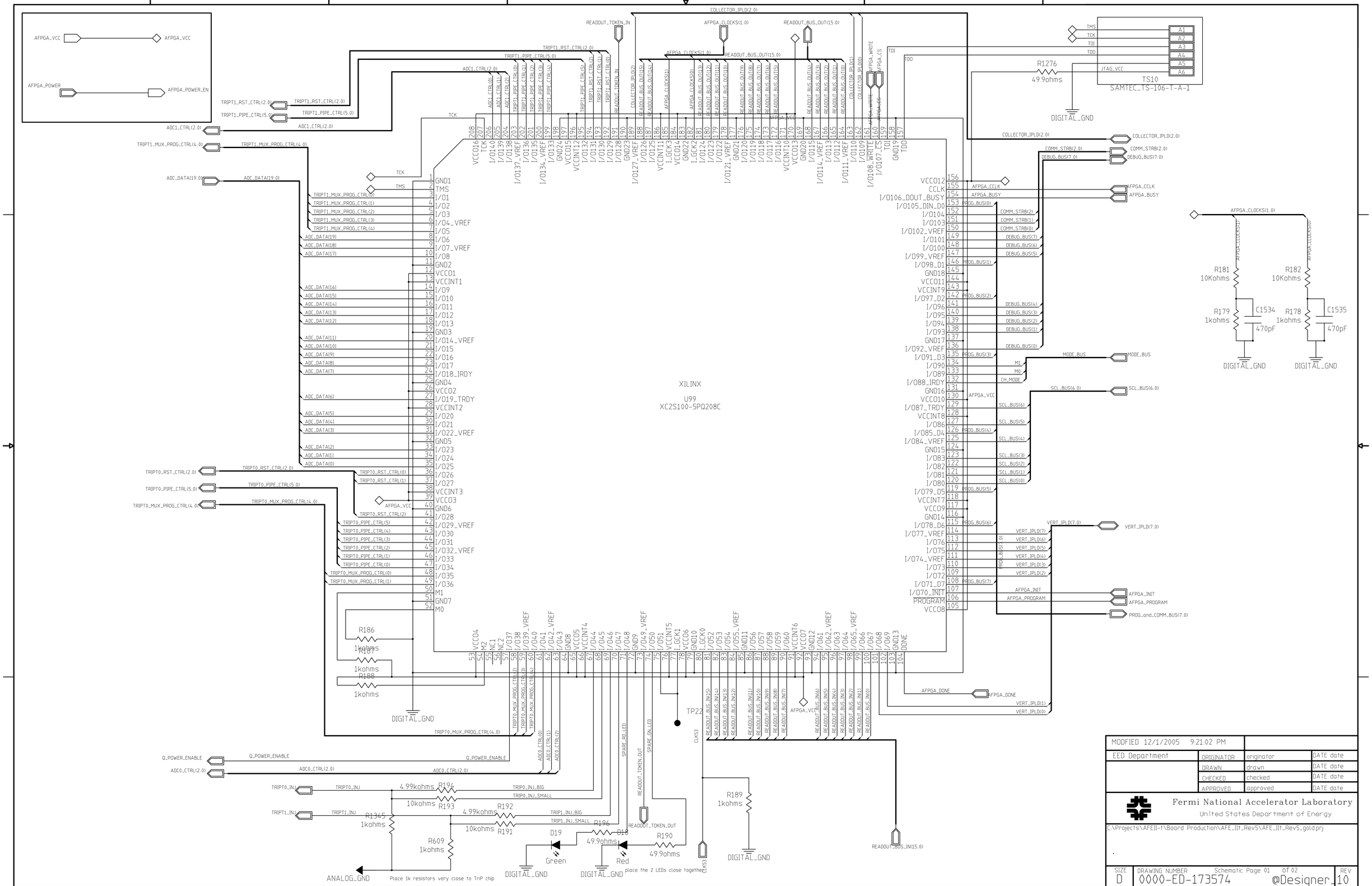
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/1/2005 9:21:02 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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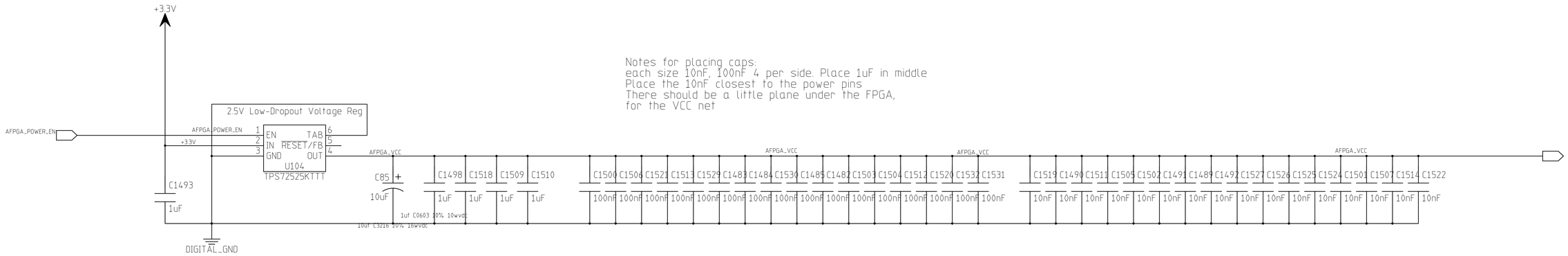
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer	10

H=8ND, V=4LA



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D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

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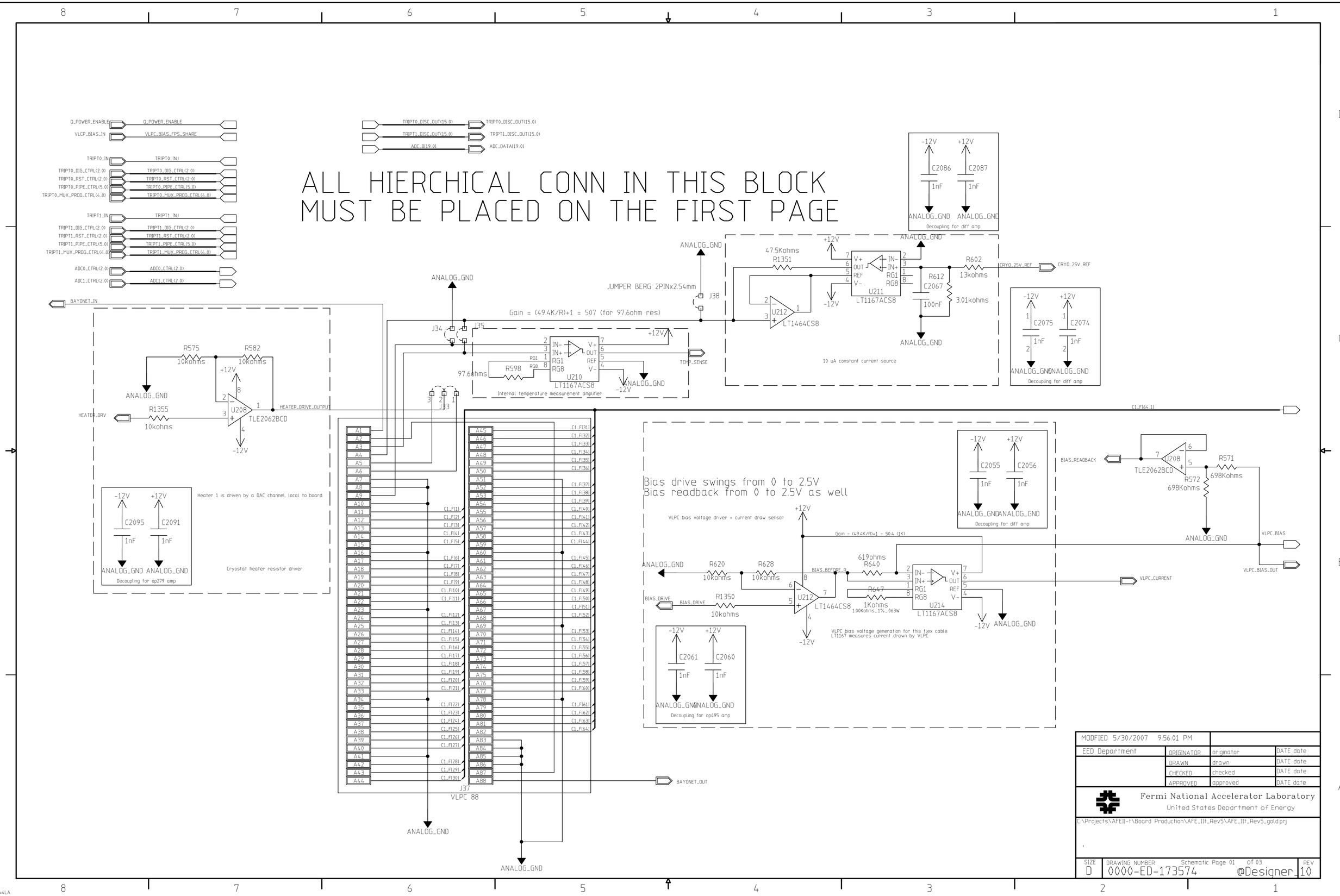
ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
VLCP_BIAS_FPS_SHARE
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
BAYONET_IN
ANALOG_GND
JUMPER BERG 2PINx2.54mm
J38
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
J34
J35
J33
R575
10kohms
R582
10kohms
R1355
10kohms
HEATER_DRV
U208
TLE2062BCD
HEATER_DRIVE_OUTPUT
Heater 1 is driven by a DAC channel, local to board.
C2095
C2091
1nF
Decoupling for op279 amp
Cryostat heater resistor driver
97.6ohms
R598
U210
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
47.5Kohms
R1351
U212
LT1464CS8
U211
LT1167ACS8
R612
C2067
100nF
R602
13kohms
3.01kohms
10 uA constant current source
C2086
C2087
Decoupling for diff amp
CRYO_25V_REF
C2075
C2074
C1_FI64_1
J37
VLPC 88
BAYONET_OUT
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R620
10kohms
R628
10kohms
R1350
10kohms
BIAS_DRIVE
BIAS_BEFORE_R
619ohms
R640
R647
1Kohms
1.00Kohms_1%_063W
U214
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
C2055
C2056
C2061
C2060
Decoupling for op495 amp
BIAS_READBACK
R571
698Kohms
R572
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
VLPC_CURRENT
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Schematic Page 01 of 03
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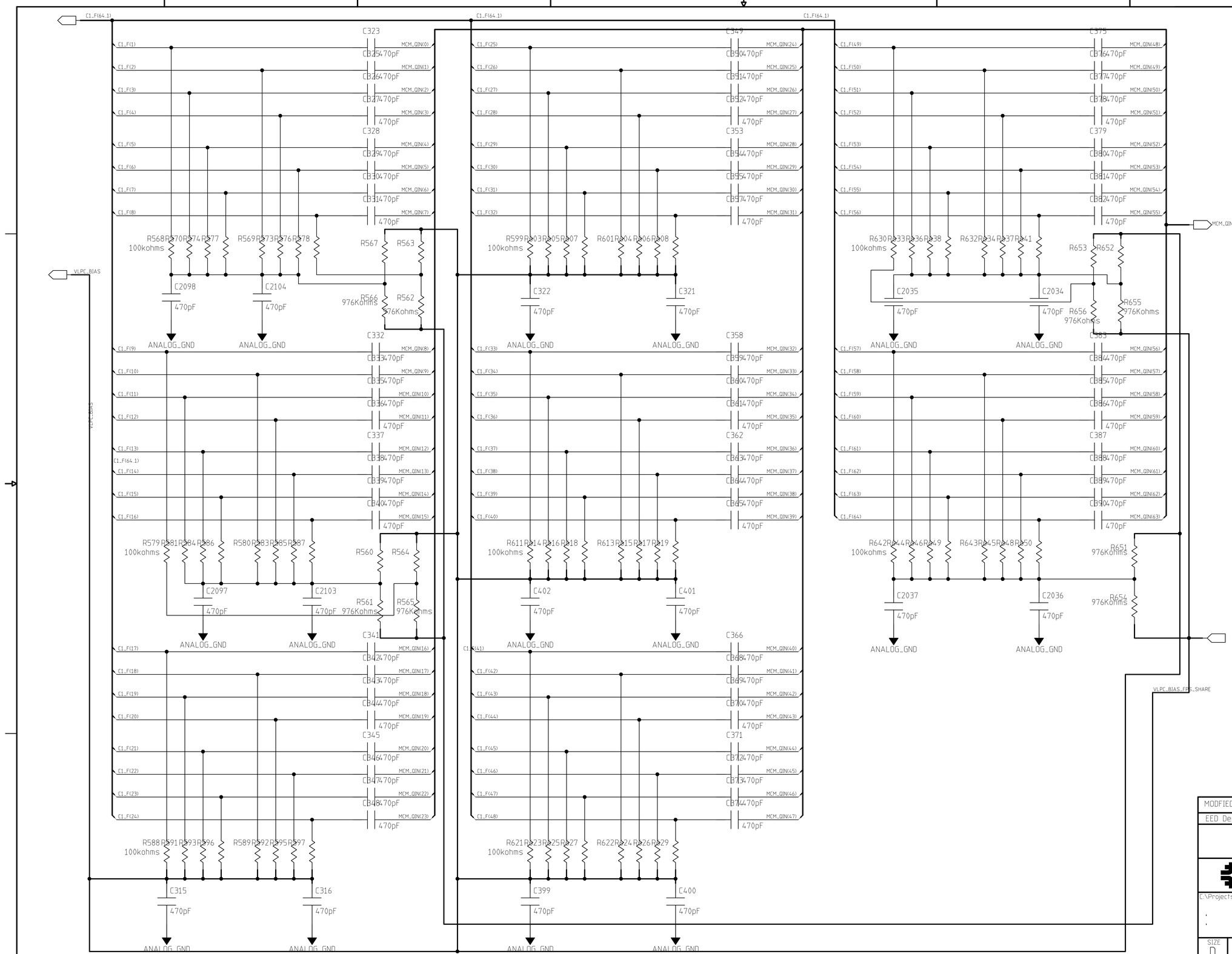
H=8ND, V=4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
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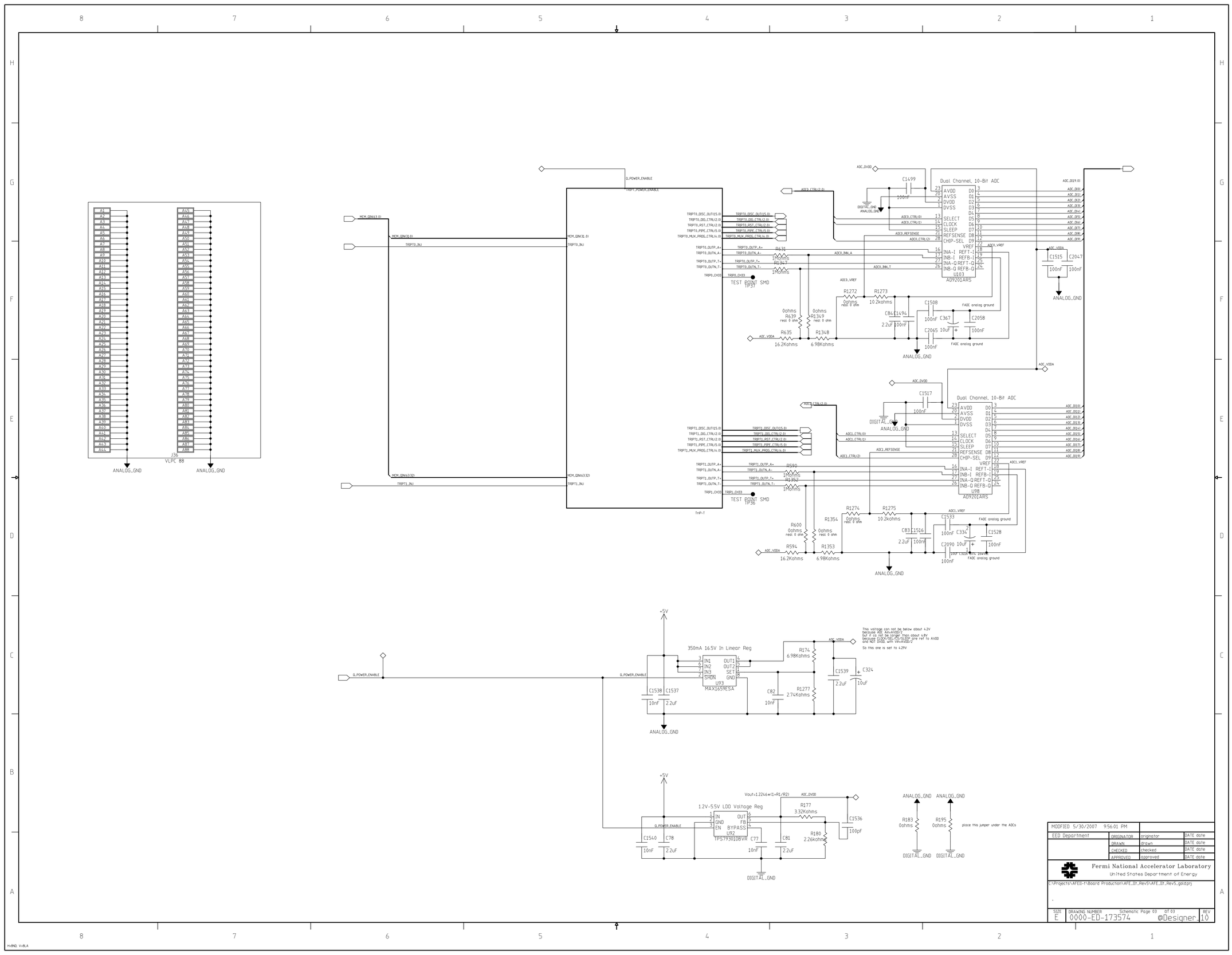
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H:8ND, V:4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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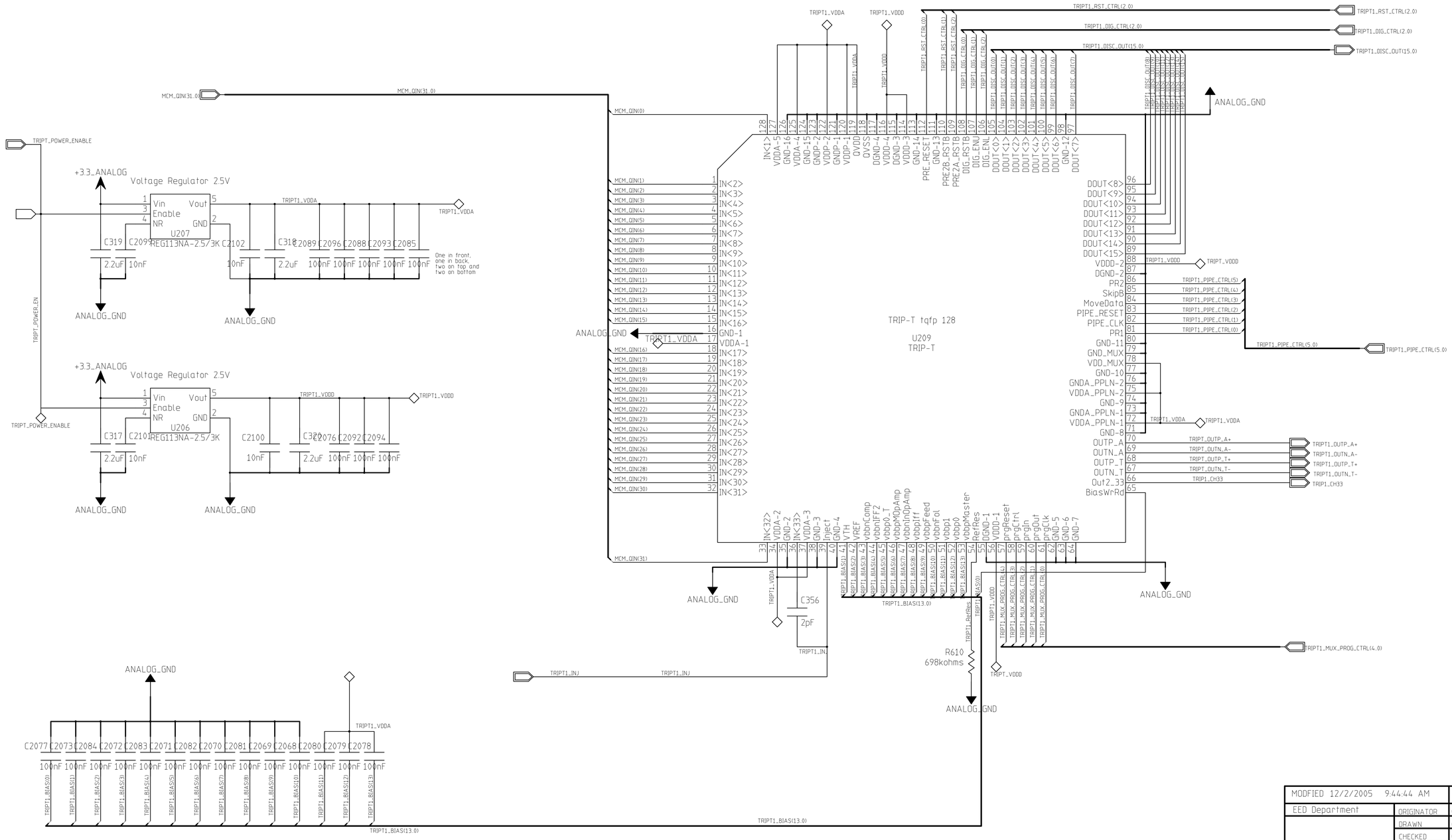
SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

H:\BND, V:\BLA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
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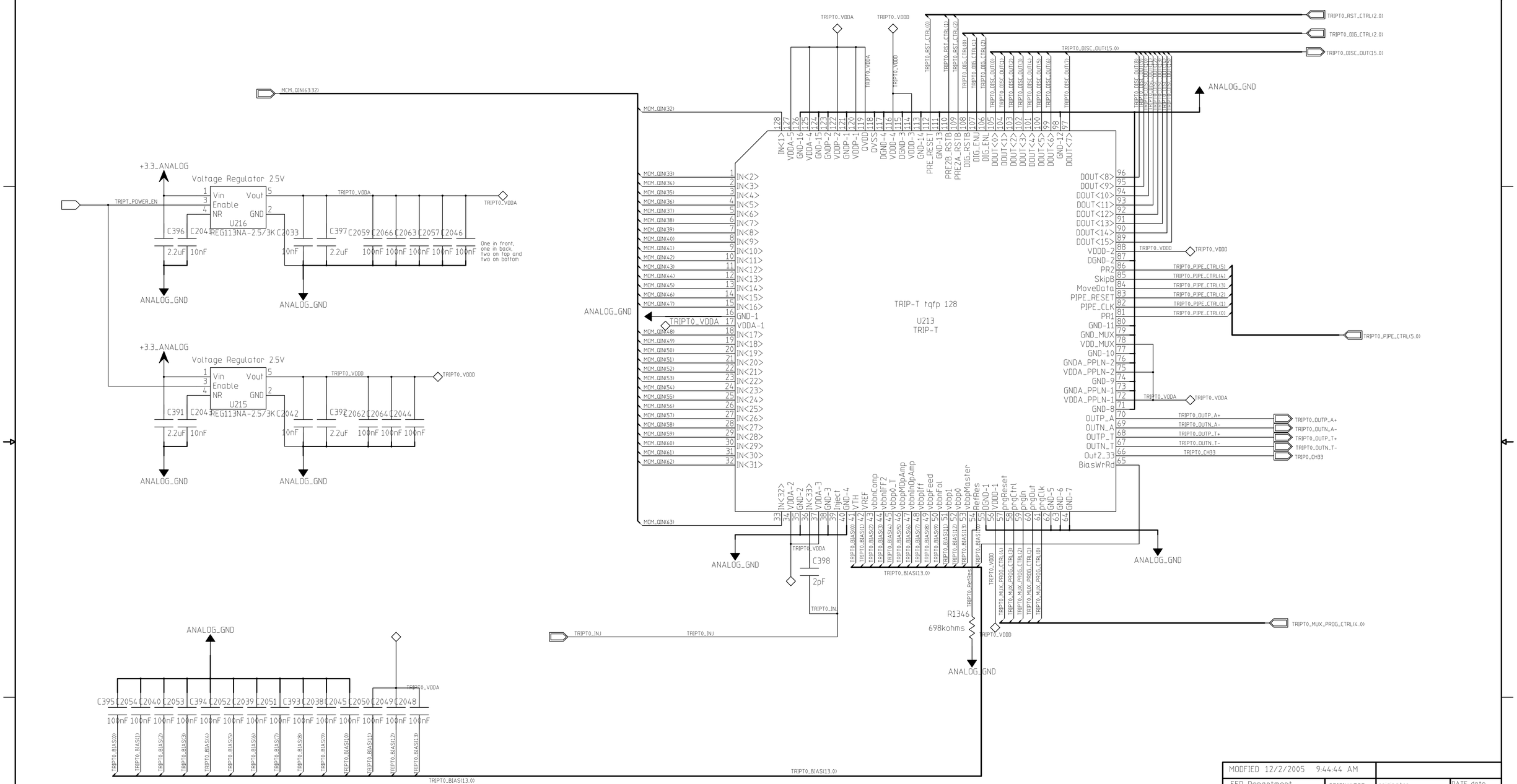
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

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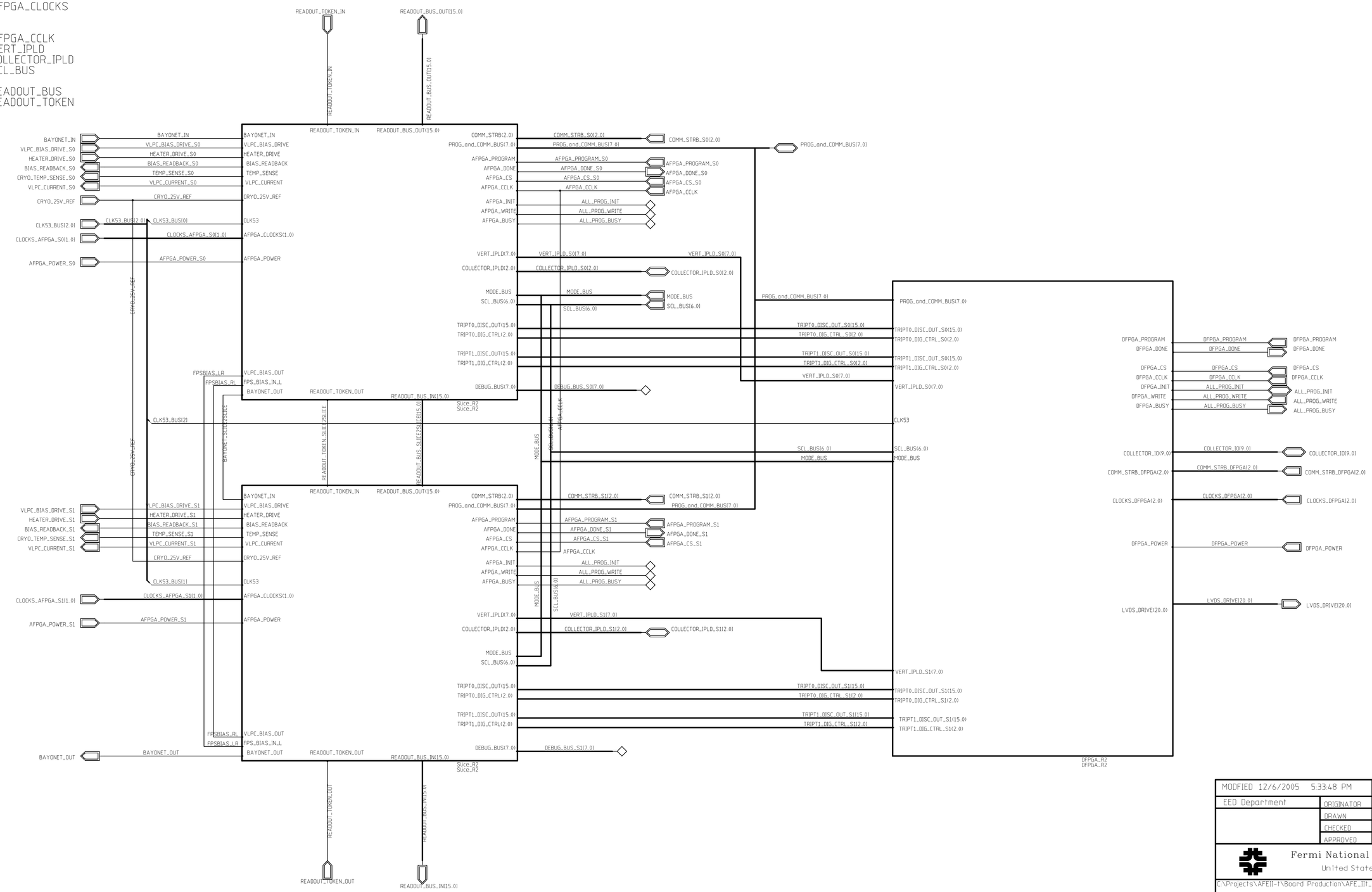
HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



MODIFIED 12/6/2005 5:33:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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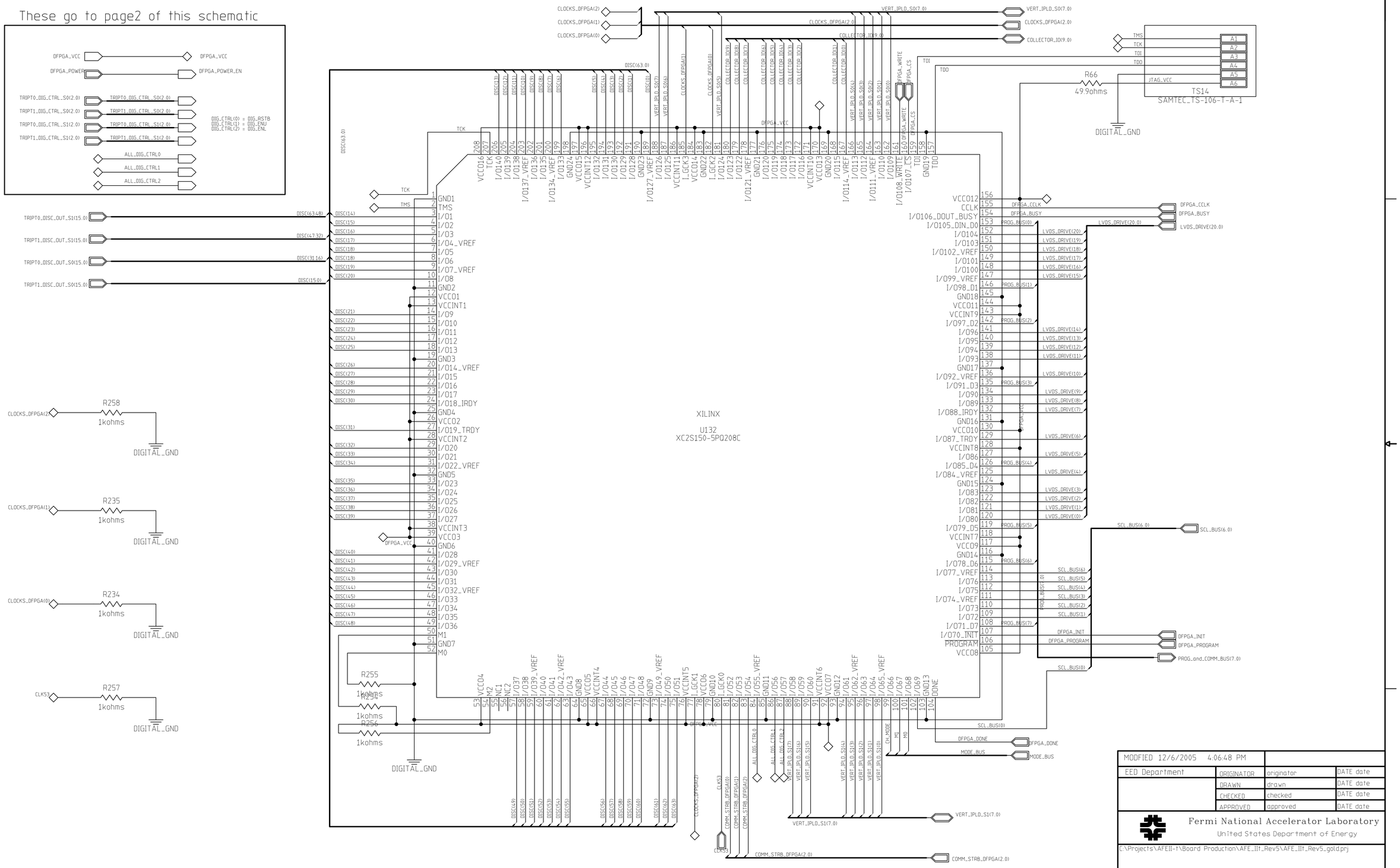
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	10

H:8ND, V:4LA



MODIFIED 12/6/2005 4:06:48 PM

EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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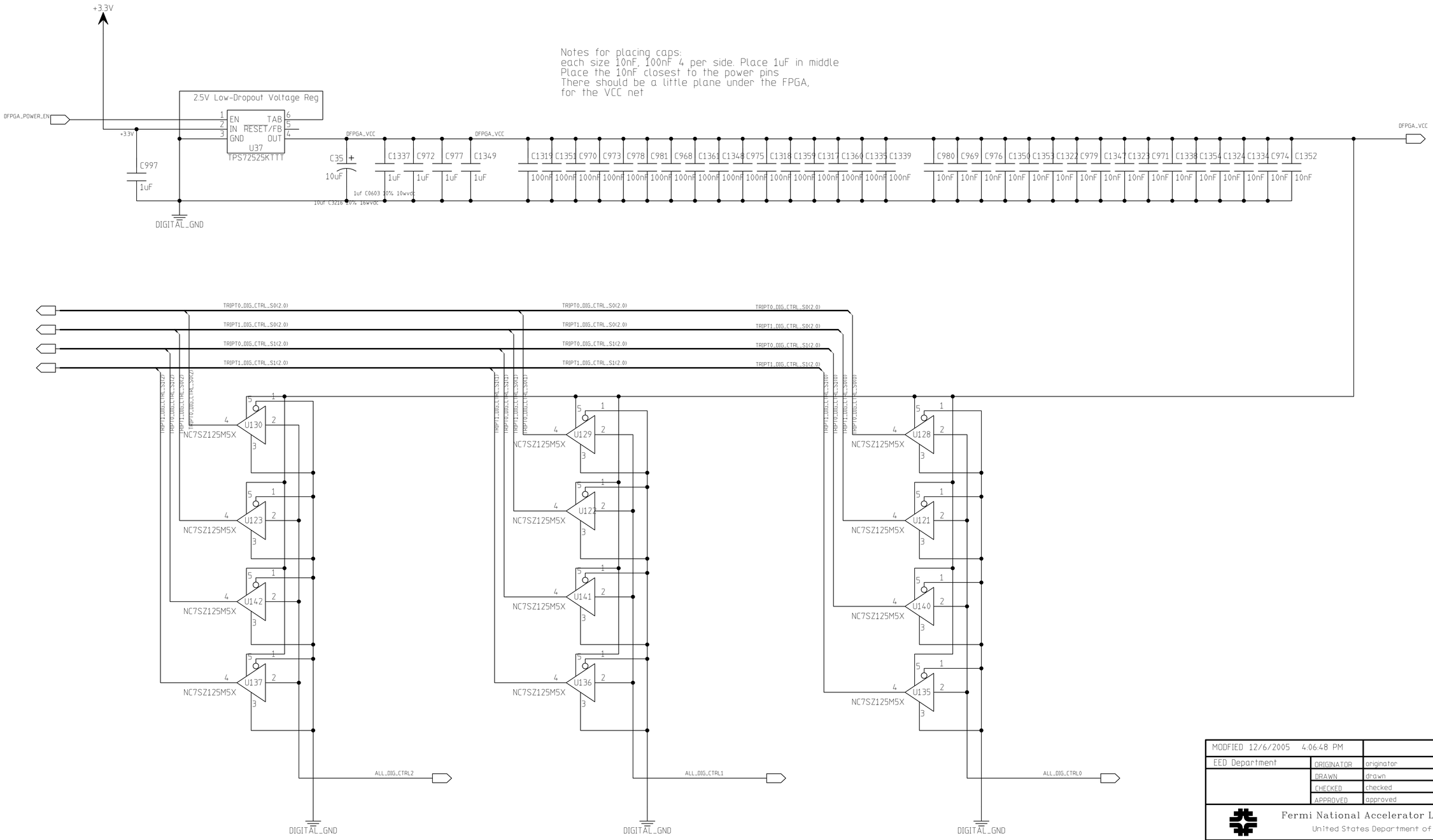
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_1	10

H:8ND, V:4LA



MODIFIED 12/6/2005 4:06:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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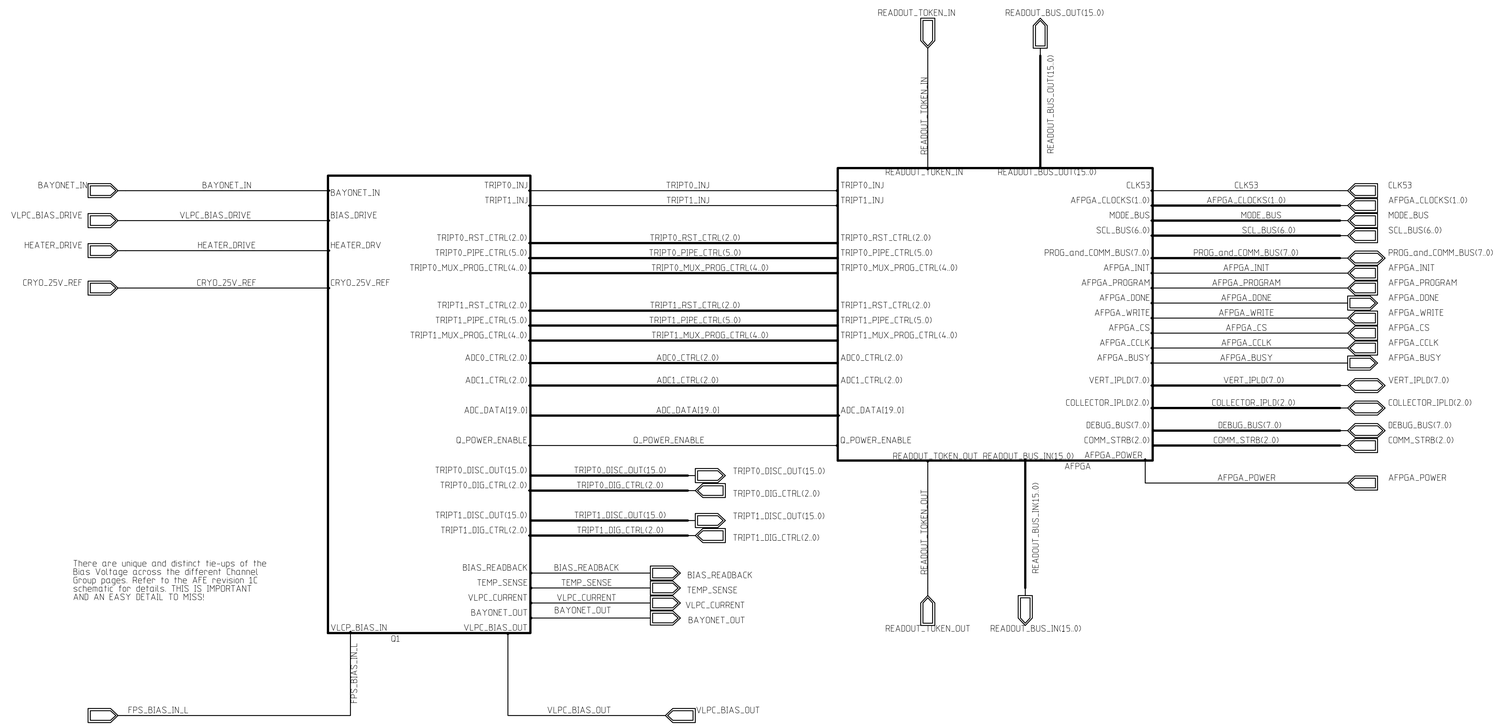
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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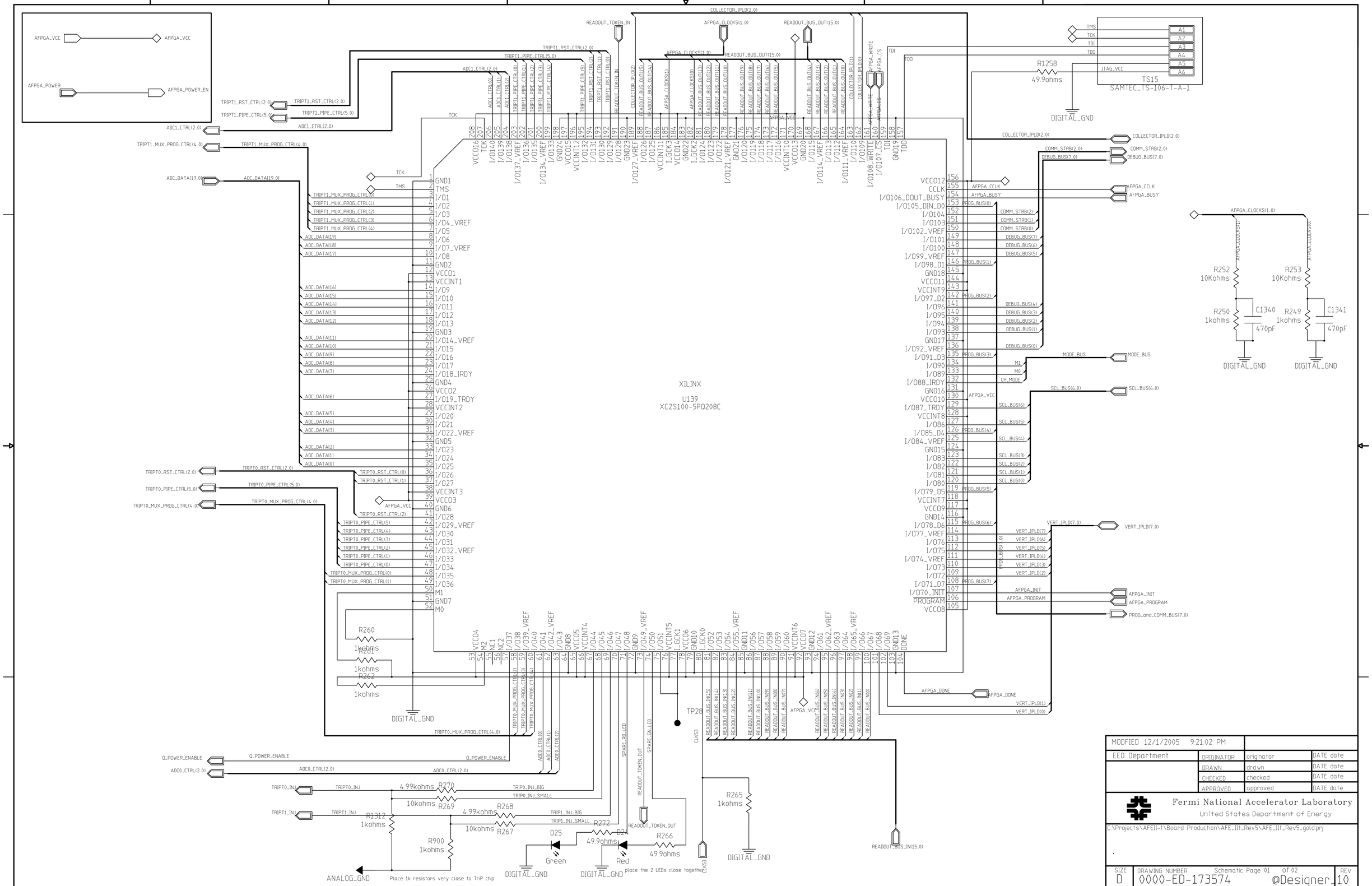
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/1/2005 9:21:02 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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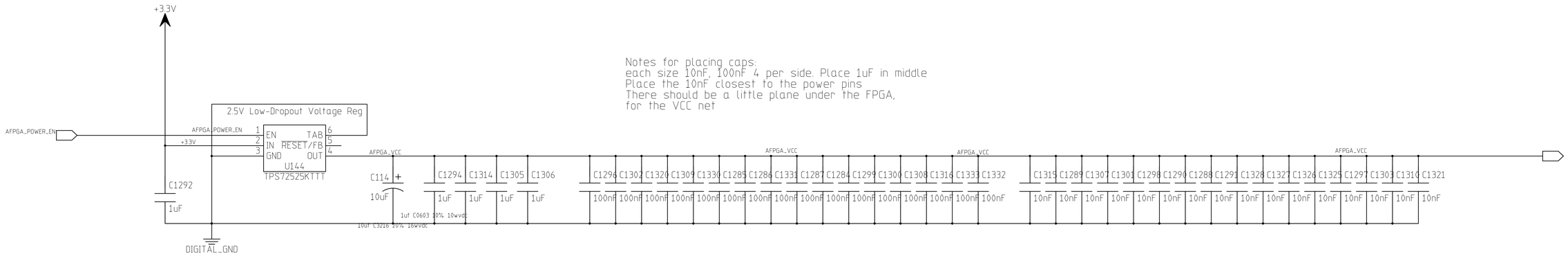
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer	10

H=8ND, V=4LA



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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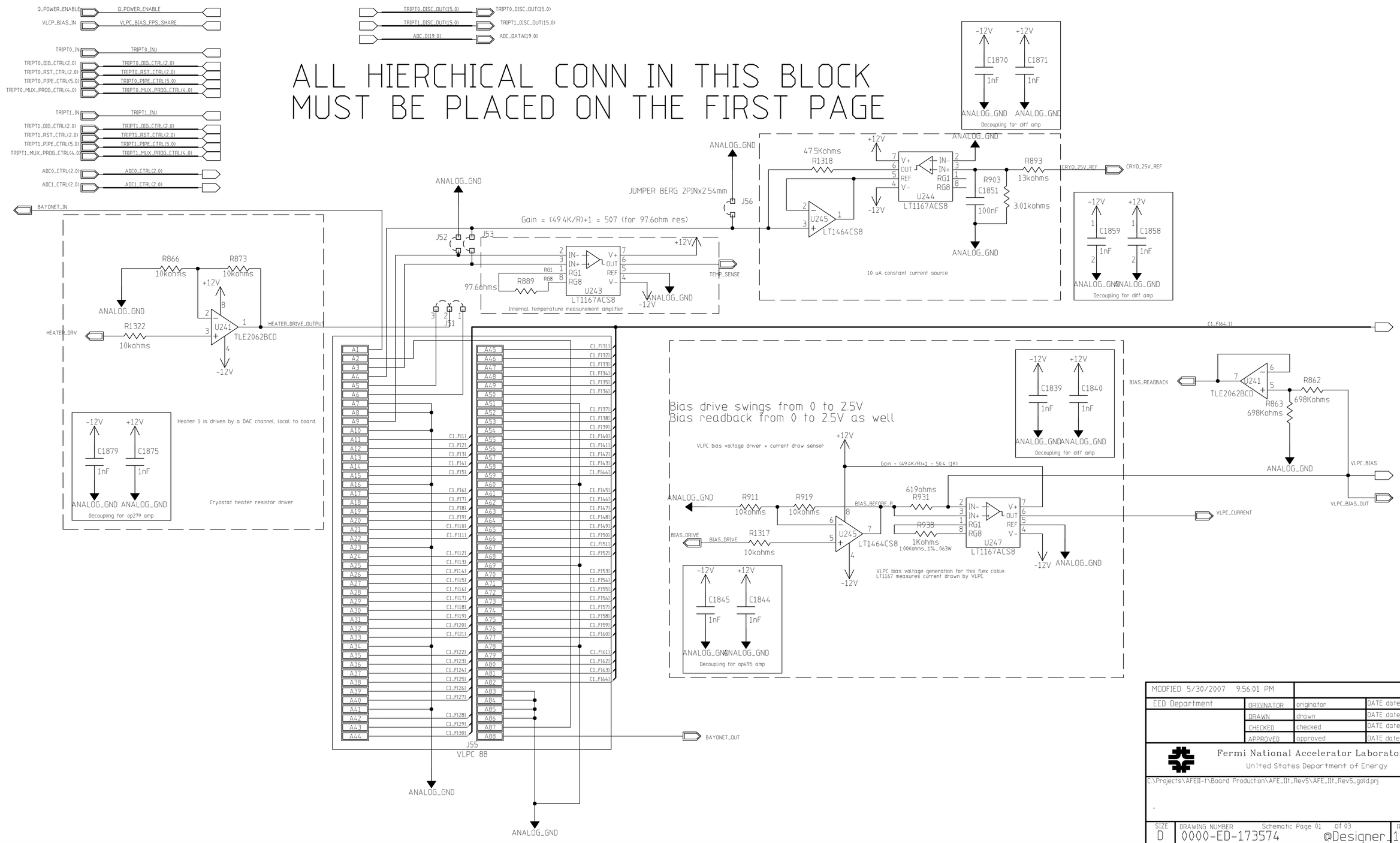
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H=8ND, V=4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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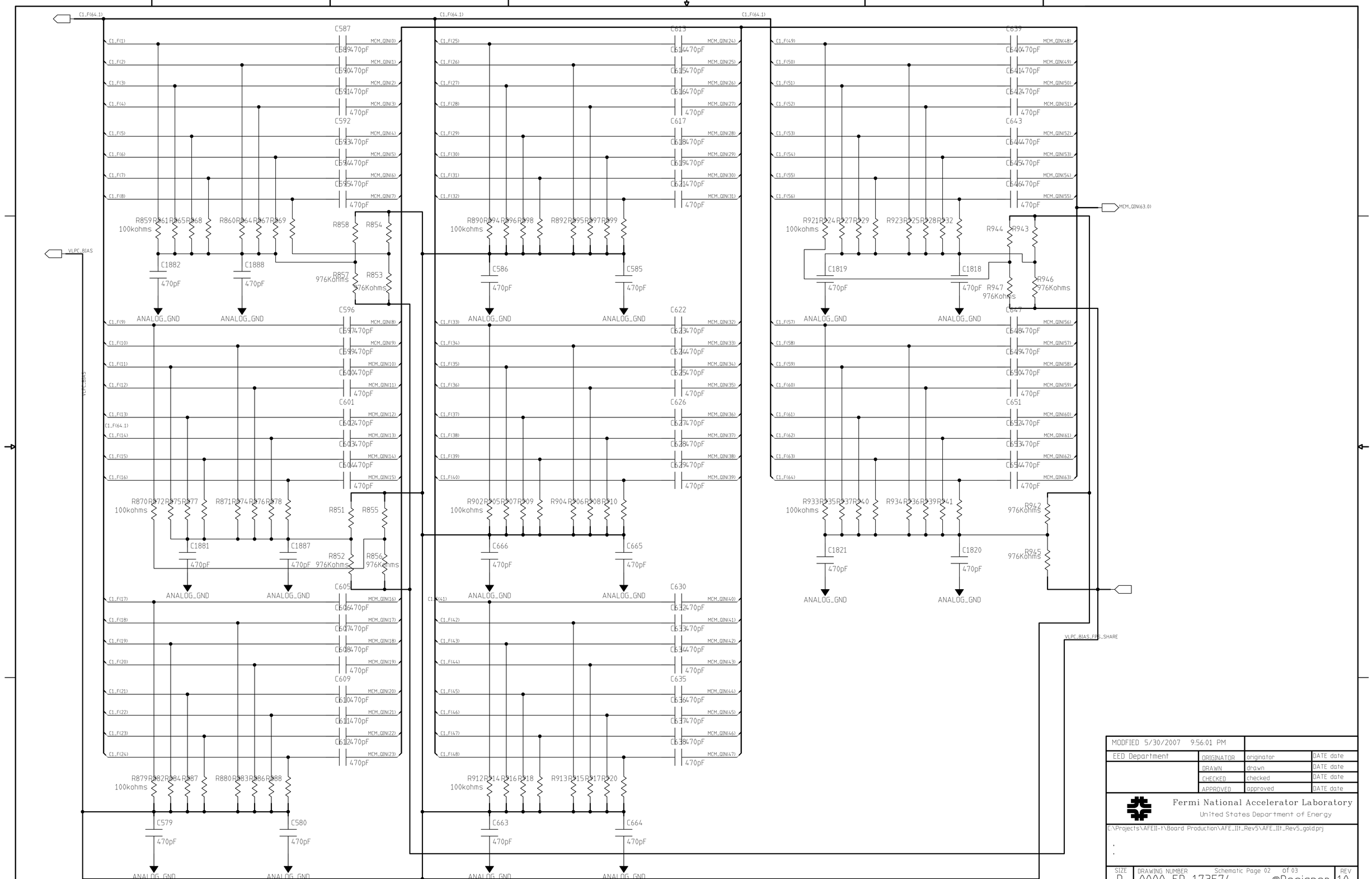
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer_1	10

H:8ND, V:4LA



MODIFIED 5/30/2007 9:56:01 PM

EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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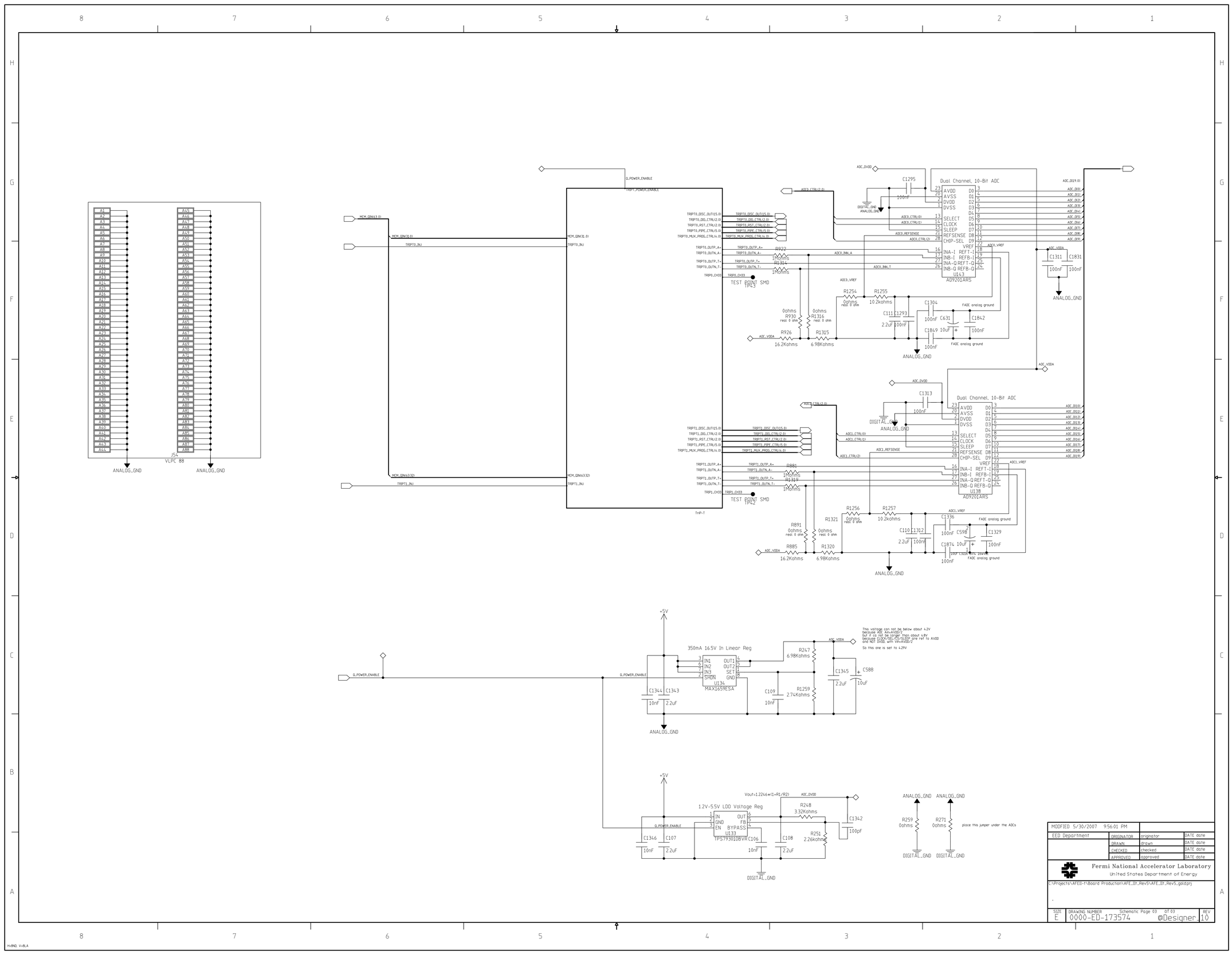
H=8ND, V=4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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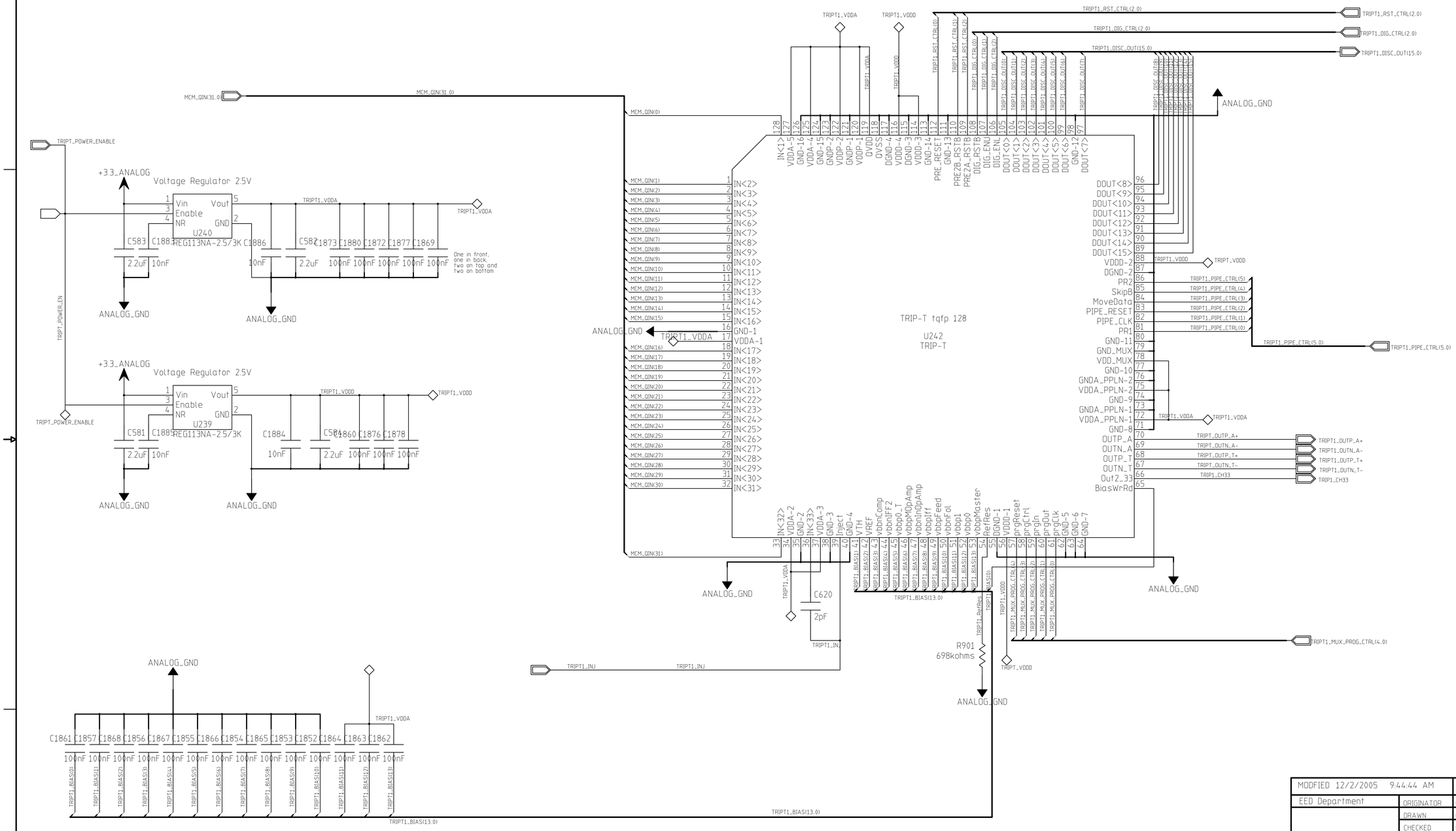
SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

H:\BND, V:\BLA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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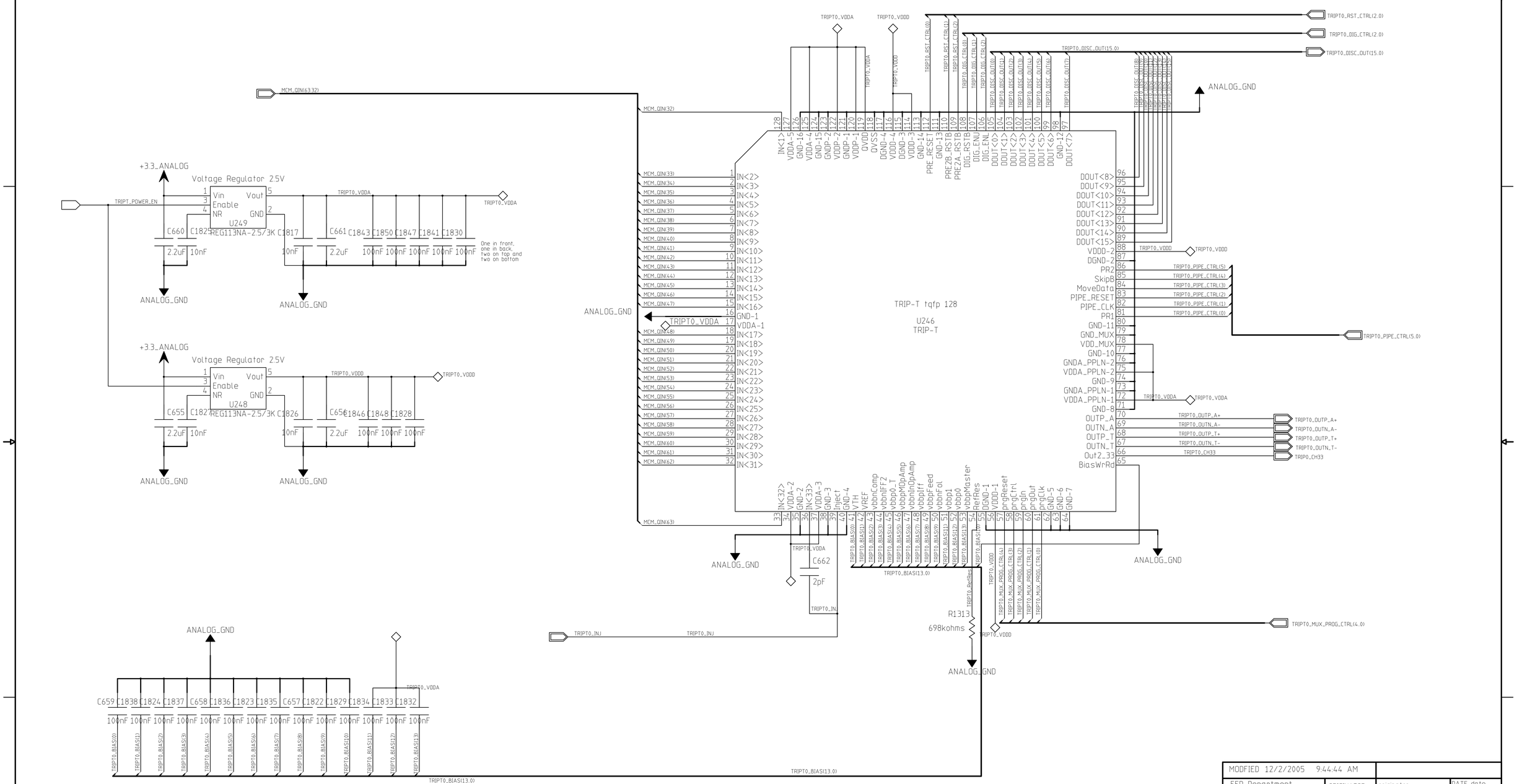
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H:8ND, V:4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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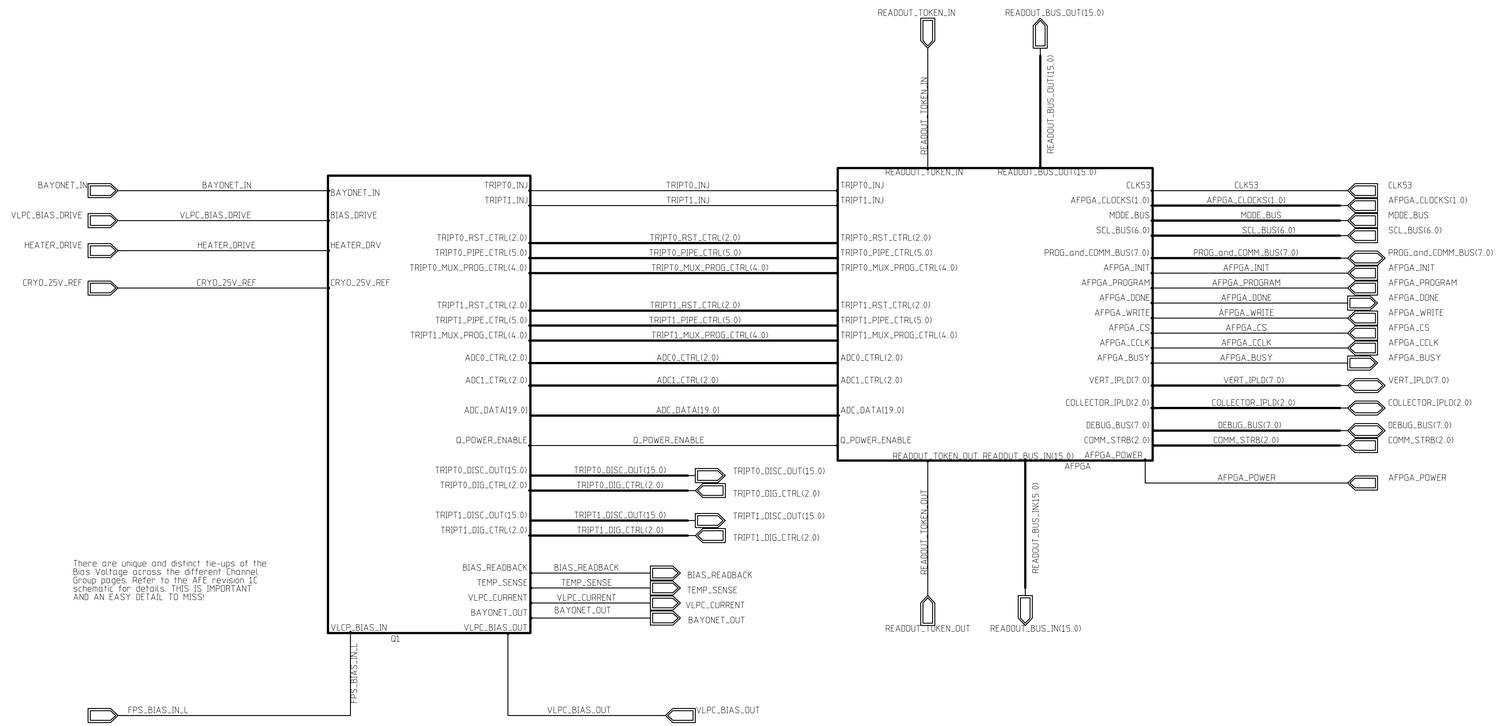
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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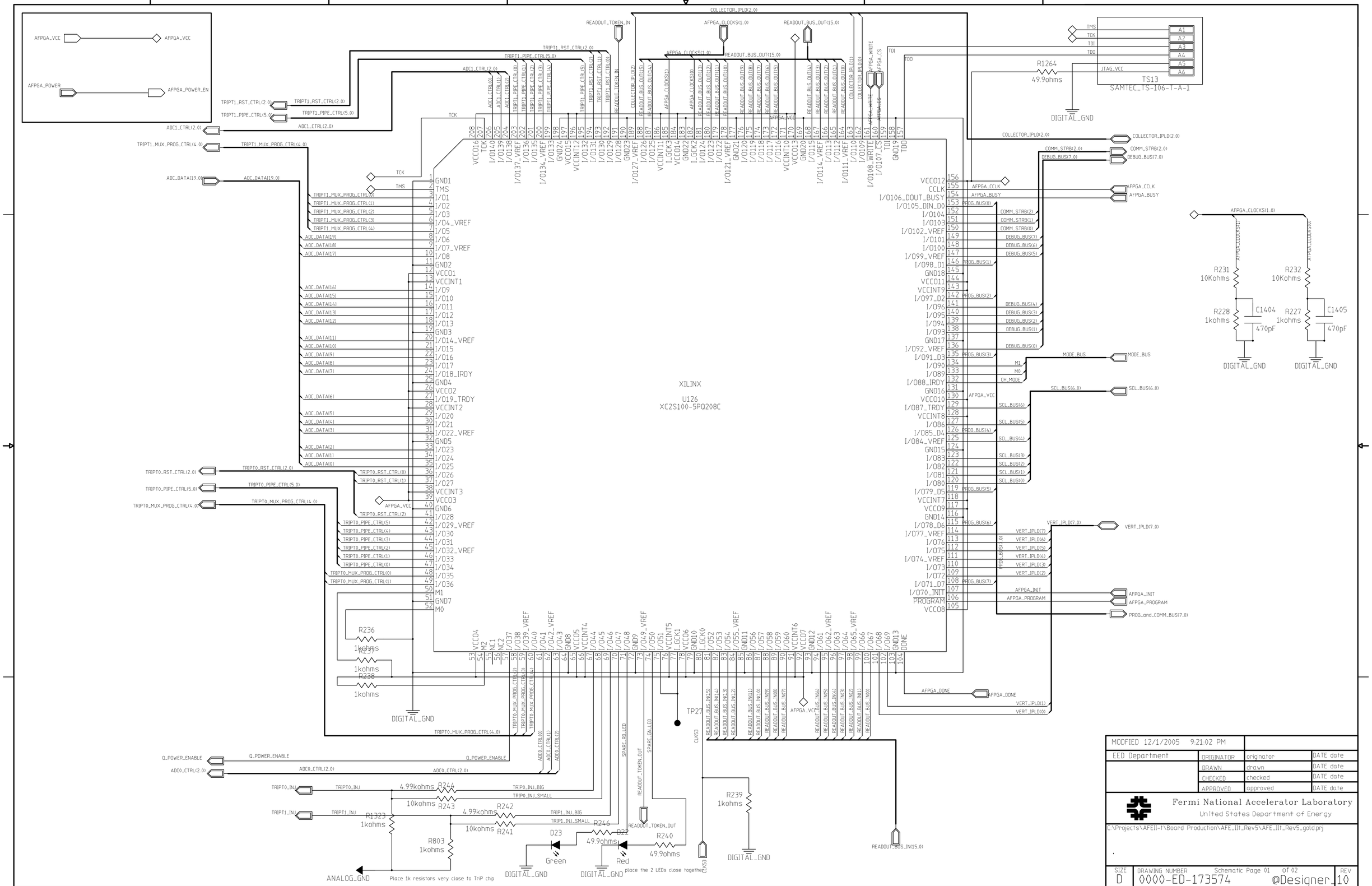
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA


XILINX
U126
XC2S100-5PQ208C
TS13
SAMTEC_TS-106-T-A-1
R1264
49.9ohms
DIGITAL_GND
R231
10Kohms
R232
10Kohms
R228
1kohms
R227
1kohms
C1404
C1405
470pF
R236
R237
R238
1kohms
R244
4.99kohms
R243
10kohms
R242
4.99kohms
R241
10kohms
R1323
1kohms
R803
1kohms
R246
49.9ohms
R240
49.9ohms
R239
1kohms
D23
Green
D22
Red
TP27
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
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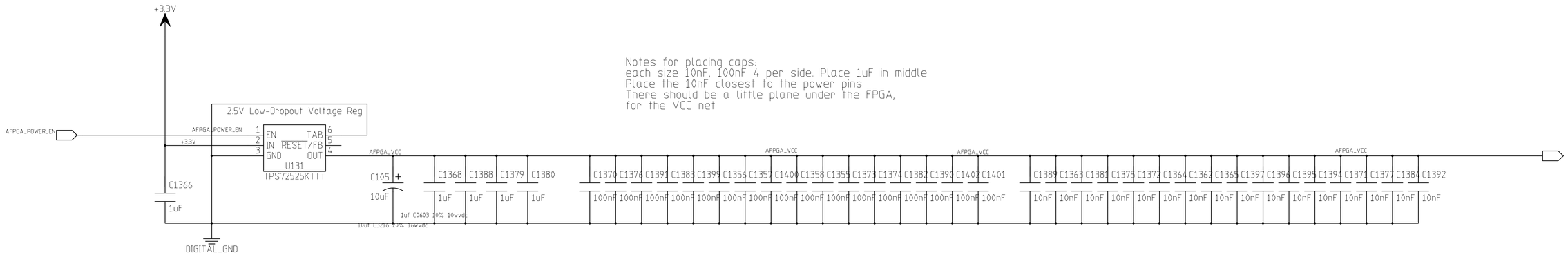
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 02
@Designer.10
REV
H=8ND, V=4LA



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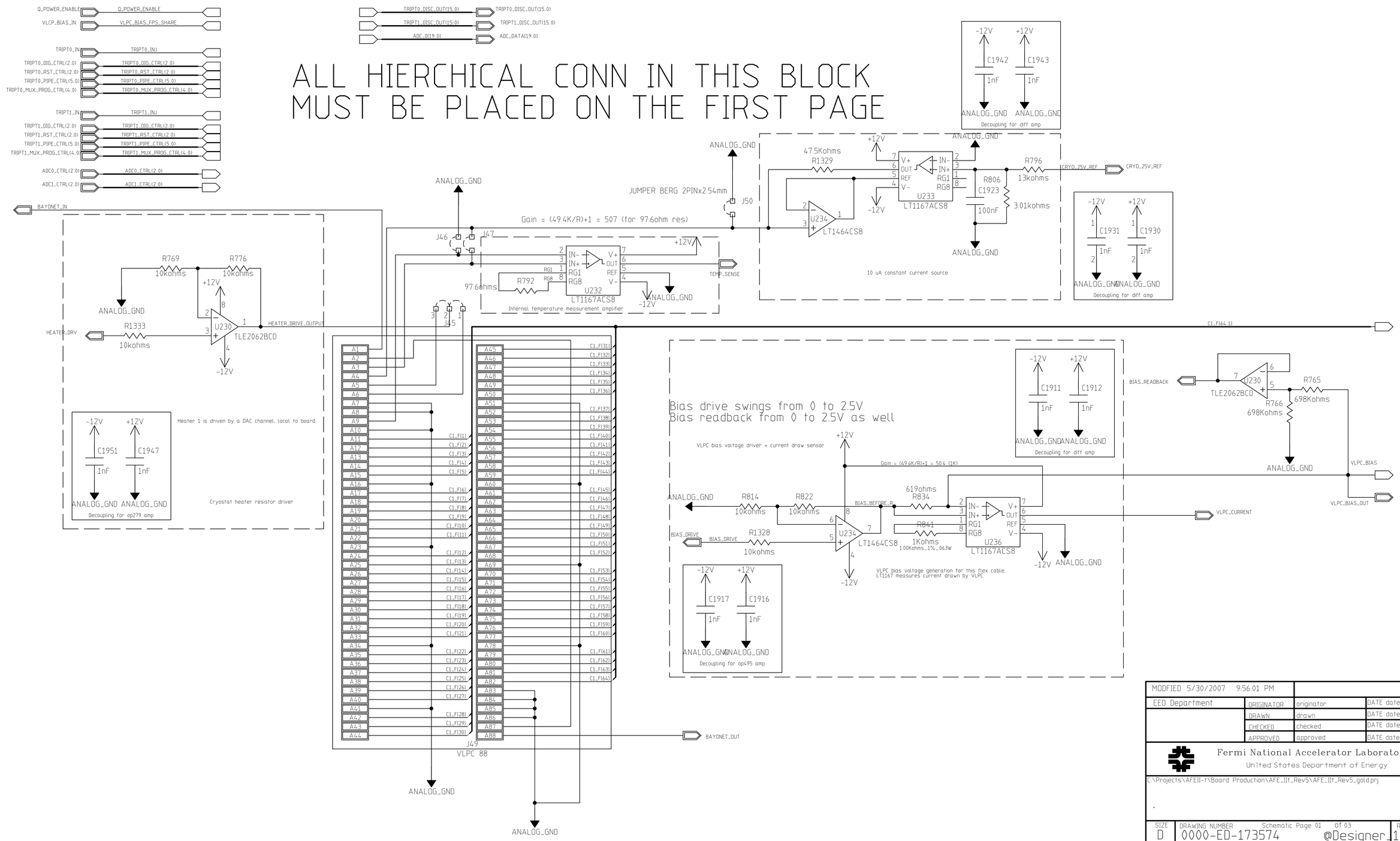
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H=8ND, V=4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
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	CHECKED	checked	DATE date
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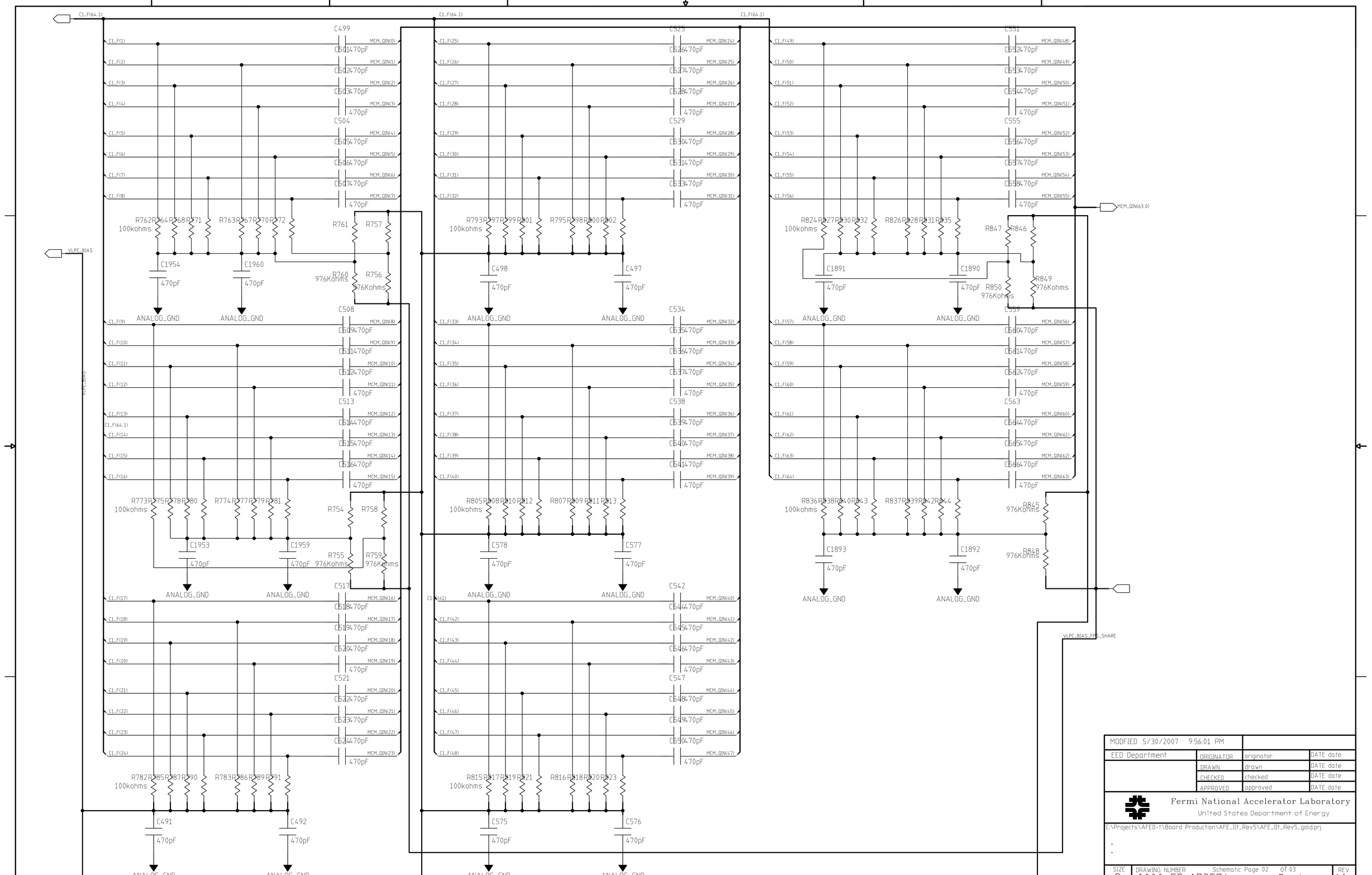
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer_1	10

H:8ND, V:4LA


C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
470pF
100kohms
976Kohms
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ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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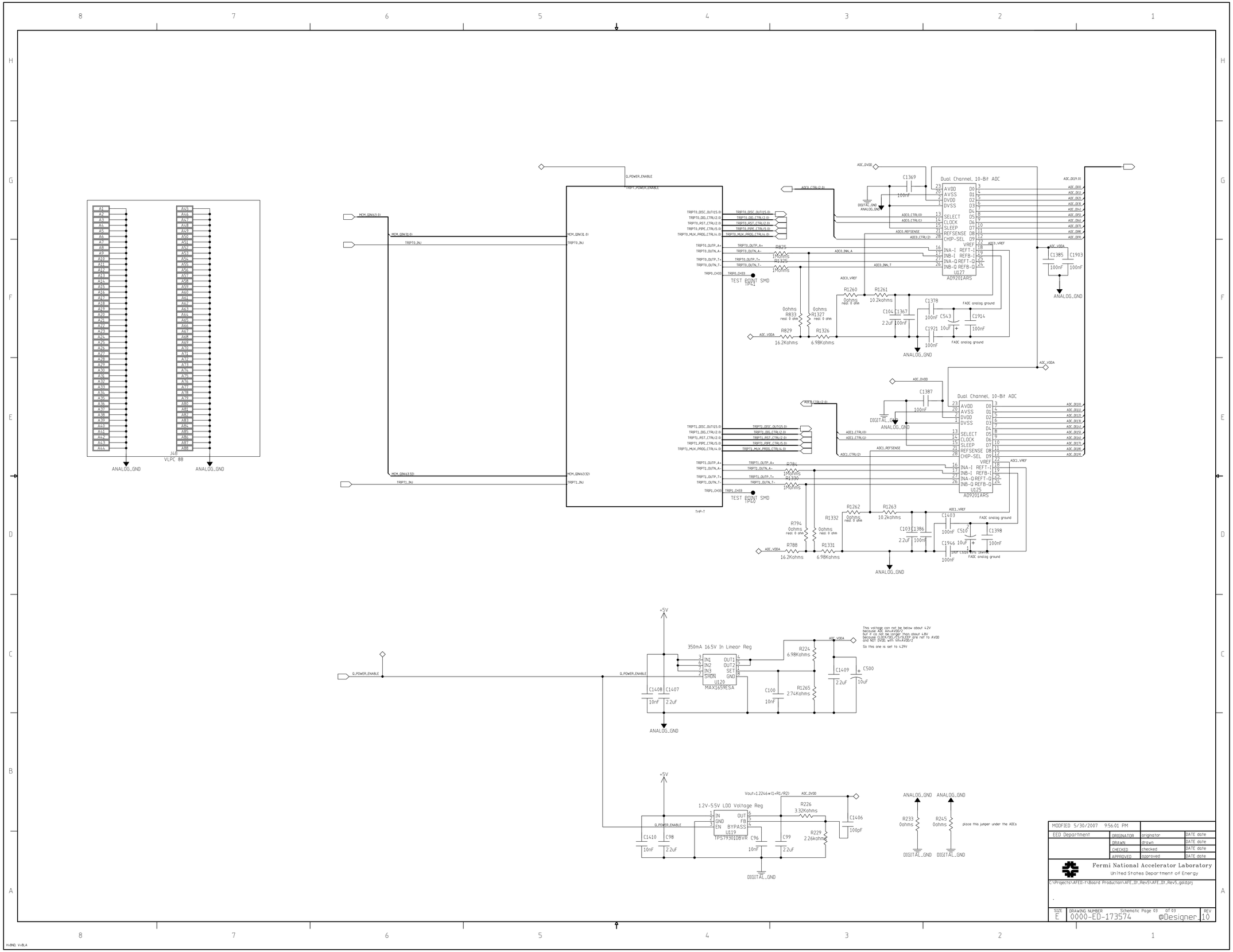
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H=8ND, V=4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
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SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

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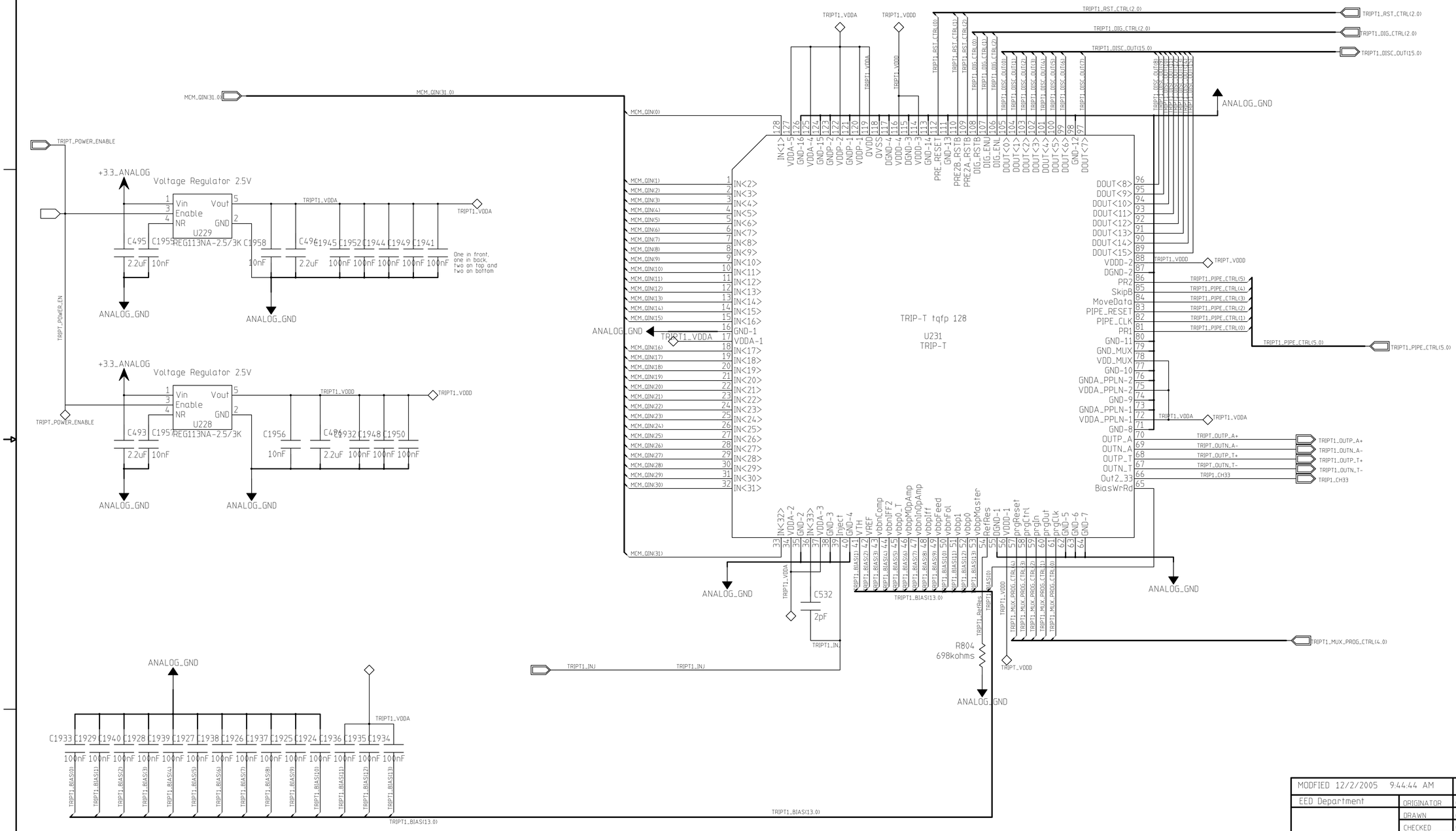

MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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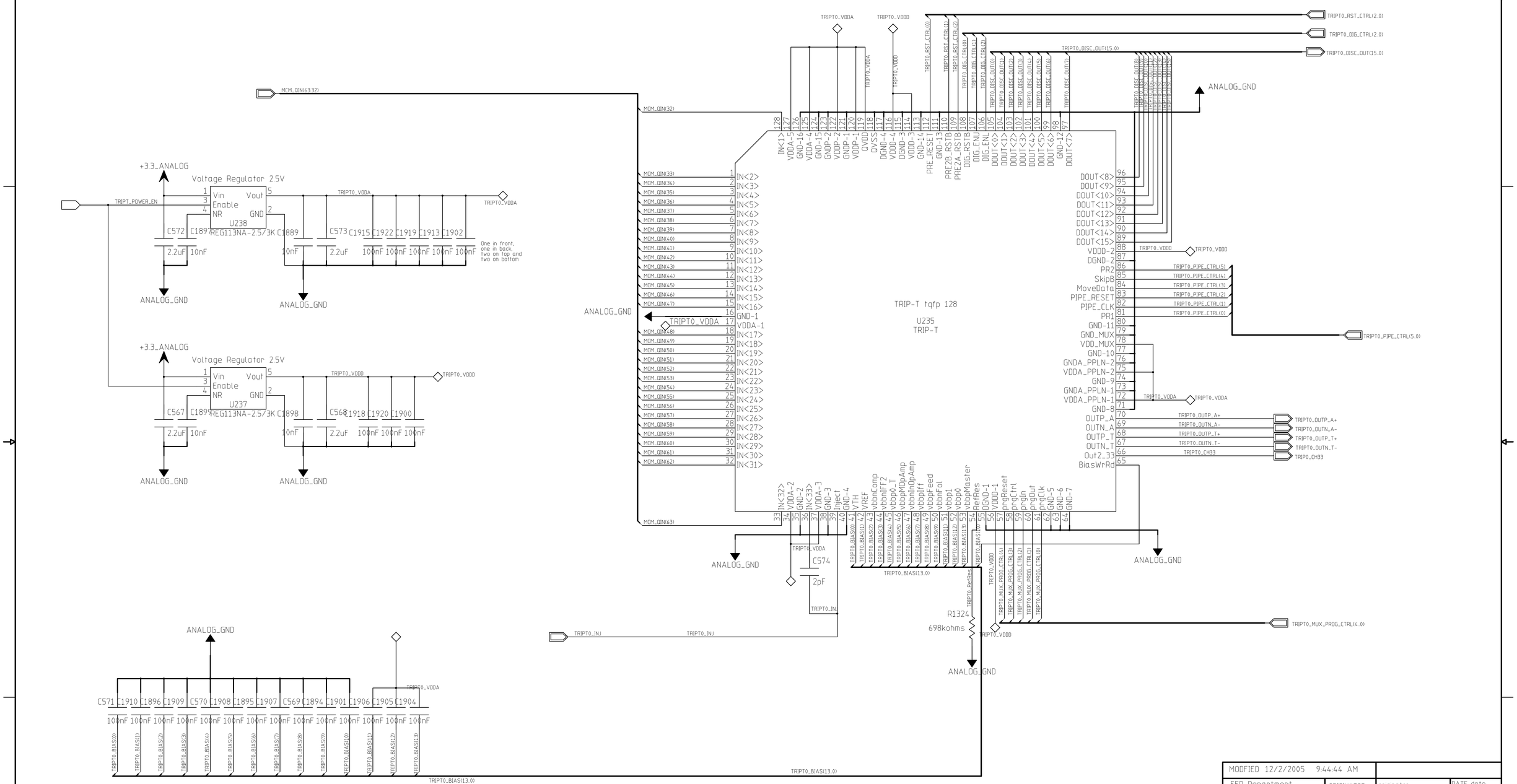
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
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	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

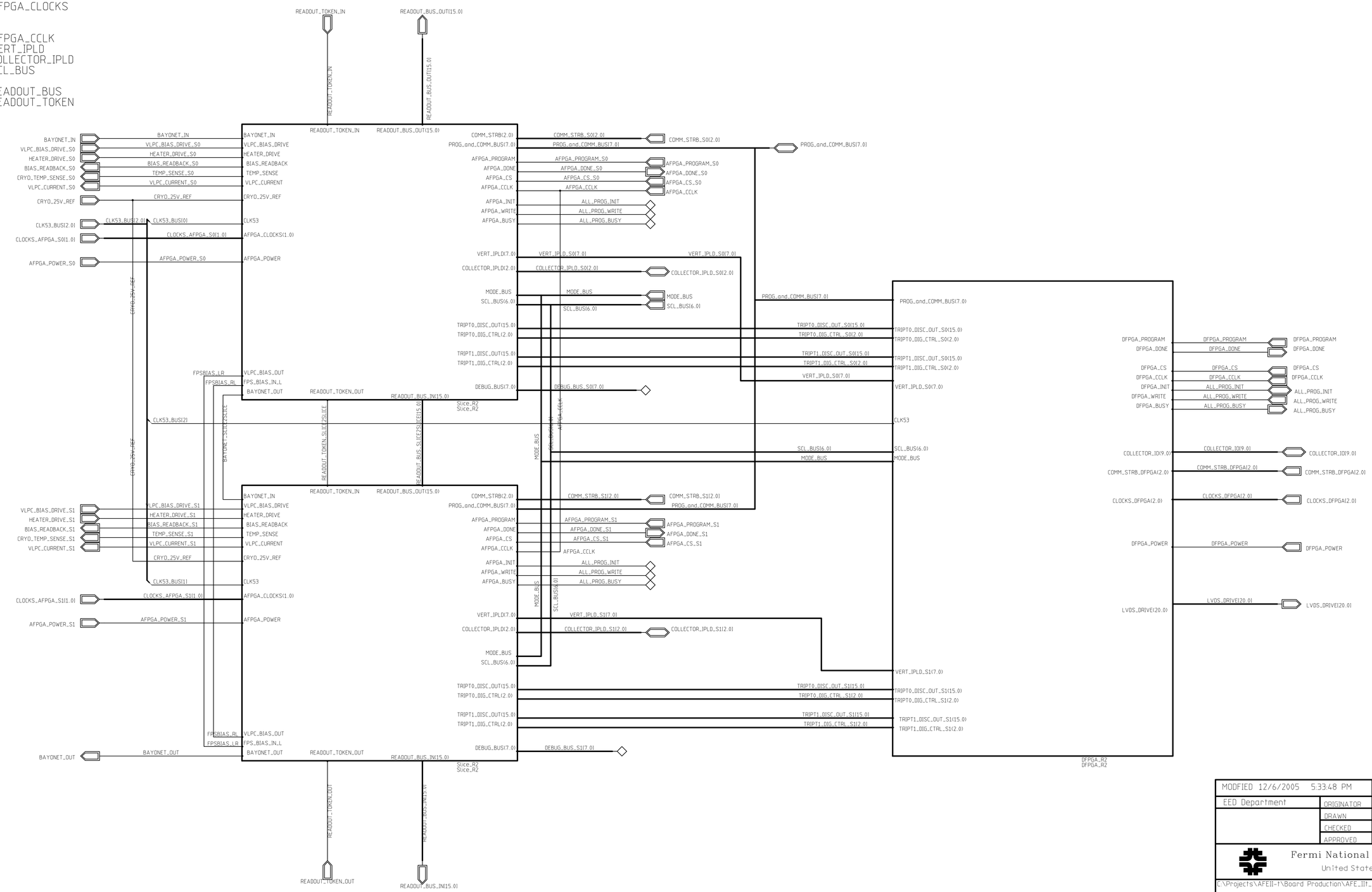
H:8ND, V:4LA

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



MODIFIED 12/6/2005 5:33:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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C:\Projects\AFEII-1\Board Production\AFE_II1_Rev5\AFE_II1_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	10

H:8ND, V:4LA

These go to page2 of this schematic

DFPGA_VCC → DFPGA_VCC
DFPGA_POWER → DFPGA_POWER_EN
TRIPT0_DIG_CTRL_S0(2.0) → TRIPT0_DIG_CTRL_S0(2.0)
TRIPT1_DIG_CTRL_S0(2.0) → TRIPT1_DIG_CTRL_S0(2.0)
TRIPT0_DIG_CTRL_S1(2.0) → TRIPT0_DIG_CTRL_S1(2.0)
TRIPT1_DIG_CTRL_S1(2.0) → TRIPT1_DIG_CTRL_S1(2.0)
DIG_CTRL(0) = DIG_RSTB
DIG_CTRL(1) = DIG_ENU
DIG_CTRL(2) = DIG_ENL
ALL_DIG_CTRL0
ALL_DIG_CTRL1
ALL_DIG_CTRL2

TRIPT0_DISC_OUT_S1(15.0) — DISC(63:48)
TRIPT1_DISC_OUT_S1(15.0) — DISC(47:32)
TRIPT0_DISC_OUT_S0(15.0) — DISC(31:16)
TRIPT1_DISC_OUT_S0(15.0) — DISC(15.0)

CLOCKS_DFPGA(2) — R309 1kohms — DIGITAL_GND
CLOCKS_DFPGA(1) — R286 1kohms — DIGITAL_GND
CLOCKS_DFPGA(0) — R285 1kohms — DIGITAL_GND
CLK53 — R308 1kohms — DIGITAL_GND
R306 1kohms
R304 1kohms
R307 1kohms
DIGITAL_GND

CLOCKS_DFPGA(2)
CLOCKS_DFPGA(1)
CLOCKS_DFPGA(0)
VERT_IPLD_S0(7.0) → VERT_IPLD_S0(7.0)
CLOCKS_DFPGA(2.0) → CLOCKS_DFPGA(2.0)
COLLECTOR_ID(9.0) → COLLECTOR_ID(9.0)
DFPGA_WRITE
DFPGA_CS
TMS
TCK
TDI
TDO
JTAG_VCC
R74 49.9ohms
TS17 SAMTEC_TS-106-T-A-1
DIGITAL_GND

XILINX
U159
XC2S150-5PQ208C

DFPGA_CCLK → DFPGA_CCLK
DFPGA_BUSY → DFPGA_BUSY
LVDS_DRIVE(20.0) → LVDS_DRIVE(20.0)
SCL_BUS(6.0) → SCL_BUS(6.0)
DFPGA_INIT → DFPGA_INIT
DFPGA_PROGRAM → DFPGA_PROGRAM
PROG_and_COMM_BUS(7.0)
SCL_BUS(0)
DFPGA_DONE → DFPGA_DONE
MODE_BUS → MODE_BUS
VERT_IPLD_S1(7.0) → VERT_IPLD_S1(7.0)
COMM_STRB_DFPGA(2.0) → COMM_STRB_DFPGA(2.0)

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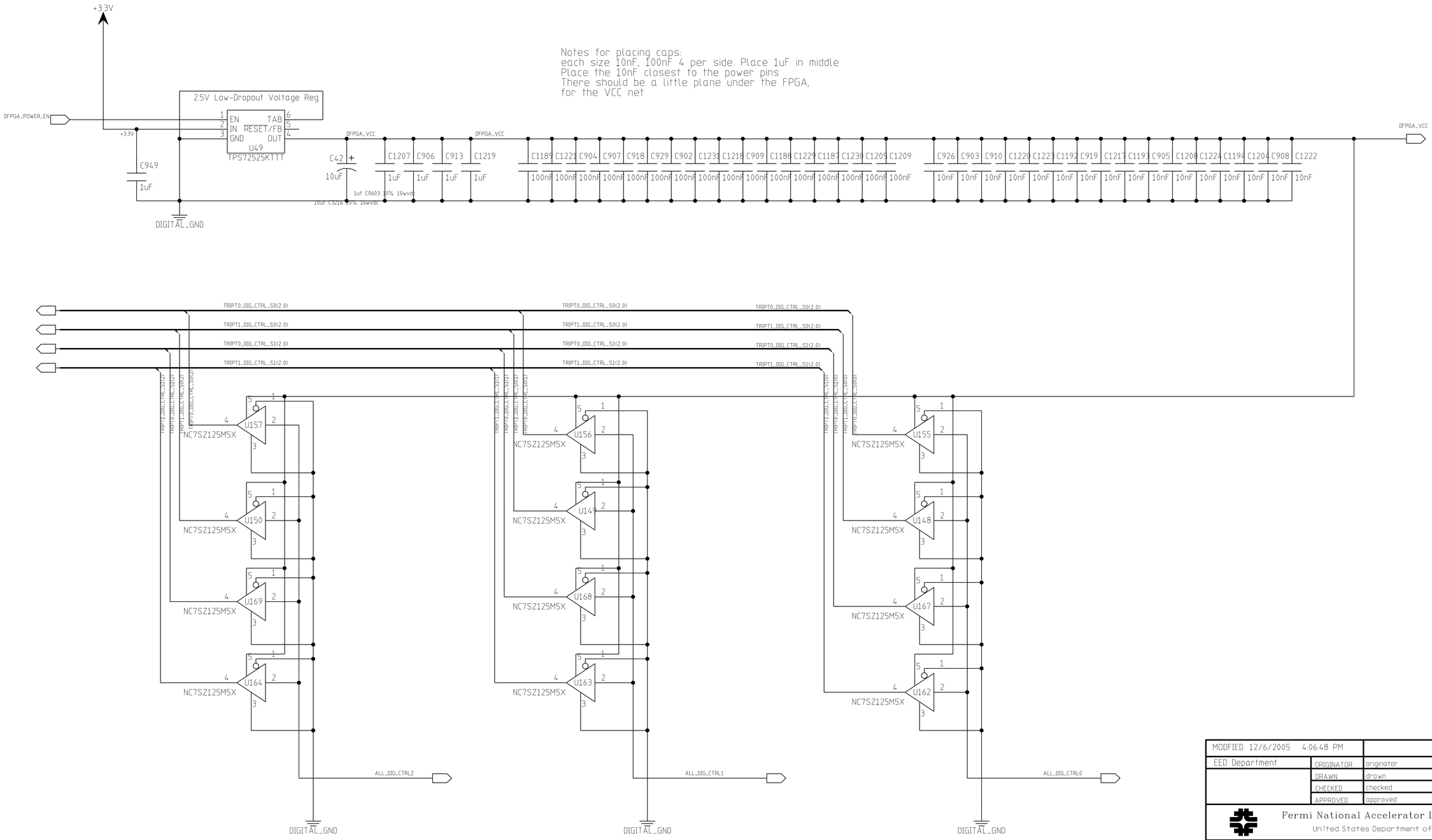
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer	10

H:8ND, V:4LA



MODFIED 12/6/2005 4:06:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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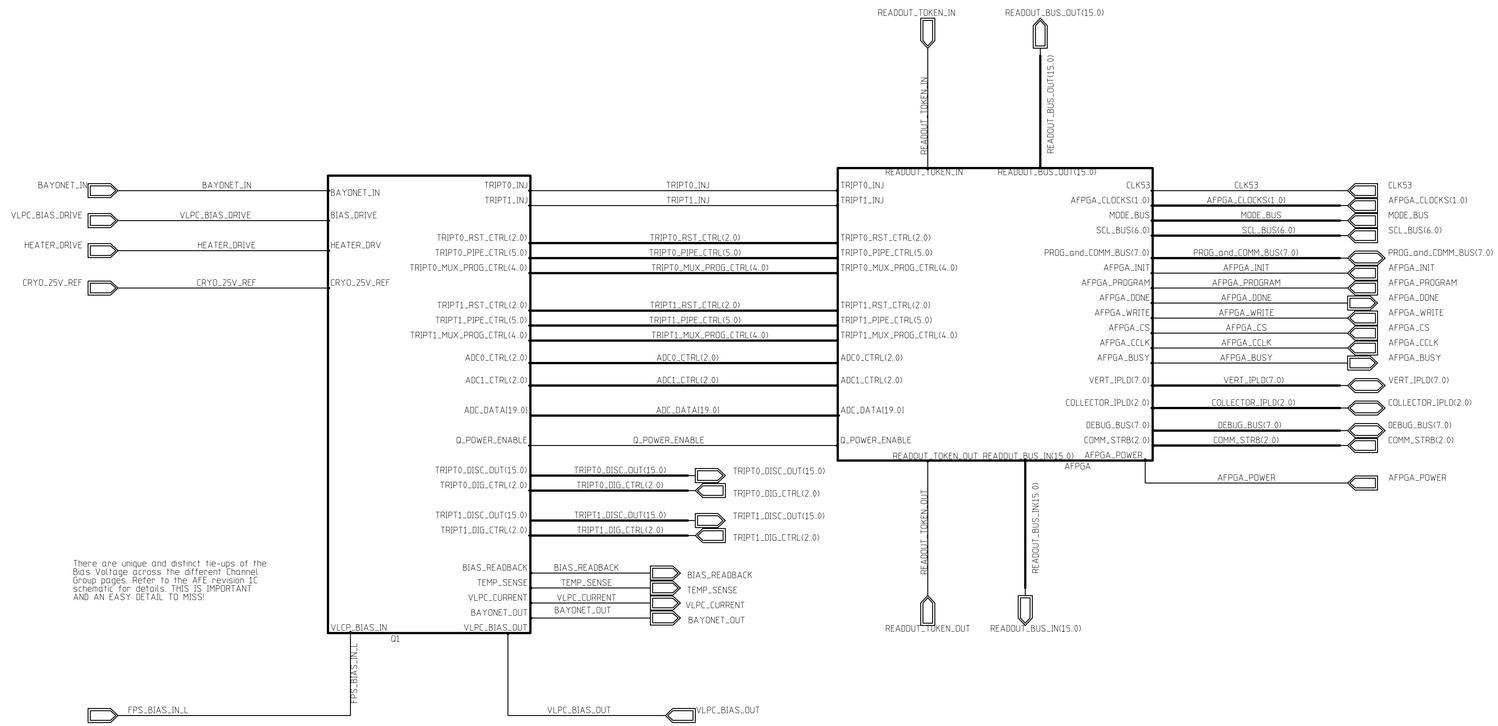
C:\Projects\AFEII-T\Board Production\AFE_II+_Rev5\AFE_II+_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_	10

H:8ND, V:4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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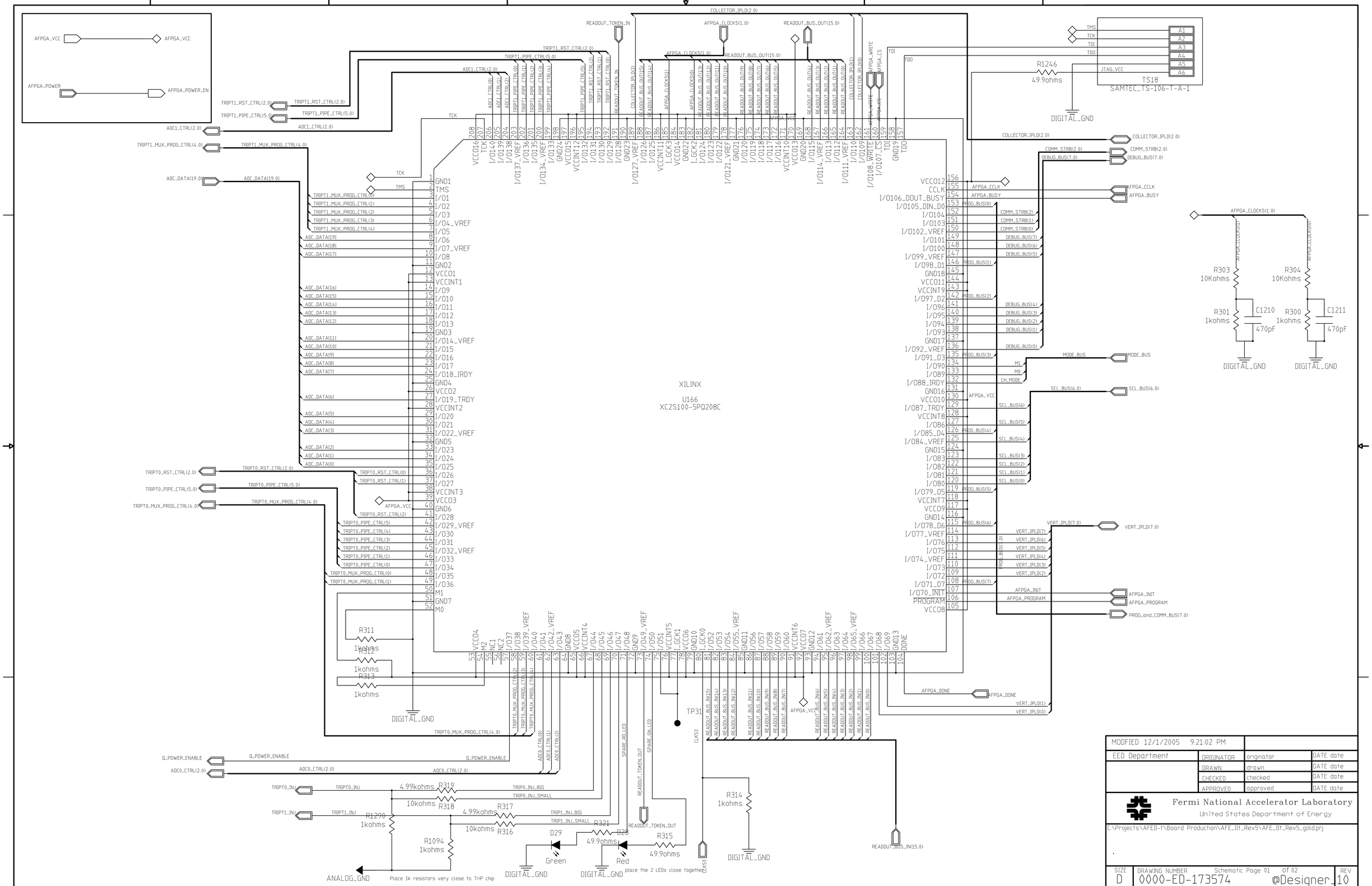
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA


XILINX
U166
XC2S100-5PQ208C
TS18
SAMTEC_TS-106-T-A-1
R1246
49.9ohms
DIGITAL_GND
R303
10Kohms
R304
10Kohms
R301
1kohms
R300
1kohms
C1210
470pF
C1211
470pF
R311
1kohms
R312
1kohms
R313
1kohms
R319
4.99kohms
R318
10kohms
R317
4.99kohms
R316
10kohms
R321
49.9ohms
R315
49.9ohms
R314
1kohms
R1290
1kohms
R1094
1kohms
D29
Green
D28
Red
TP31
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
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SIZE
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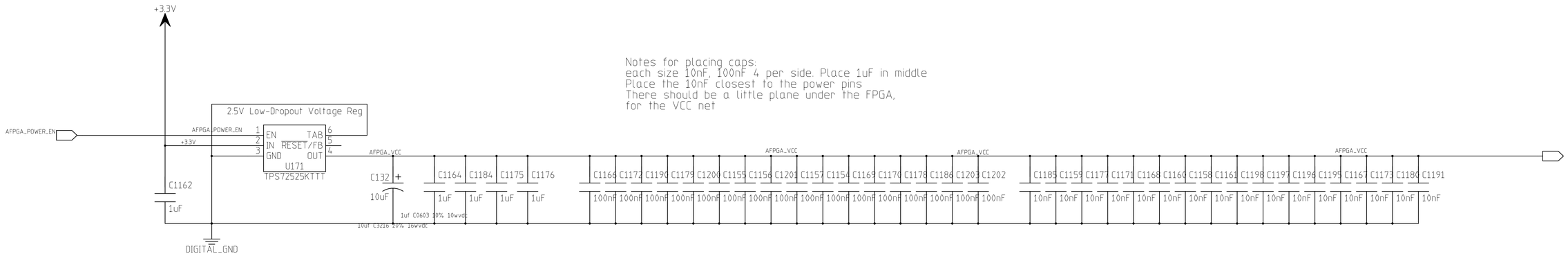
Schematic Page 01 of 02
@Designer
REV
10



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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EED Department	ORIGINATOR	originator	DATE date
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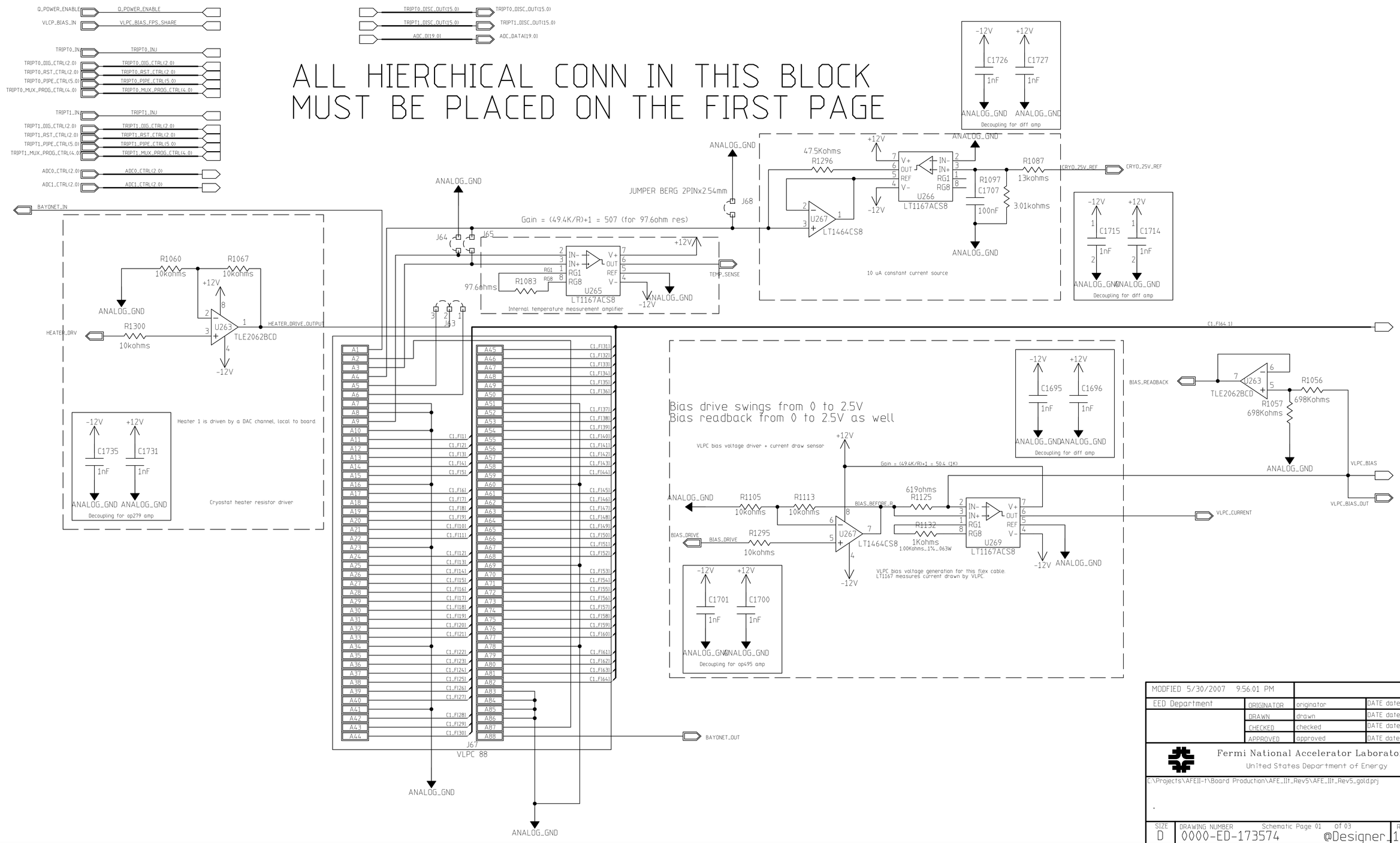
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H=8ND, V=4LA


ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
BAYONET_IN
ANALOG_GND
HEATER_DRV
R1300
10kohms
R1060
R1067
U263
TLE2062BCD
HEATER_DRIVE_OUTPUT
C1735
C1731
1nF
Heater 1 is driven by a DAC channel, local to board.
Cryostat heater resistor driver
Decoupling for op279 amp
J64
J65
J63
J67
VLPC 88
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
97.6ohms
R1083
U265
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
JUMPER BERG 2PINx2.54mm
J68
47.5Kohms
R1296
U267
LT1464CS8
U266
LT1167ACS8
R1087
13kohms
R1097
3.01kohms
C1707
100nF
CRYO_25V_REF
10 uA constant current source
C1726
C1727
C1715
C1714
Decoupling for diff amp
C1_FI64.1
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R1105
10kohms
R1113
10kohms
BIAS_BEFORE_R
619ohms
R1125
R1132
1Kohms
1.00Kohms_1%_.063W
R1295
10kohms
BIAS_DRIVE
U269
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
C1695
C1696
C1701
C1700
Decoupling for op495 amp
BIAS_READBACK
R1056
698Kohms
R1057
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
VLPC_CURRENT
BAYONET_OUT
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checked
approved
DATE date
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United States Department of Energy
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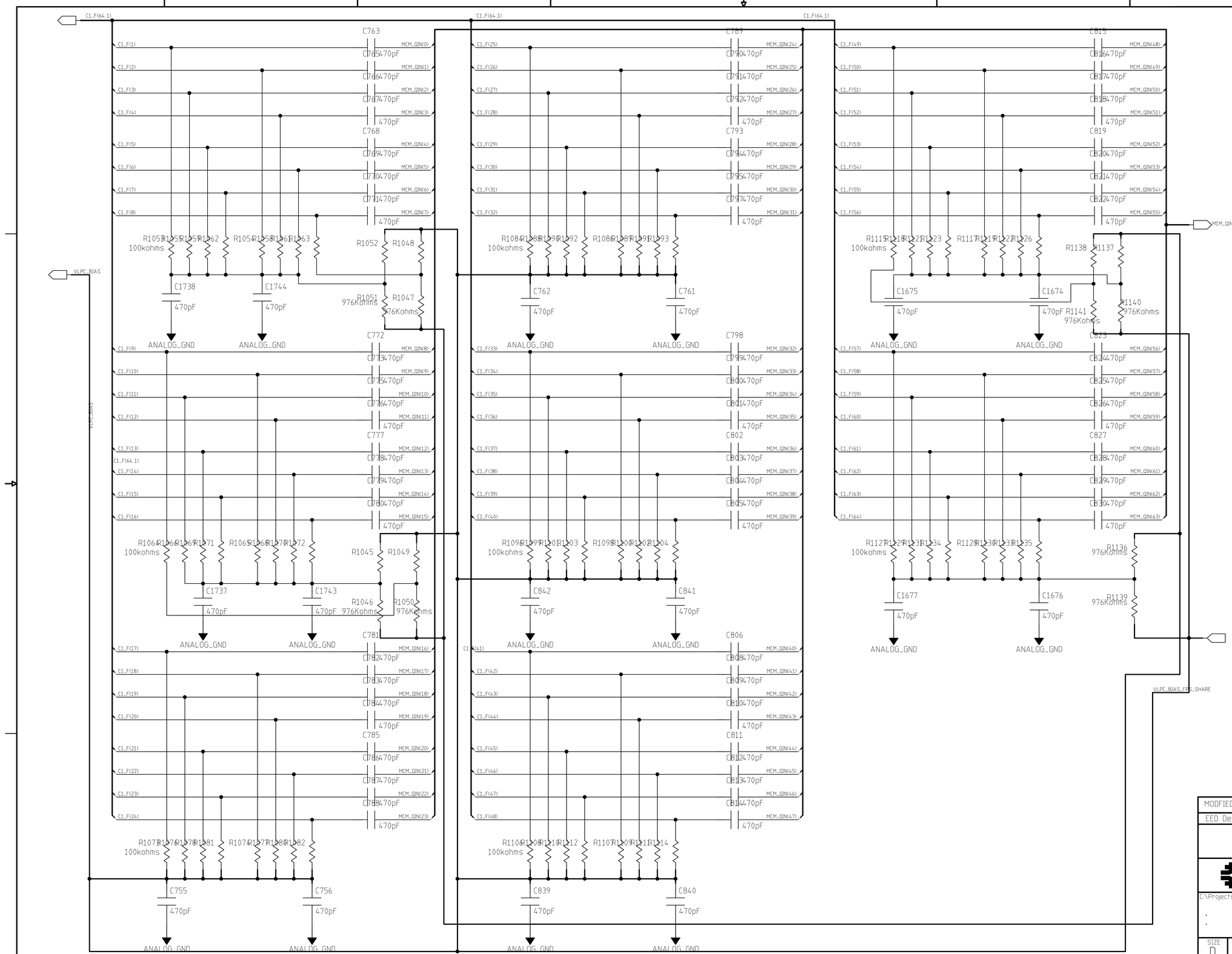
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV
H:8ND, V:4LA



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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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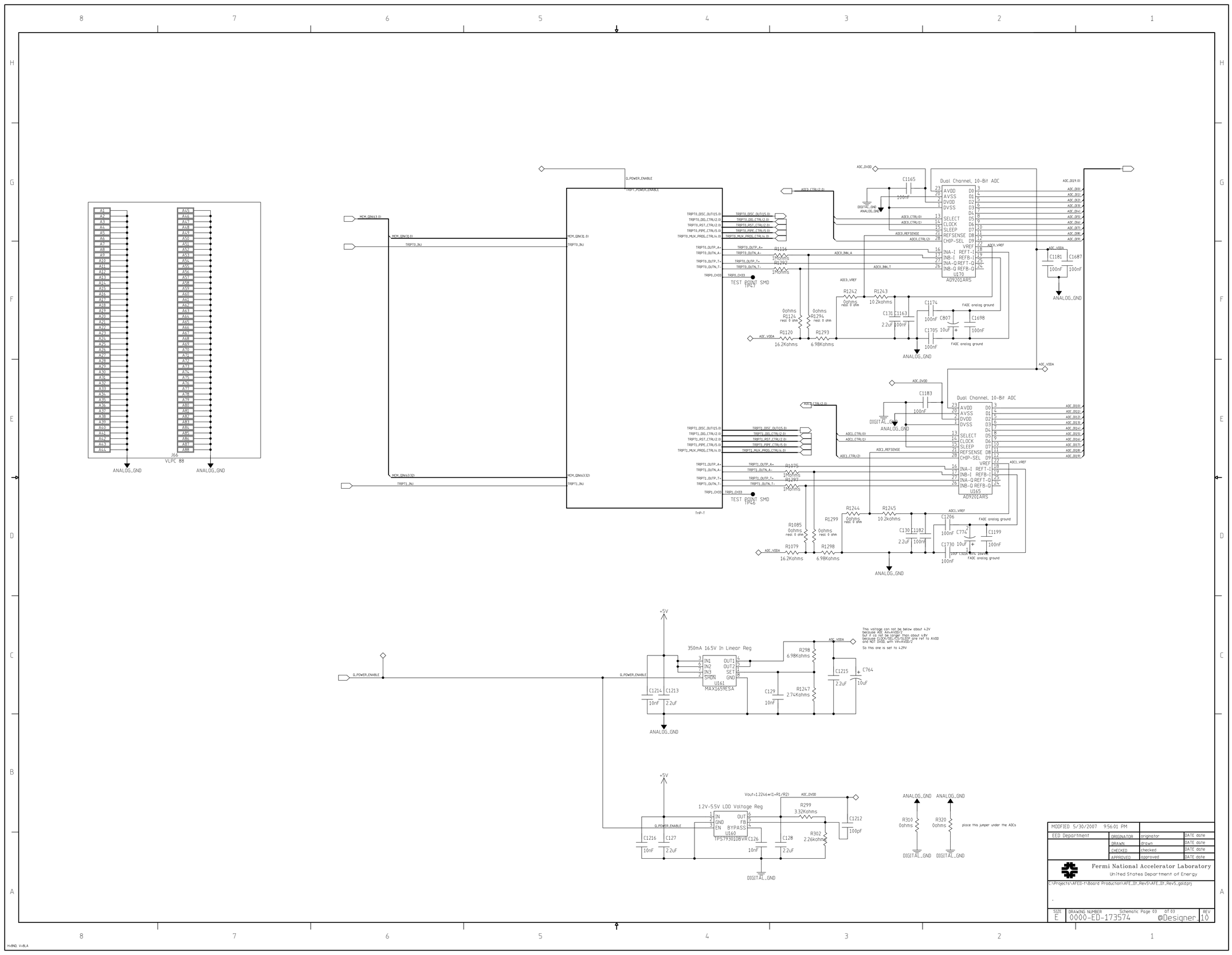
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H:8ND, V:4LA



MODFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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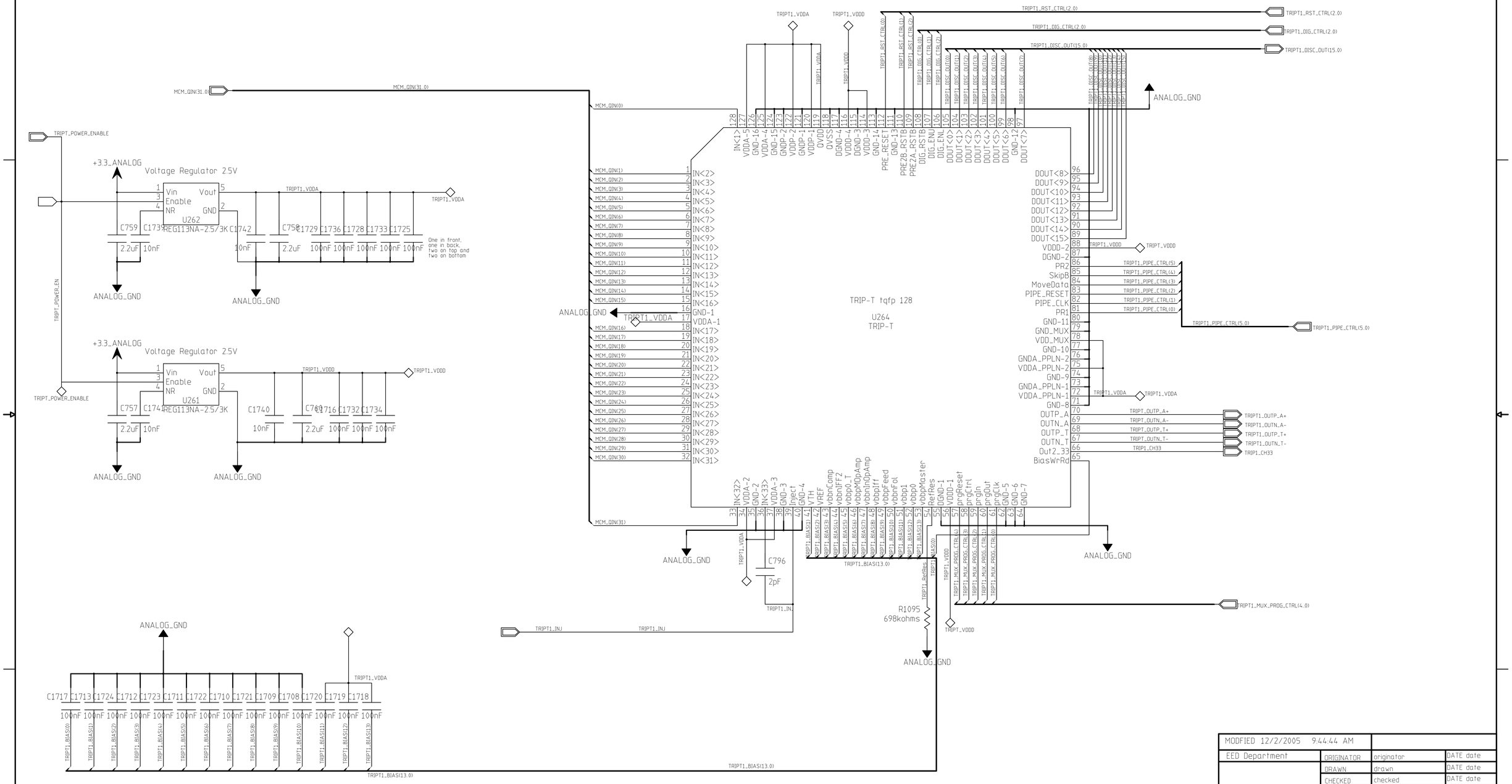
SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

H:\BND, V:\BLA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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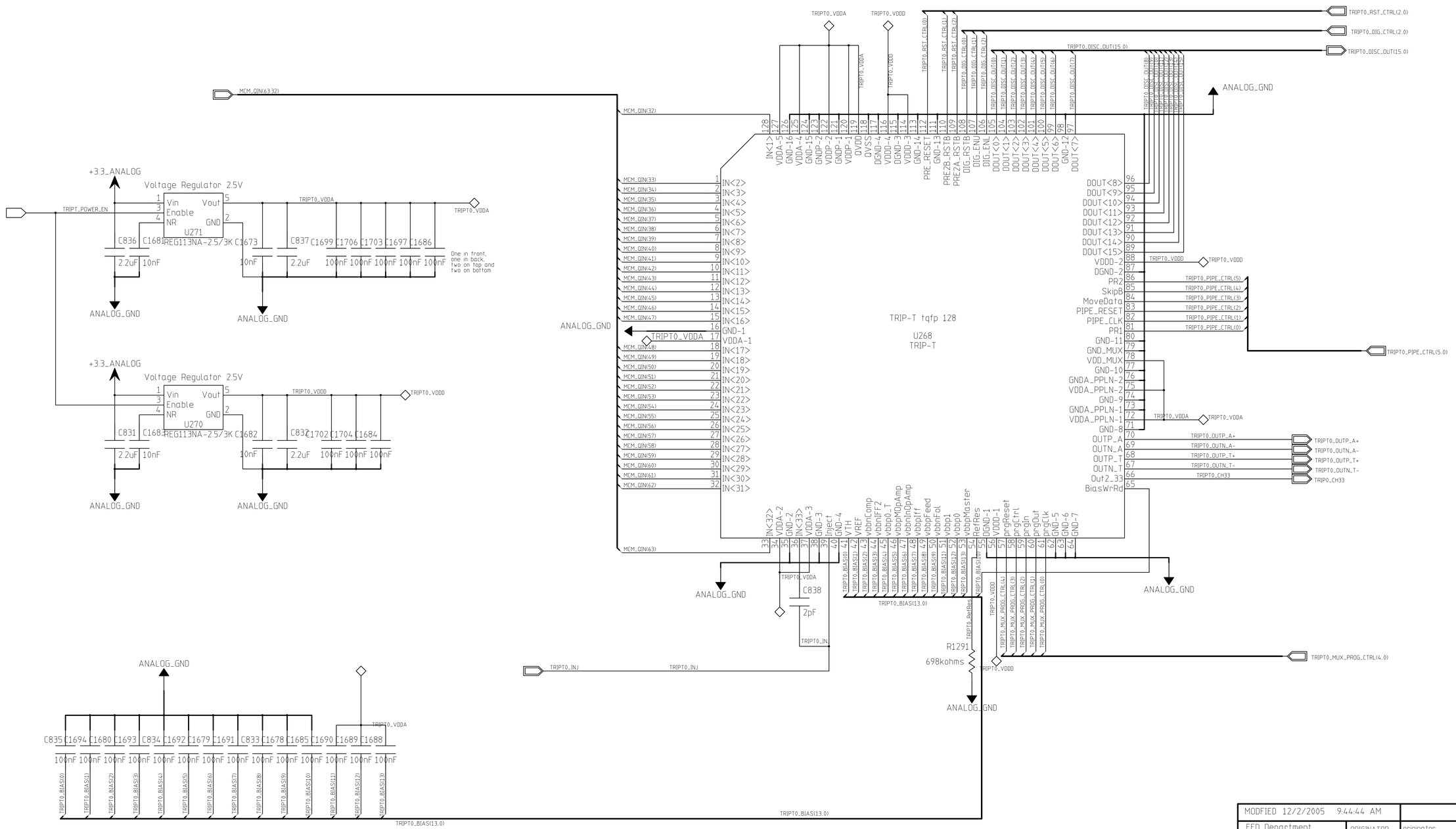
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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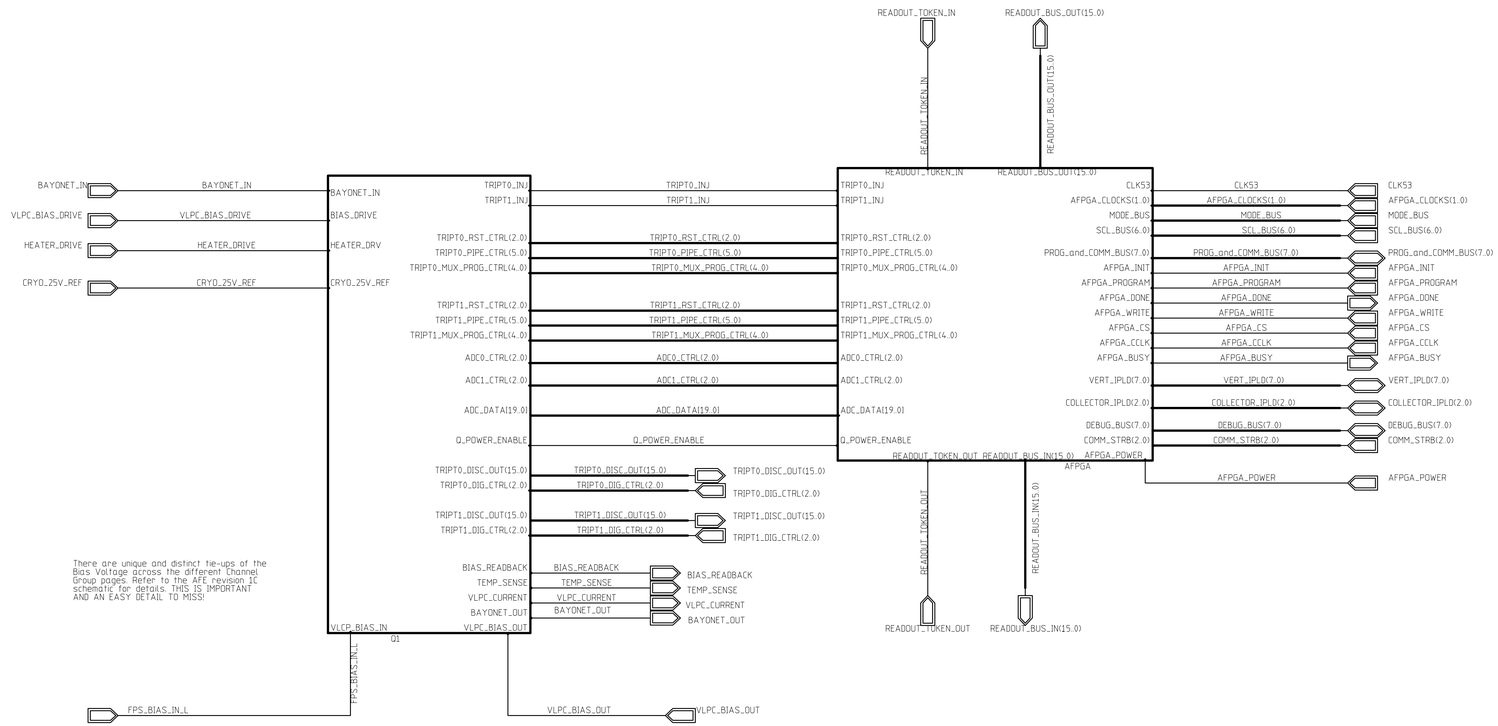
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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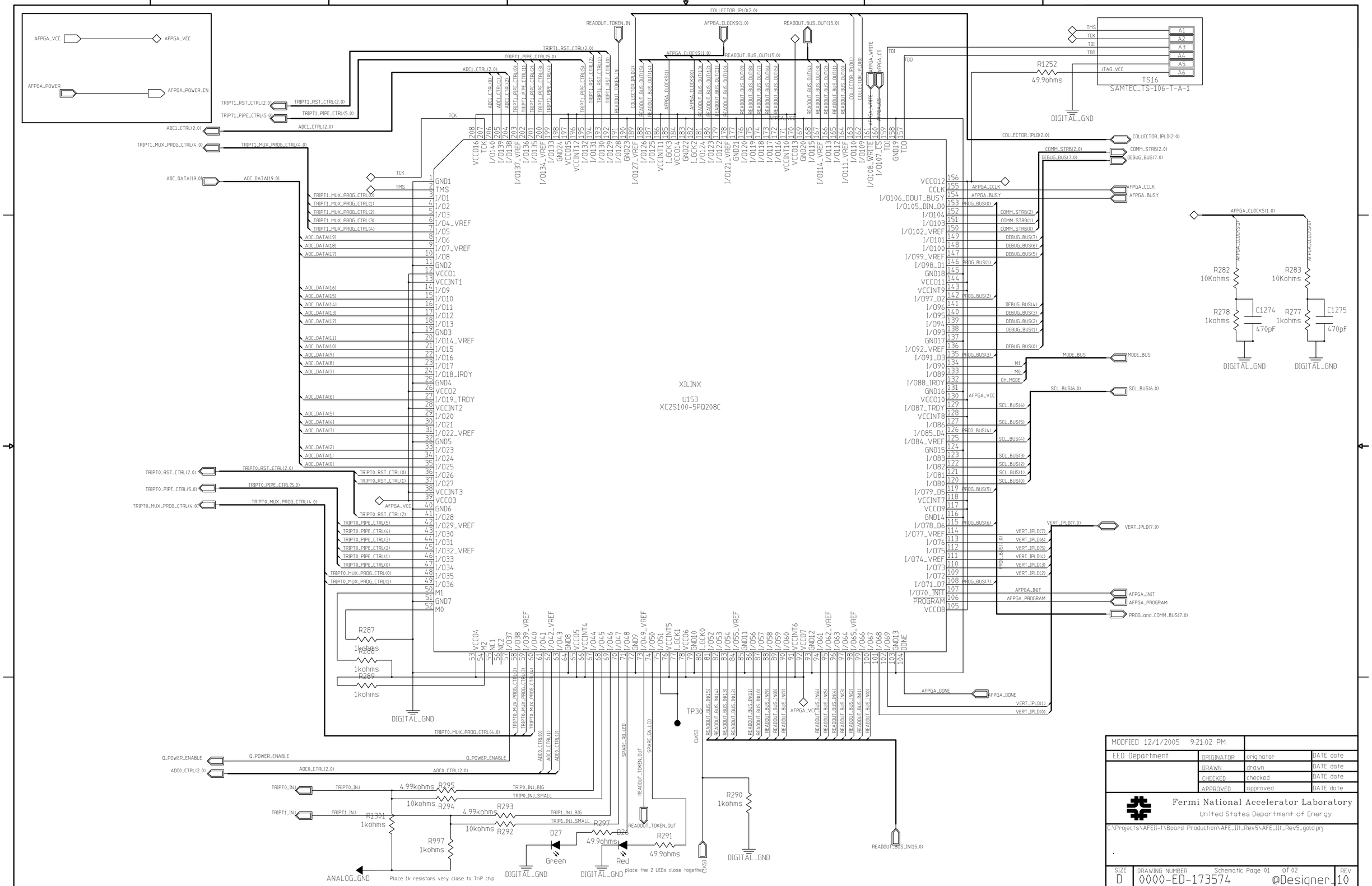
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA


XILINX
U153
XC2S100-5PQ208C
TS16
SAMTEC_TS-106-T-A-1
R1252
49.9ohms
R282
10Kohms
R283
10Kohms
R278
1kohms
R277
1kohms
C1274
470pF
C1275
470pF
R287
1kohms
R288
1kohms
R289
1kohms
R295
4.99kohms
R294
10kohms
R293
4.99kohms
R292
10kohms
R1301
1kohms
R997
1kohms
R297
49.9ohms
R291
49.9ohms
R290
1kohms
D27
Green
D26
Red
TP30
DIGITAL_GND
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
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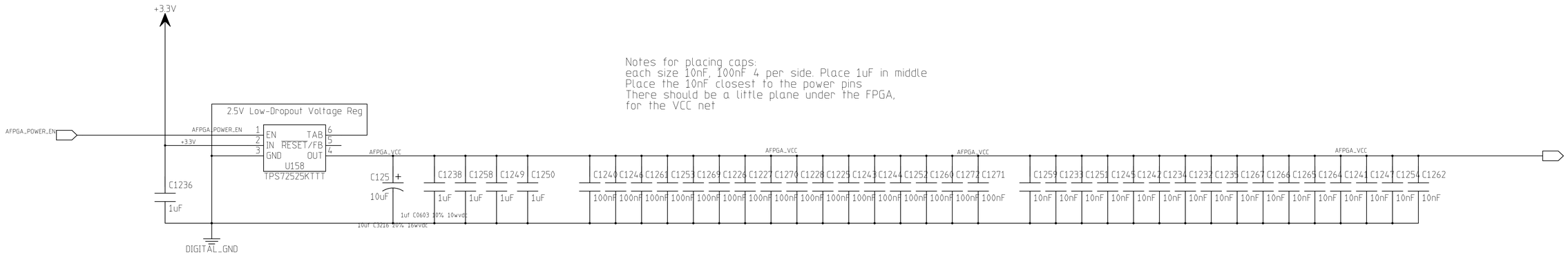
Schematic Page 01 of 02
REV
10
@Designer



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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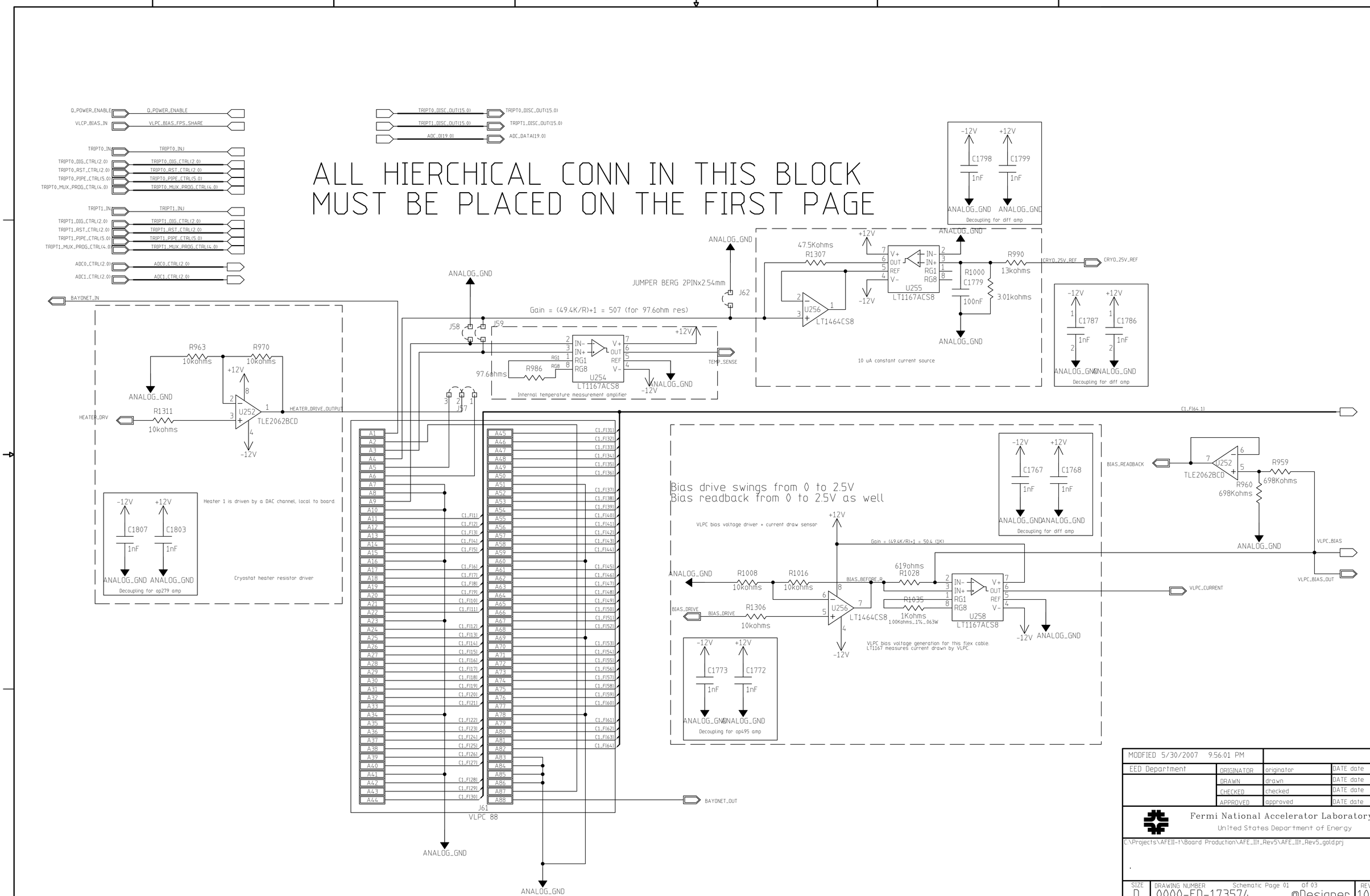
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H=8ND, V=4LA


ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
VLCP_BIAS_FPS_SHARE
TRIPT0_IN
TRIPT0_INJ
TRIPT1_IN
TRIPT1_INJ
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
BAYONET_IN
BAYONET_OUT
HEATER_DRV
HEATER_DRIVE_OUTPUT
R963
10kohms
R970
10kohms
R1311
10kohms
U252
TLE2062BCD
Heater 1 is driven by a DAC channel, local to board.
Cryostat heater resistor driver
C1807
C1803
1nF
Decoupling for op279 amp
ANALOG_GND
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
J58
J59
J57
J62
JUMPER BERG 2PINx2.54mm
R986
97.6ohms
U254
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
47.5Kohms
R1307
U256
LT1464CS8
U255
LT1167ACS8
R1000
C1779
100nF
R990
13kohms
3.01kohms
10 uA constant current source
CRYO_25V_REF
C1798
C1799
C1787
C1786
Decoupling for diff amp
C1_FI64_1
J61
VLPC 88
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R1008
10kohms
R1016
10kohms
R1306
10kohms
BIAS_DRIVE
BIAS_BEFORE_R
619ohms
R1028
R1035
1Kohms
1.00Kohms_1%_.063W
U258
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
C1773
C1772
Decoupling for op495 amp
C1767
C1768
BIAS_READBACK
R959
698Kohms
R960
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
VLPC_CURRENT
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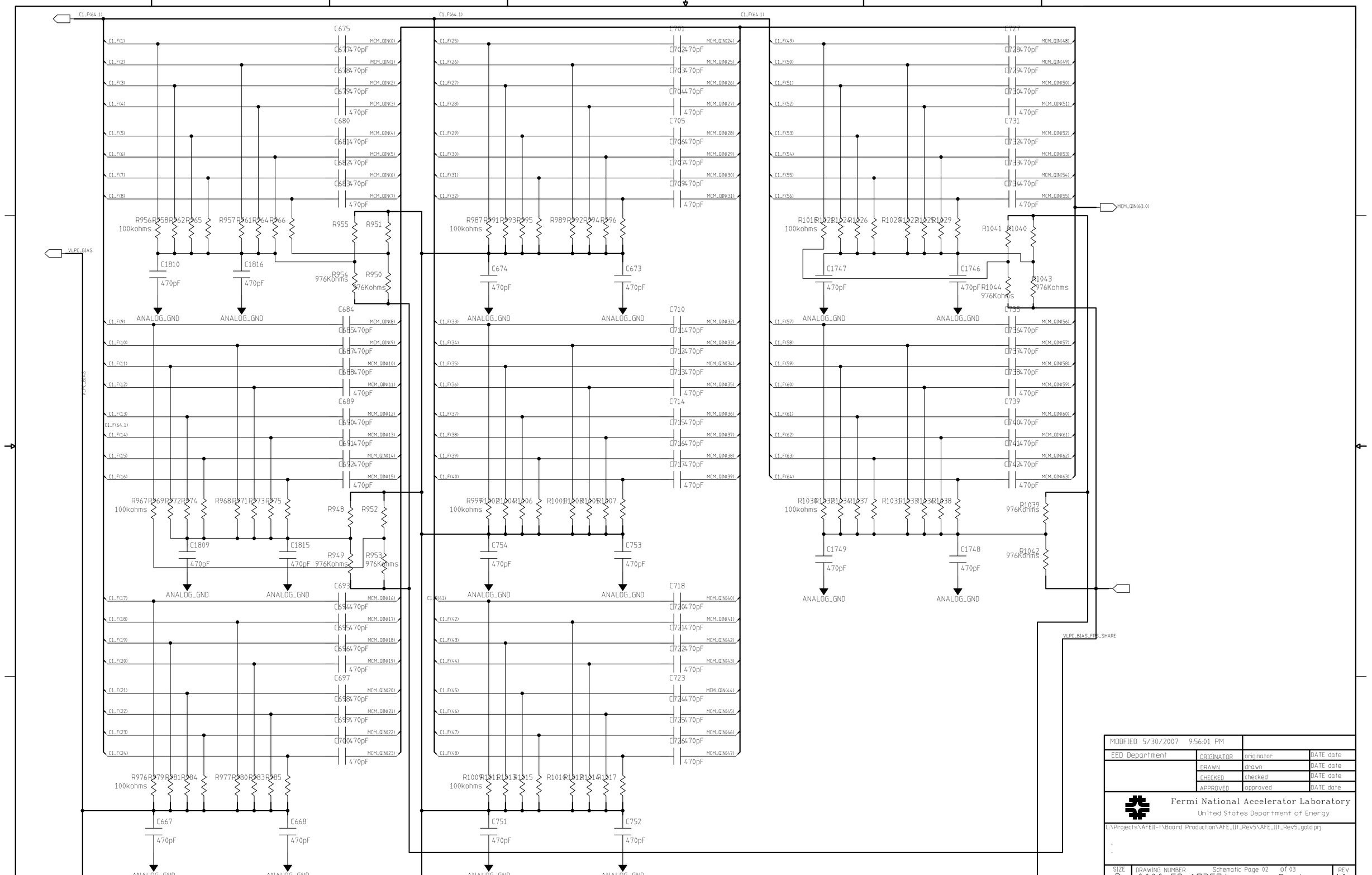
drawn
checked
approved
DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE
D
DRAWING NUMBER
0000-ED-173574
Schematic Page 01 of 03
@Designer_1
REV
10
H=8ND, V=4LA



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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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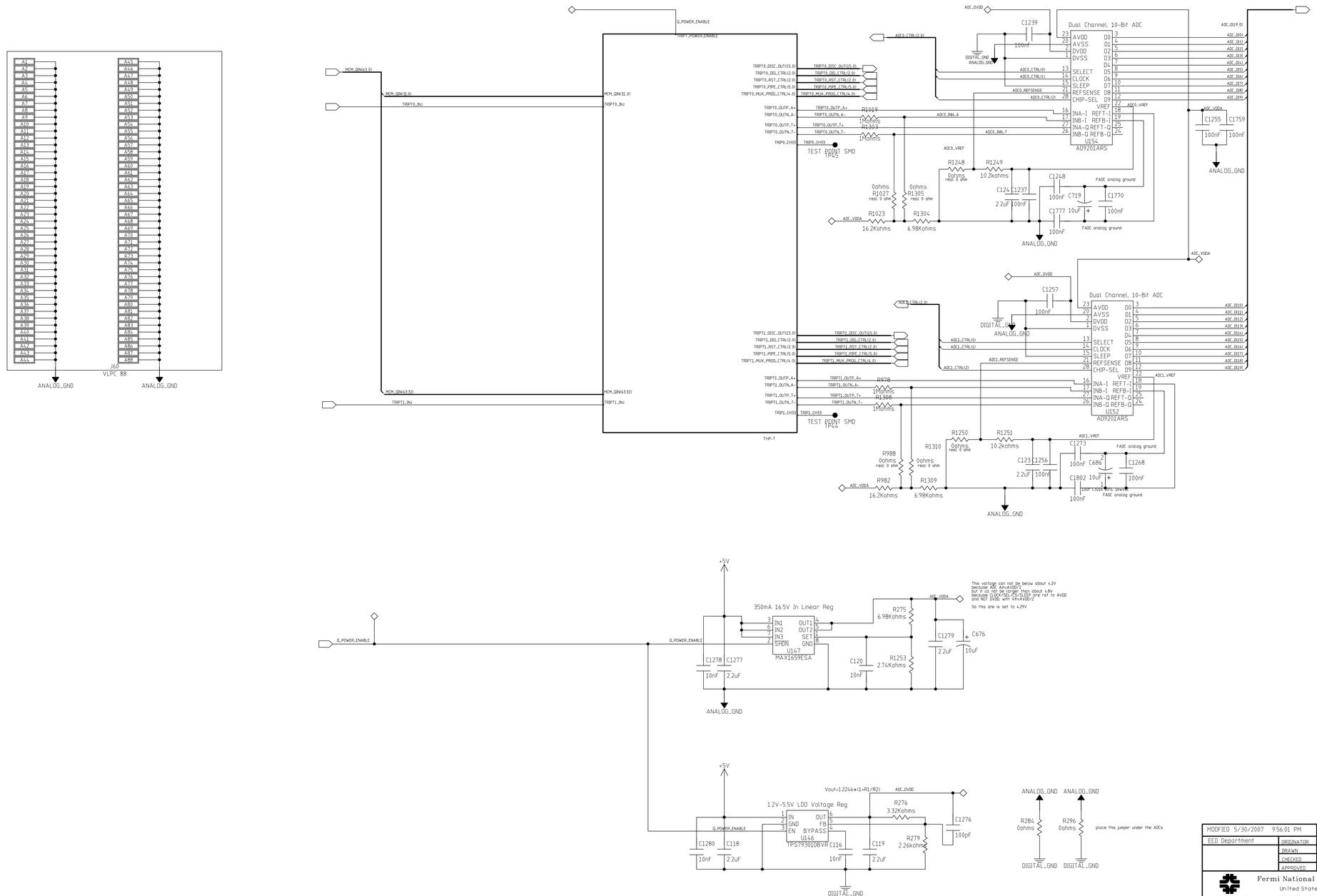
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H:8ND, V:4LA



MODIFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
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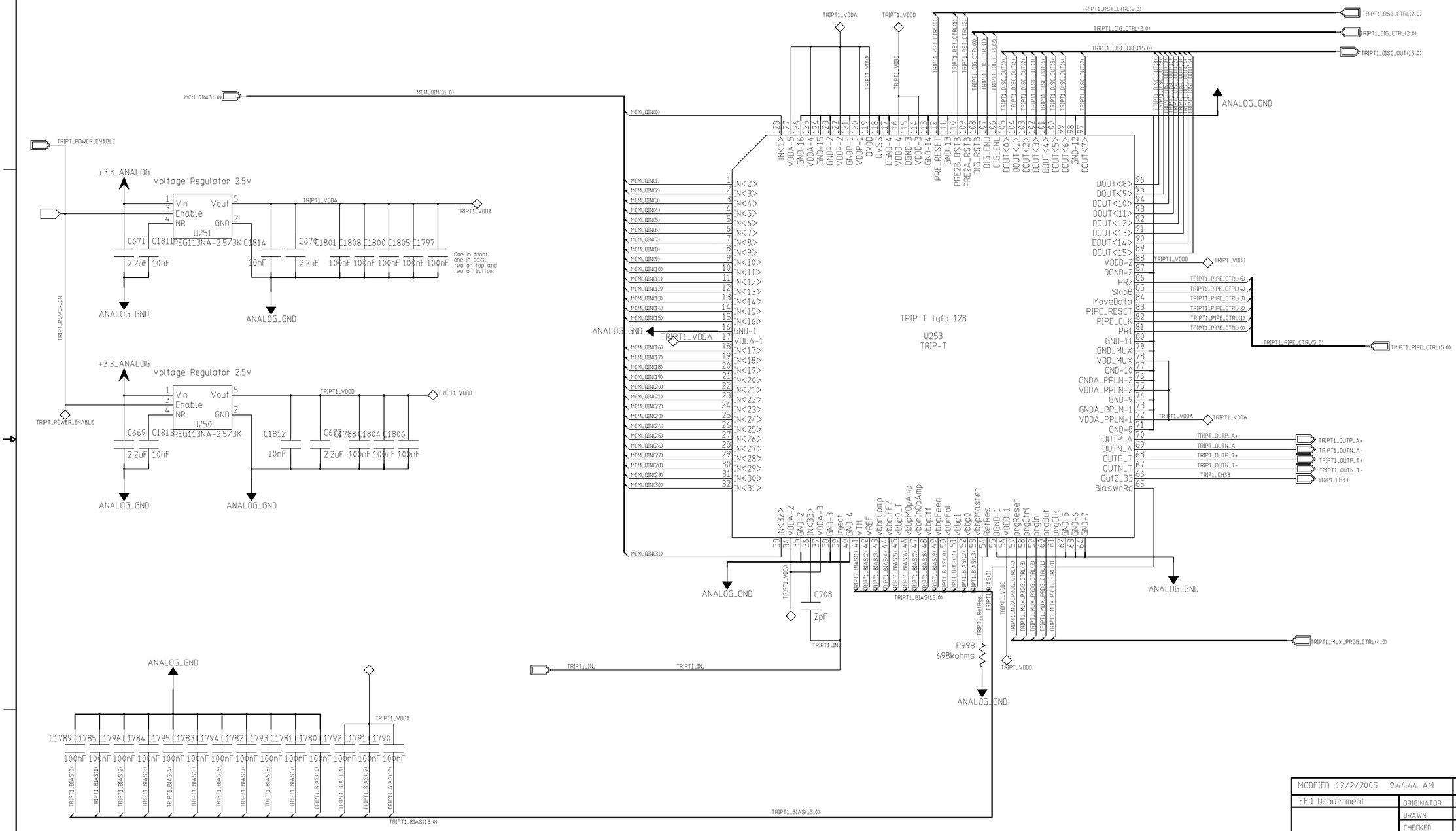
SIZE	DRAWING NUMBER	REV
E	0000-ED-173574 Schematic Page 03 of 03 @Designer_10	

HnBND V:BLA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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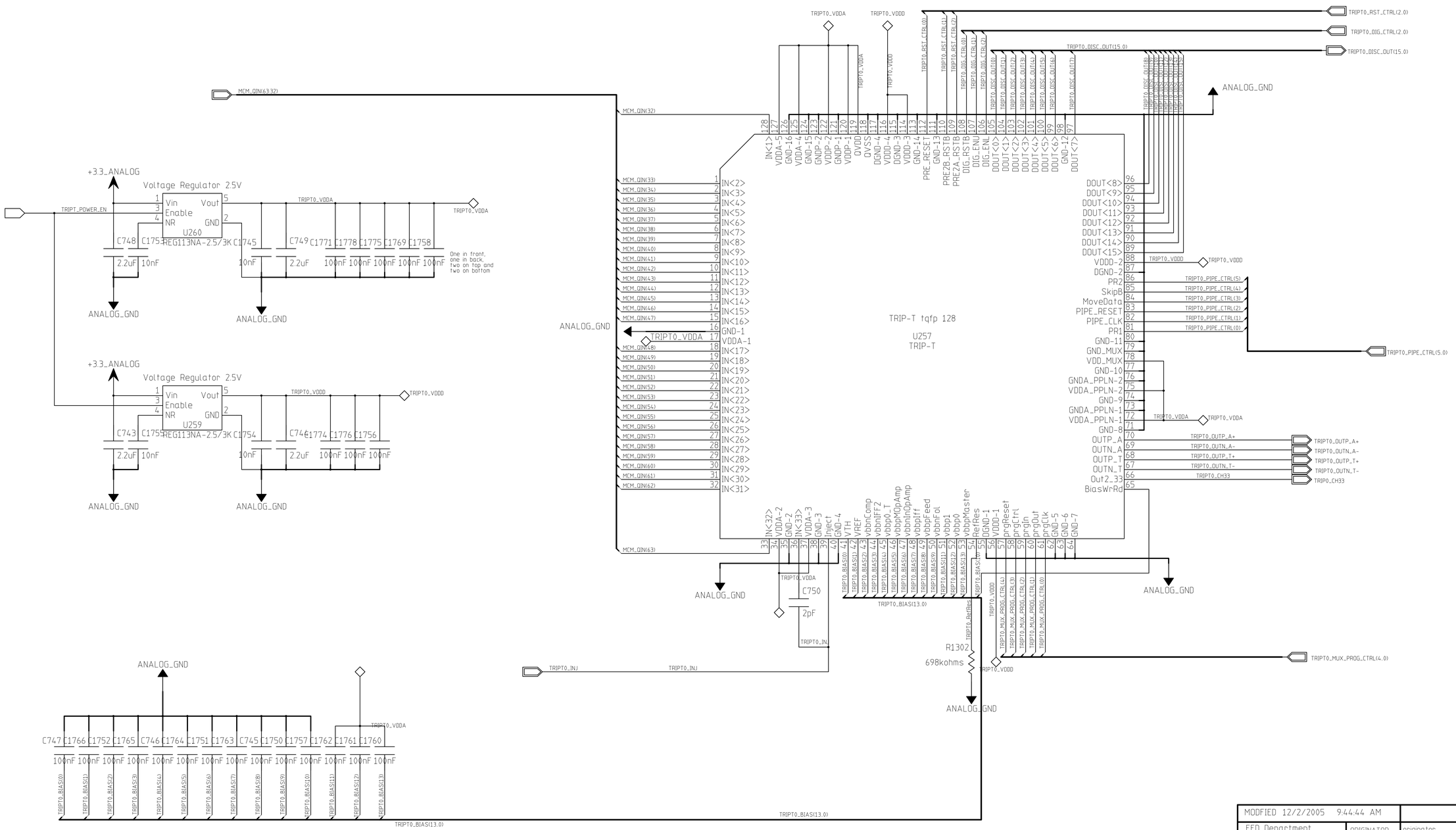
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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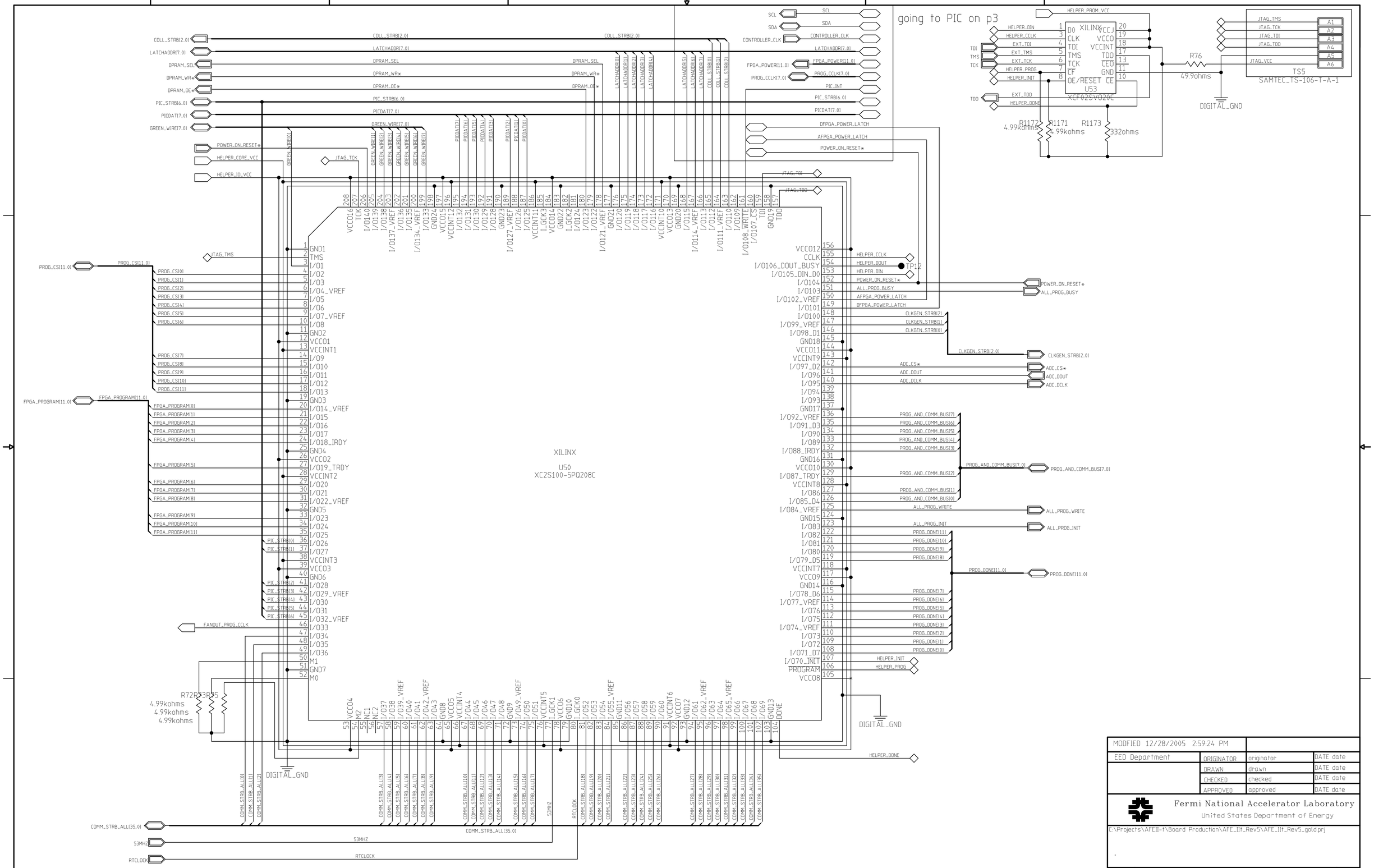
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA


XILINX
U50
XC2S100-5PQ208C
going to PIC on p3
XILINX
U53
XCF02SVO20C
TS5
SAMTEC_TS-106-T-A-1
R76
49.9ohms
R1172
4.99kohms
R1171
4.99kohms
R1173
332ohms
R72R73R75
4.99kohms
4.99kohms
4.99kohms
DIGITAL_GND
TP12
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ORIGINATOR originator DATE date
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SIZE D
DRAWING NUMBER 0000-ED-173574
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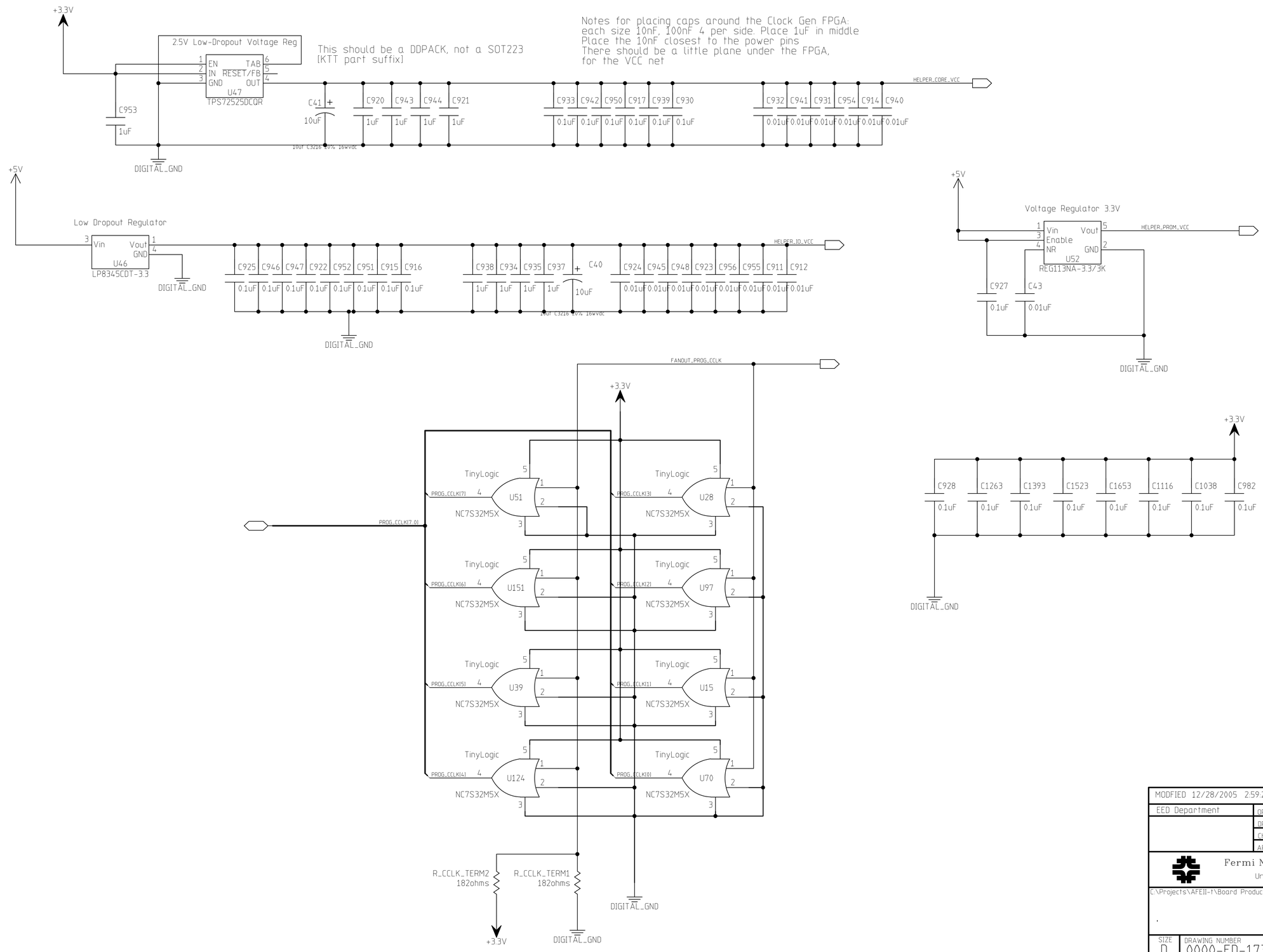
@Designer_10
REV



MODFIED 12/28/2005 2:59:24 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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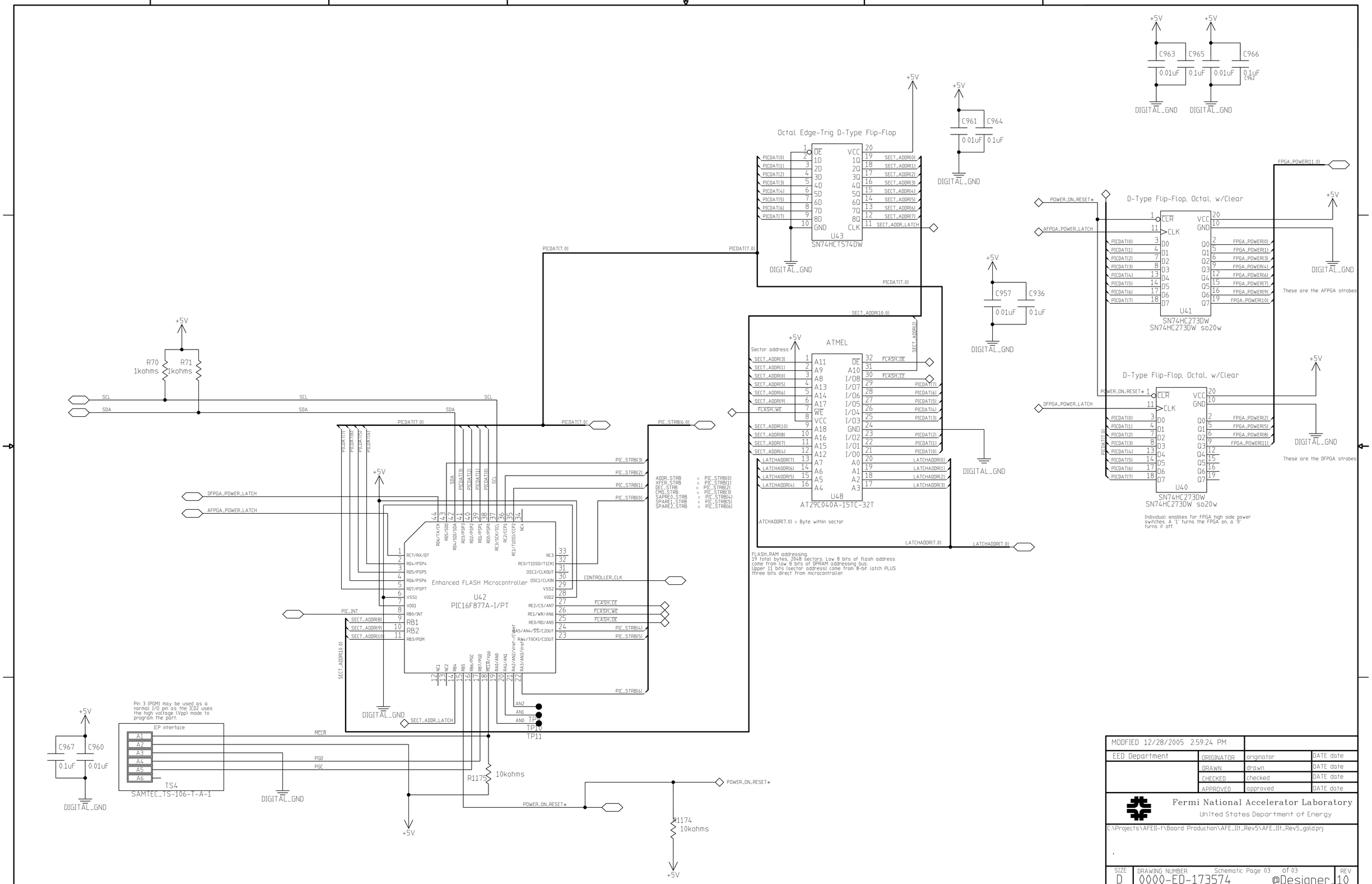
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_1	0

H:8ND, V:4LA


Octal Edge-Trig D-Type Flip-Flop
U43
SN74HCT574DW
ATMEL
U48
AT29C040A-15TC-32T
ATCHADDR[7..0] = Byte within sector
FLASH_RAM addressing
19 total bytes, 2048 sectors. Low 8 bits of flash address come from low 8 bits of DPRAM addressing bus.
Upper 11 bits (sector address) come from 8-bit latch PLUS three bits direct from microcontroller.
D-Type Flip-Flop, Octal, w/Clear
U41
SN74HC273DW
SN74HC273DW so20w
These are the AFPGA strobes
U40
These are the DFPGA strobes
Individual enables for FPGA high side power switches. A '1' turns the FPGA on, a '0' turns it off.
Enhanced FLASH Microcontroller
U42
PIC16F877A-I/PT
ADDR_STRB = PIC_STRB(0)
XFER_STRB = PIC_STRB(1)
DEC_STRB = PIC_STRB(2)
CMD_STRB = PIC_STRB(3)
SAPRE0_STRB = PIC_STRB(4)
SPARE1_STRB = PIC_STRB(5)
SPARE2_STRB = PIC_STRB(6)
Pin 3 (PGM) may be used as a normal I/O pin as the ICD2 uses the high voltage (Vpp) mode to program the part.
ICP interface
TS4
SAMTEC_TS-106-T-A-1
R70 1kohms
R71 1kohms
R1175 10kohms
R1174 10kohms
C963 0.01uF
C965 0.1uF
C966 0.01uF
C962 0.1uF
C961 0.01uF
C964 0.1uF
C957 0.01uF
C936 0.1uF
C967 0.1uF
C960 0.01uF
DIGITAL_GND
+5V
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SIZE D
DRAWING NUMBER 0000-ED-173574
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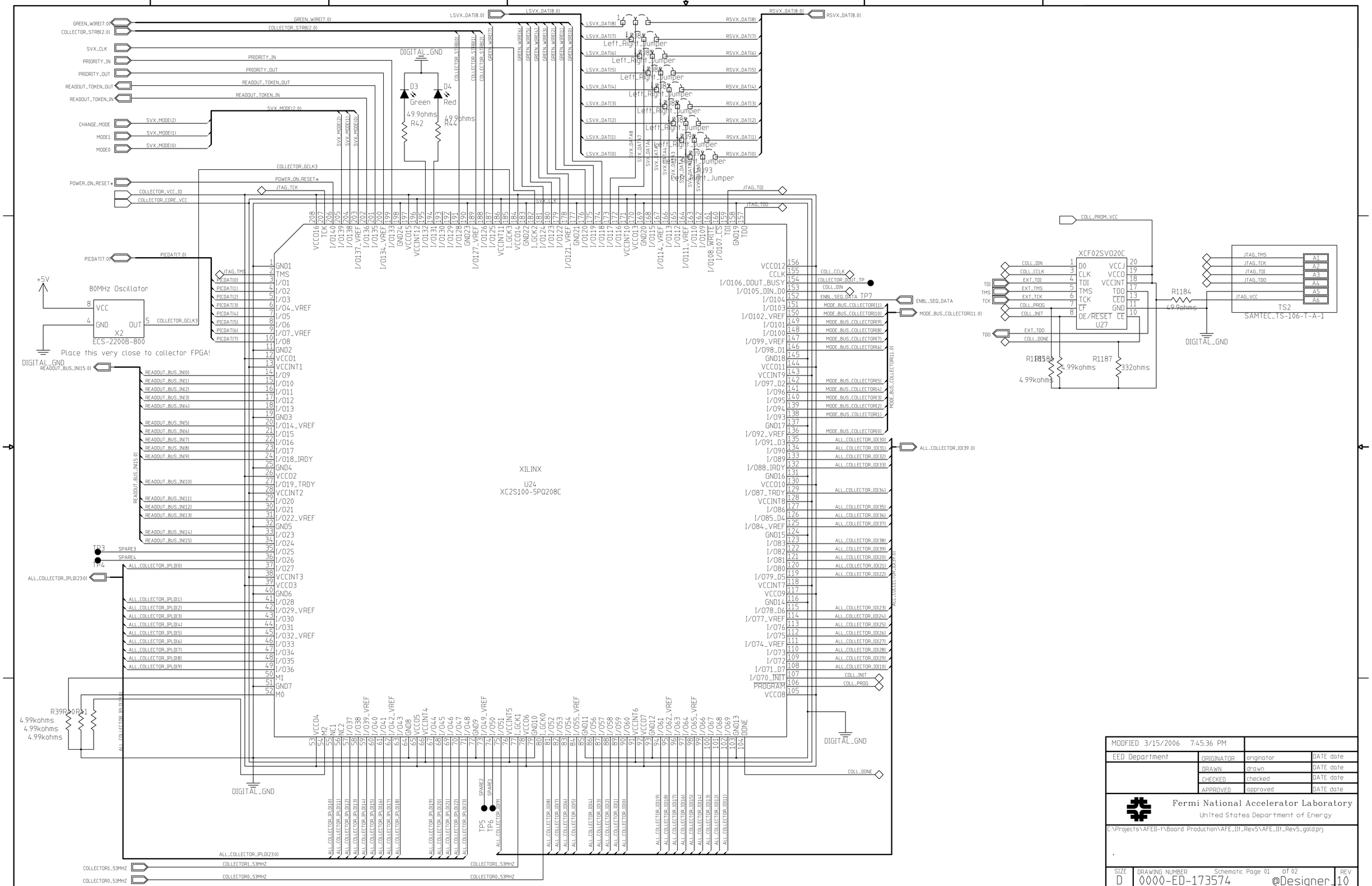
@Designer_10
REV
H=8ND, V=4LA



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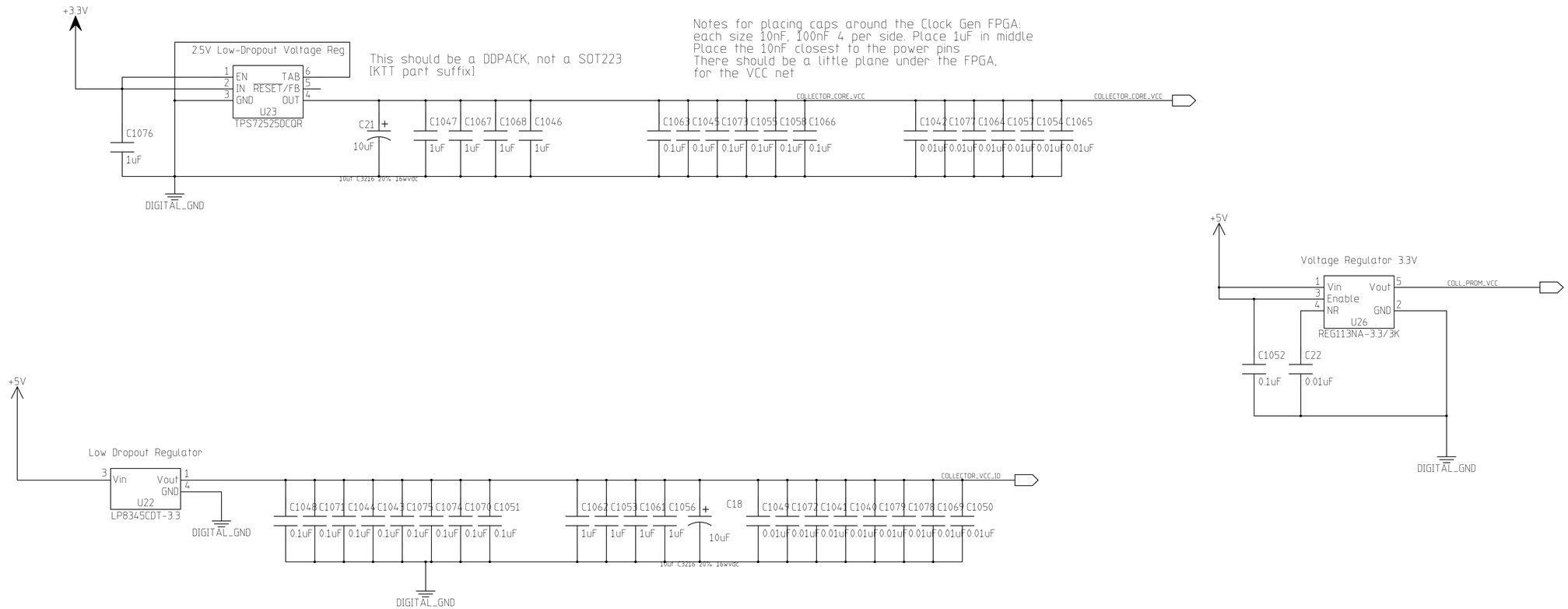

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SIZE	DRAWING NUMBER		REV
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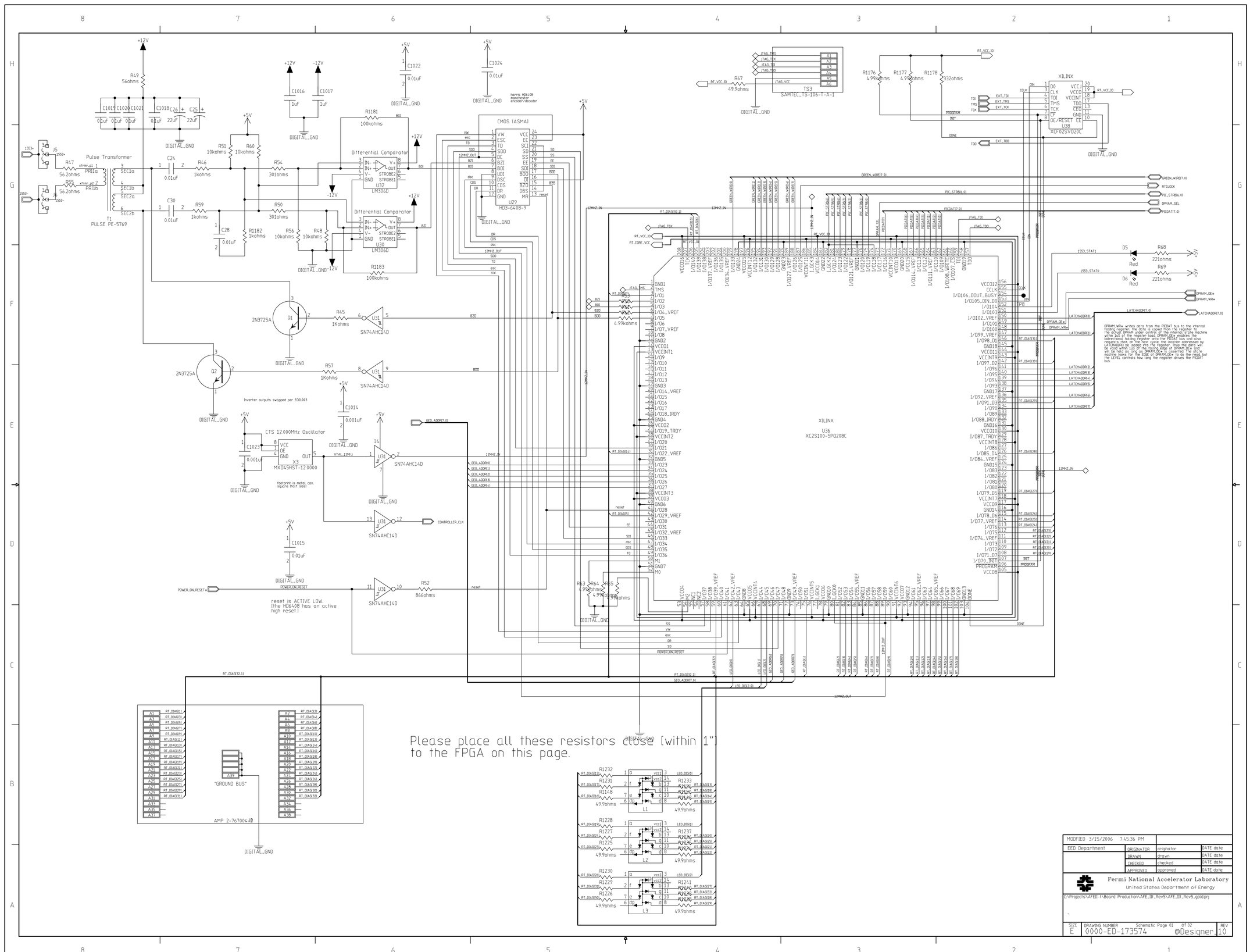
H:8ND, V:4LA



Please place all these resistors close (within 1") to the FPGA on this page.

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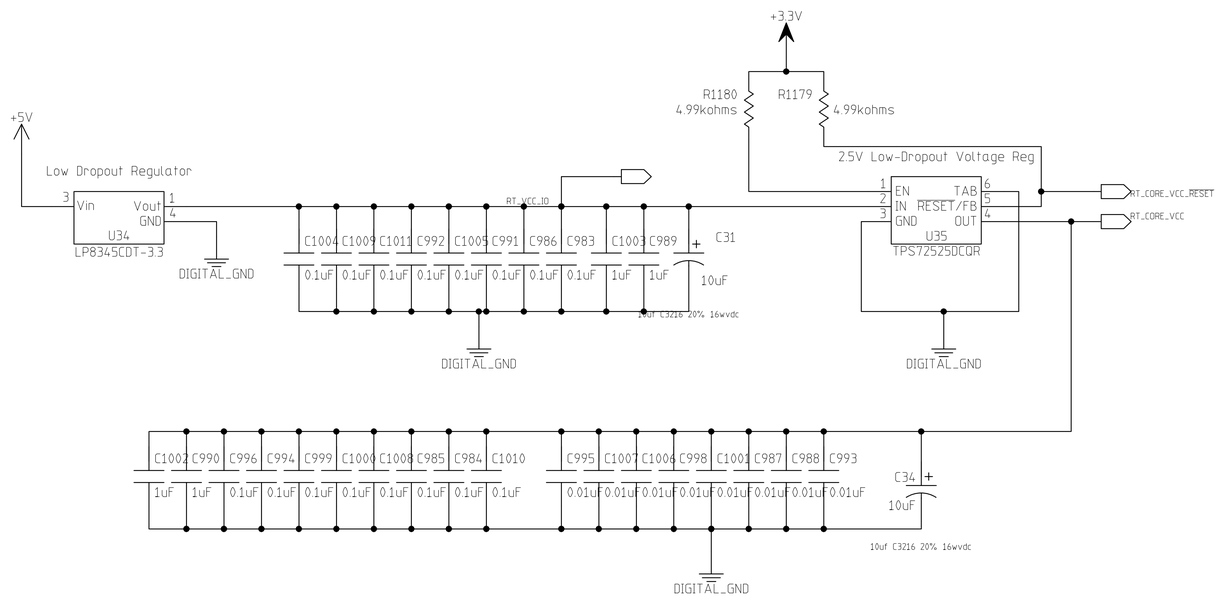

MODFIED 3/15/2006 7:45:36 PM			
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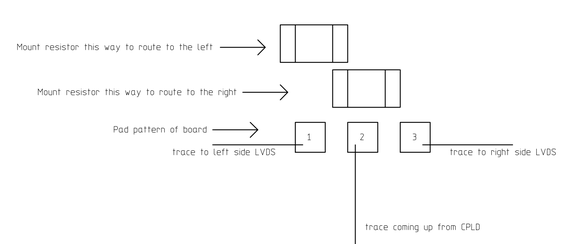
H=8ND, V=4LA

All jumpers are actually 3-pin pad arrays designed to allow installation of a low-resistance 0402 resistor either between pads 1 and 2 or pads 3 and 4, manually routing all eighty bits of the bus to the left-side LDVS drivers or to the right side LVDS drivers. This break removes the long stubs to the unused side allowing the unused side to be unstuffed and eliminating reflection possibilities.

Blowup sketch of how this works



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EED Department	ORIGINATOR	originator	DATE date
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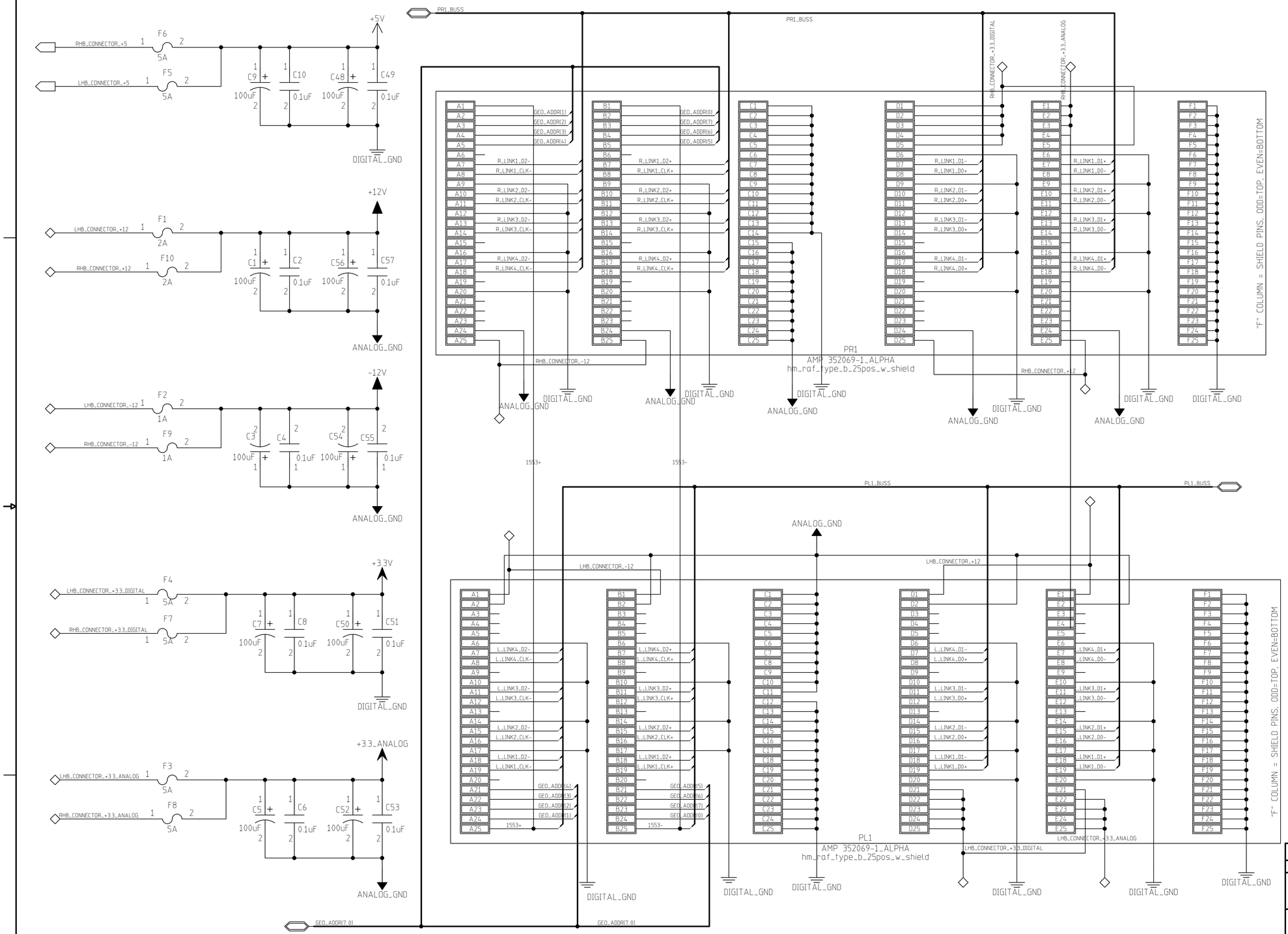
H:8ND, V:4LA



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EED Department	ORIGINATOR	originator	DATE date
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H=8ND, V=4LA

LEFT HAND INSERTION INTO BACKPLANE
PINOUT AS VIEWED FROM BOARD COMPONENT SIDE

CONNECTOR P1

	A	B	C	D	E
25			GND		
24			GND		
22			GND		
21			GND		
20			GND		
19			GND		
18			GND		
17	GND	GND	GND	GND	GND
16			GND		
15			GND		
14	GND	GND	GND	GND	GND
13			GND		
12			GND		
11			GND		
10	GND	GND	GND	GND	GND
9			GND		
8			GND		
7			GND		
6	GND	GND	GND	GND	GND
5			GND		
4			GND		
3			GND		
2	GND	GND	GND	GND	GND
1	-12V	-12V	GND	+12V	+12V

RIGHT HAND INSERTION INTO BACKPLANE
PINOUT AS VIEWED FROM BOARD COMPONENT SIDE

CONNECTOR P1

	E	D	C	B	A
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					

CONNECTOR P2

	A	B	C	D	E
25					
24					
22					
21					
20					
19					
18					
17					
16					
15					

	A	B	C	D	E
11					
10					
9					
8					
7					
6					
5					
4					
3					
2					
1					

	E	D	C	B	A
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					

	E	D	C	B	A
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					

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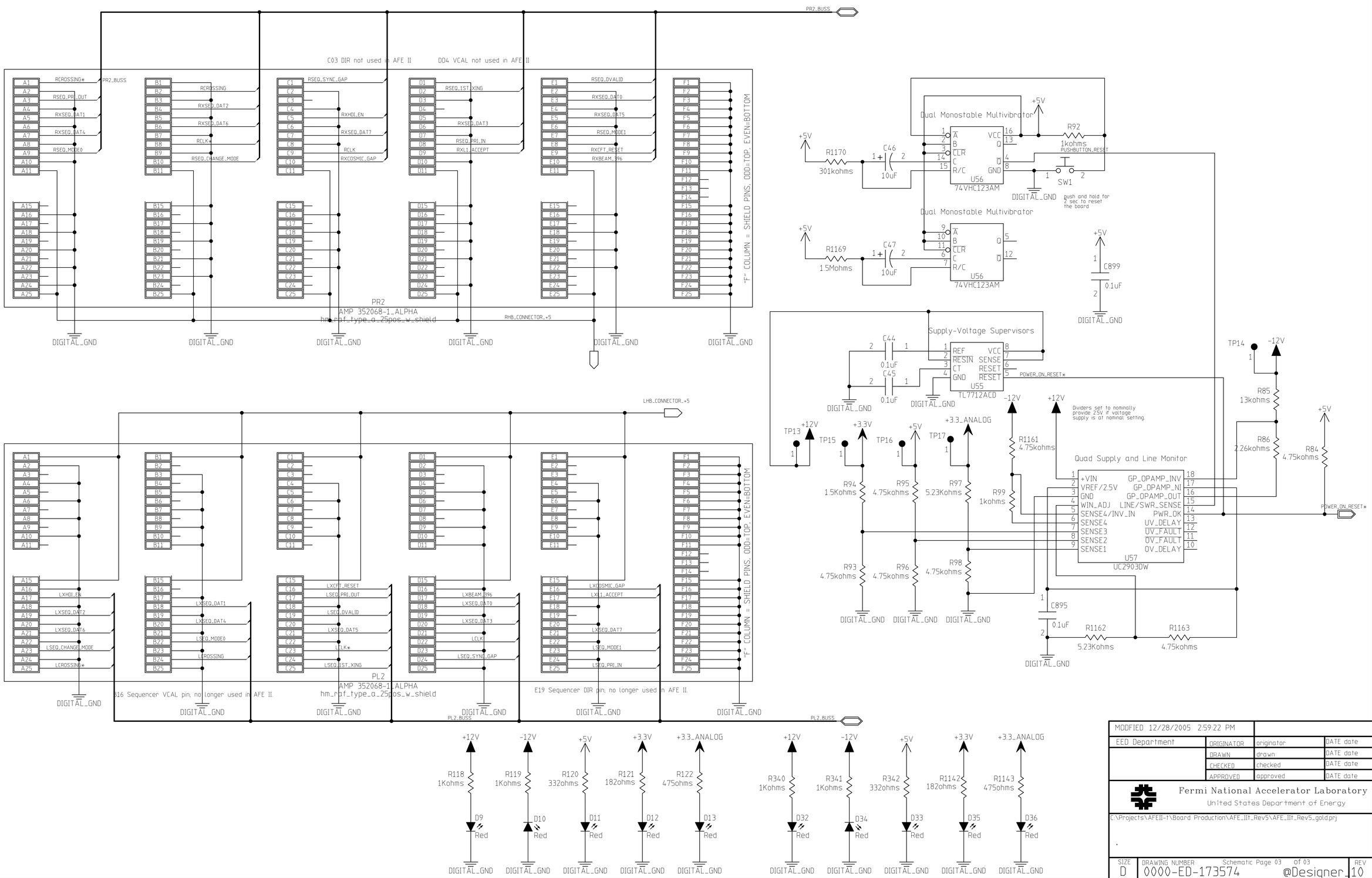
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H:8ND, V:4LA


PR2_BUSS
C03 DIR not used in AFE II
D04 VCAL not used in AFE II
RCROSSING*
RSEQ_PRI_OUT
RXSEQ_DAT1
RXSEQ_DAT4
RSEQ_MODE0
RCROSSING
RXSED_DAT2
RXSED_DAT6
RCLK*
RSEQ_CHANGE_MODE
RSEQ_SYNC_GAP
RXHDI_EN
RXSEQ_DAT7
RCLK
RXCOSMIC_GAP
RSEQ_1ST_XING
RXSEQ_DAT3
RSEQ_PRI_IN
RXL1_ACCEPT
RSEQ_DVALID
RXSEQ_DAT0
RXSEQ_DAT5
RSEQ_MODE1
RXCFT_RESET
RXBEAM_396
"F" COLUMN = SHIELD PINS, ODD=TOP, EVEN=BOTTOM
PR2
AMP 352068-1_ALPHA
hm_raf_type_a_25pos_w_shield
RHB_CONNECTOR_+5
DIGITAL_GND
Dual Monostable Multivibrator
74VHC123AM
U56
R1170
301kohms
C46
10uF
R92
1kohms
PUSHBUTTON_RESET
SW1
push and hold for 2 sec to reset the board
R1169
1.5Mohms
C47
C899
0.1uF
Supply-Voltage Supervisors
TL7712ACD
U55
C44
C45
POWER_ON_RESET*
TP14
-12V
R85
13kohms
R86
2.26kohms
R84
4.75kohms
TP13
TP15
TP16
TP17
+3.3_ANALOG
R1161
4.75kohms
Dividers set to nominally provide 2.5V if voltage supply is at nominal setting.
Quad Supply and Line Monitor
UC2903DW
U57
+VIN
VREF/2.5V
GND
WIN_ADJ
SENSE4/INV_IN
SENSE4
SENSE3
SENSE2
SENSE1
GP_OPAMP_INV
GP_OPAMP_NI
GP_OPAMP_OUT
LINE/SWR_SENSE
PWR_OK
UV_DELAY
UV_FAULT
OV_FAULT
OV_DELAY
R94
1.5Kohms
R95
4.75kohms
R97
5.23Kohms
R99
1kohms
R93
4.75kohms
R96
4.75kohms
R98
4.75kohms
C895
R1162
5.23Kohms
R1163
4.75kohms
LHB_CONNECTOR_+5
PL2
AMP 352068-1_ALPHA
hm_raf_type_a_25pos_w_shield
LXCFT_RESET
LSEQ_PRI_OUT
LSEQ_DVALID
LXSEQ_DAT5
LCLK*
LSEQ_1ST_XING
LXCOSMIC_GAP
LXL1_ACCEPT
LXSEQ_DAT7
LSEQ_MODE1
LSEQ_PRI_IN
LXHDI_EN
LXSEQ_DAT2
LXSEQ_DAT6
LSEQ_CHANGE_MODE
LCROSSING*
LXSEQ_DAT1
LXSEQ_DAT4
LSEQ_MODE0
LCROSSING
LXBEAM_396
LXSEQ_DAT0
LXSEQ_DAT3
LCLK
LSEQ_SYNC_GAP
B16 Sequencer VCAL pin, no longer used in AFE II.
E19 Sequencer DIR pin, no longer used in AFE II.
PL2_BUSS
+12V
-12V
+5V
+3.3V
+3.3_ANALOG
R118
1Kohms
R119
1Kohms
R120
332ohms
R121
182ohms
R122
475ohms
D9
D10
D11
D12
D13
Red
R340
1Kohms
R341
1Kohms
R342
332ohms
R1142
182ohms
R1143
475ohms
D32
D34
D33
D35
D36
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REV
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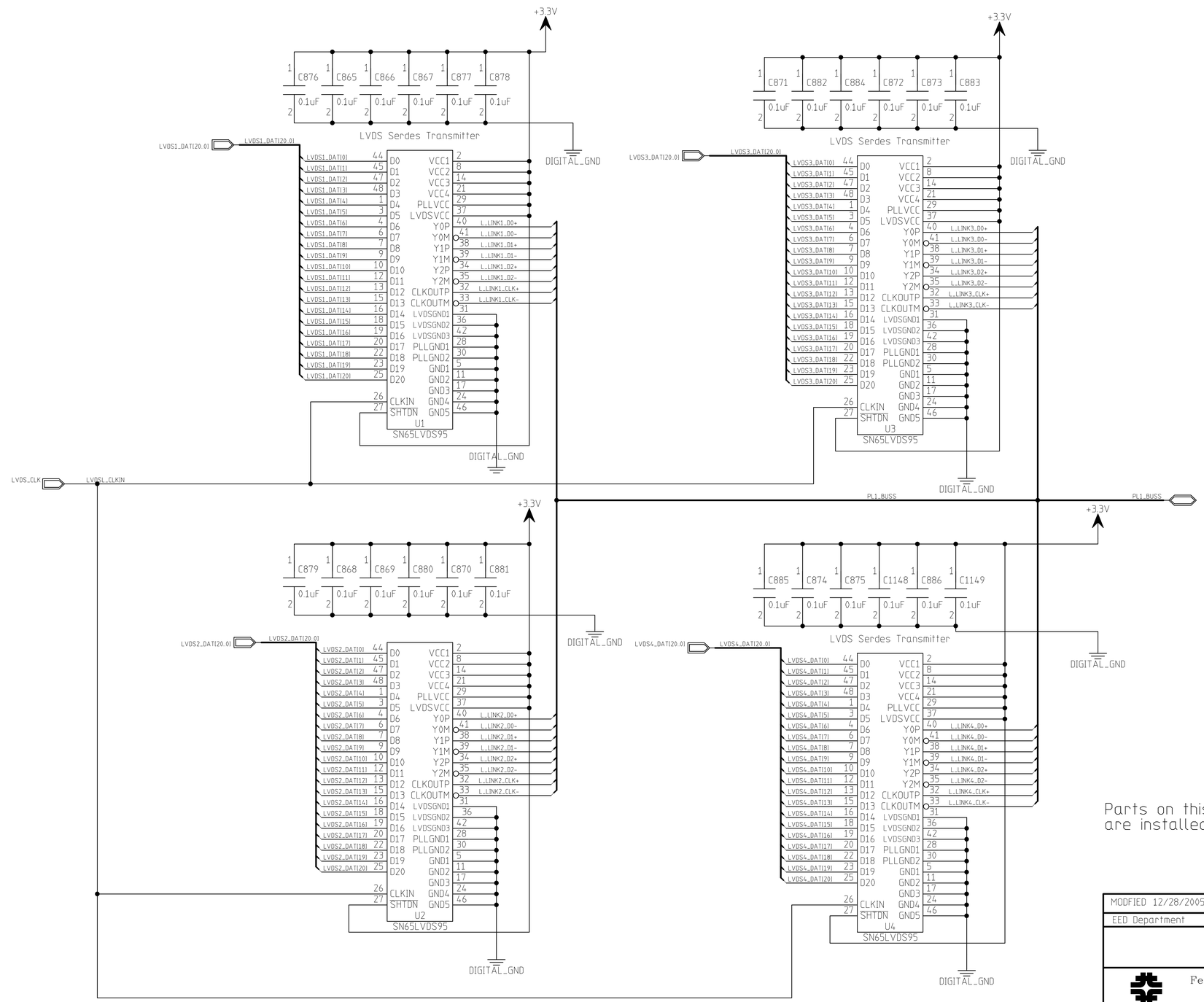

Parts on this page, if installed, are installed onto left-hand

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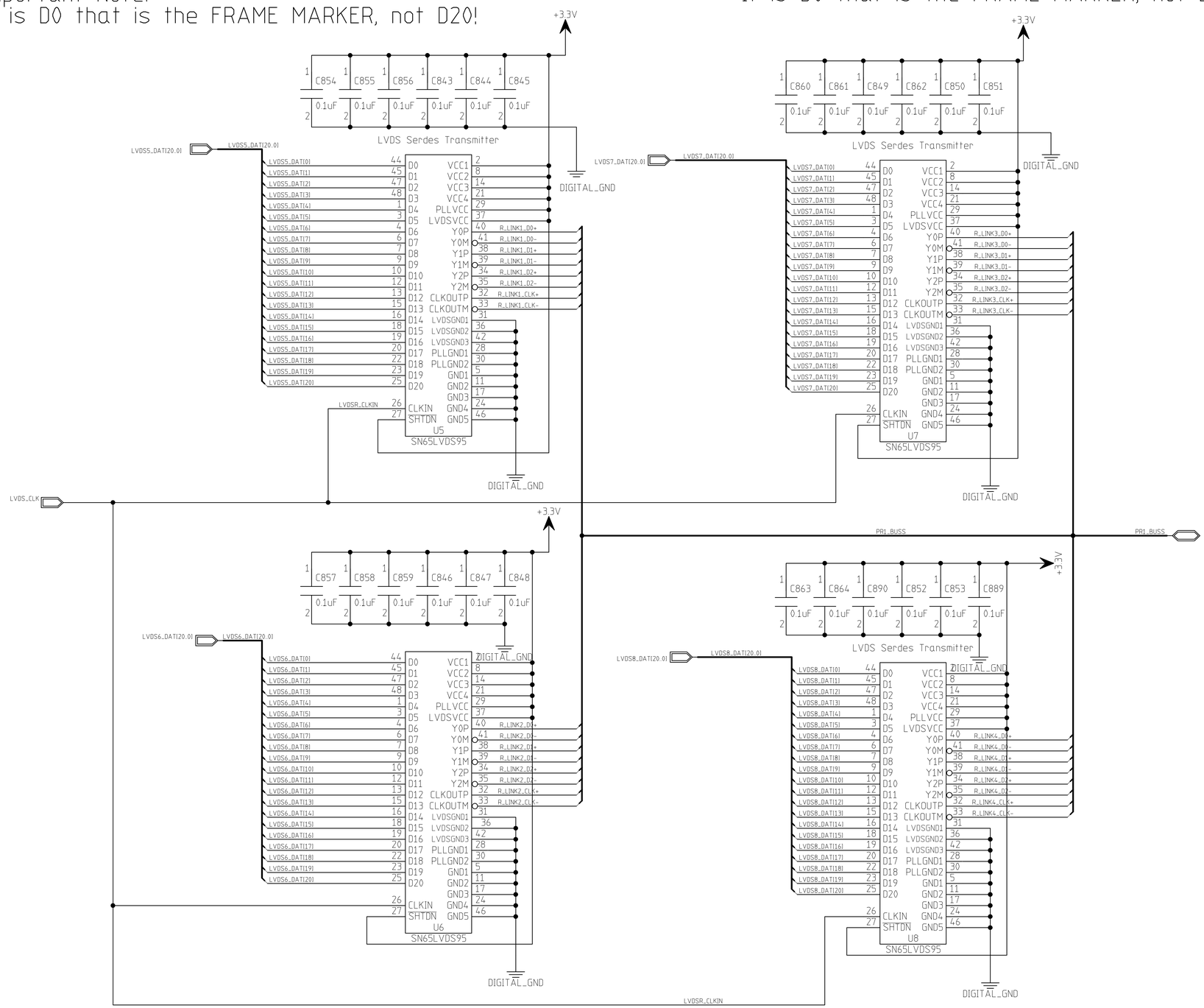
H=8ND, V=4LA

Important Note:
It is D0 that is the FRAME MARKER, not D20!

Important Note:
It is D0 that is the FRAME MARKER, not D20!



MODIFIED 12/28/2005 2:59:20 PM			
EED Department	ORIGINATOR	originator	DATE date
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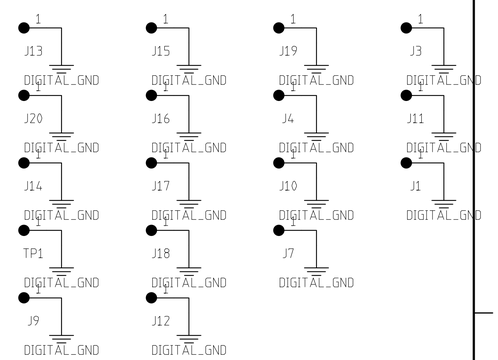

MODFIED 3/15/2006 7:45:42 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
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.

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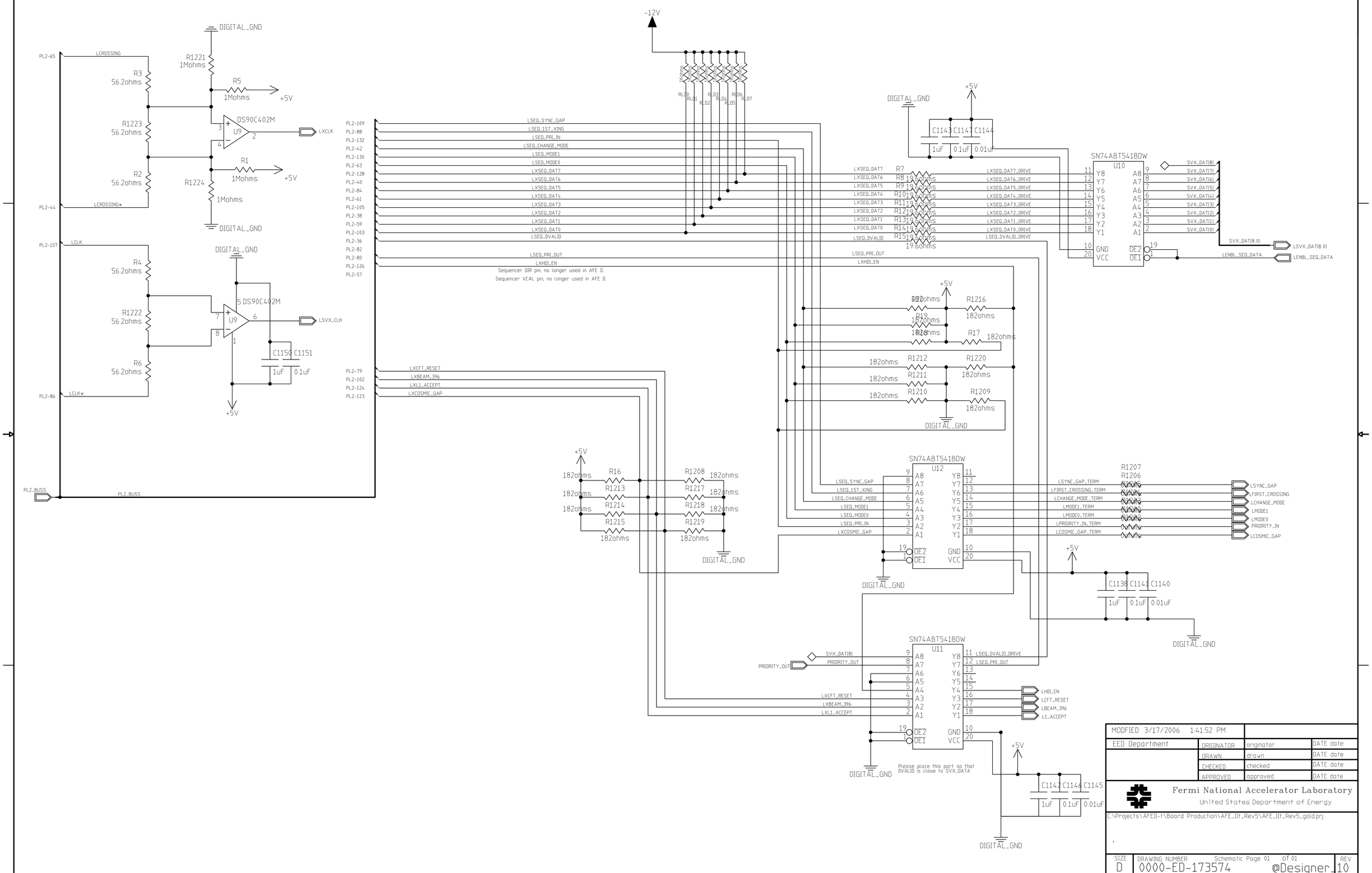
H=8ND, V=4LA



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EED Department	ORIGINATOR	originator	DATE date
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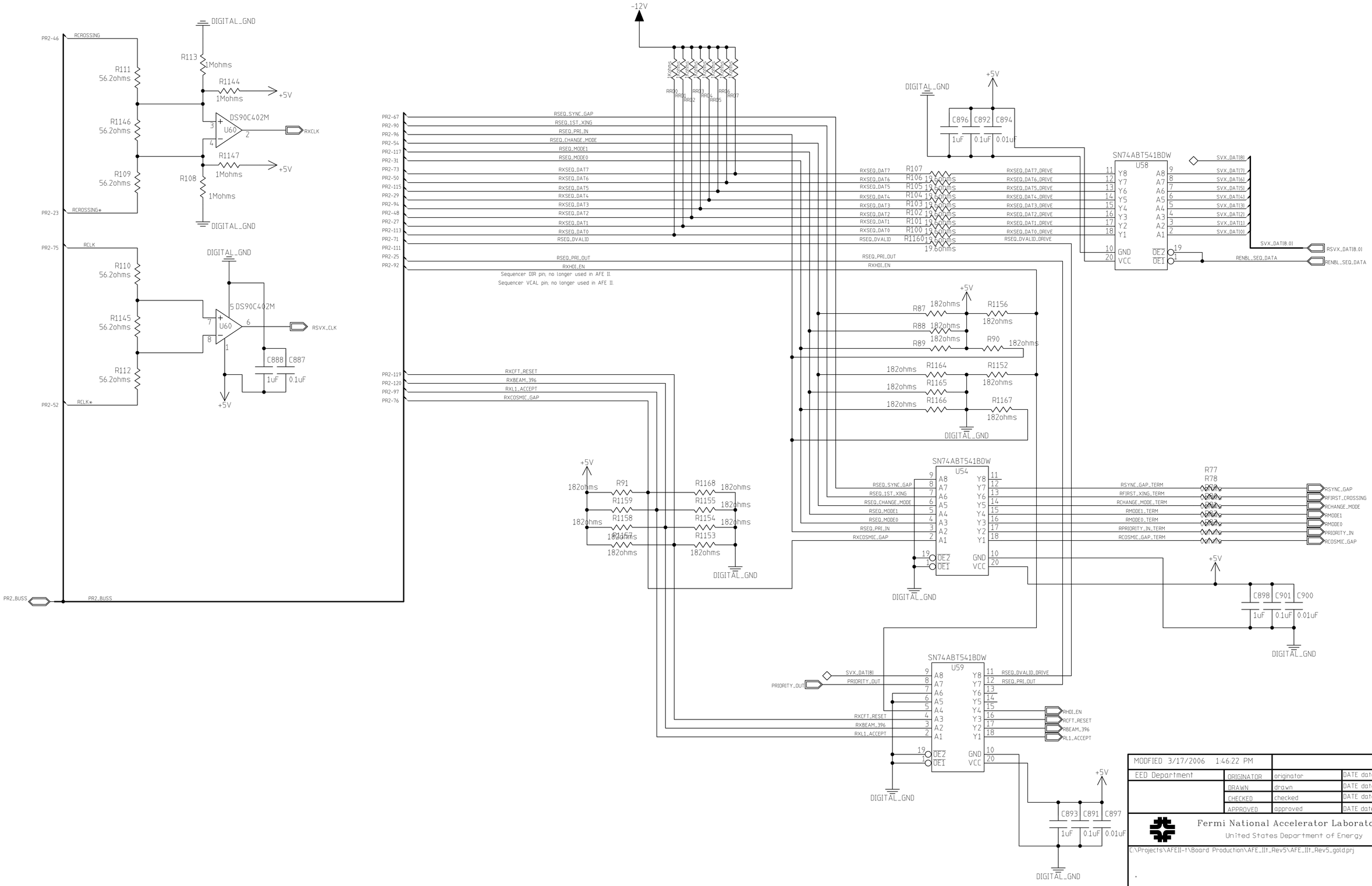
D	0000-ED-173574	@Designer_10	

H=8ND, V=4LA



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EED Department	ORIGINATOR	originator	DATE date
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	APPROVED	approved	DATE date

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United States Department of Energy

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