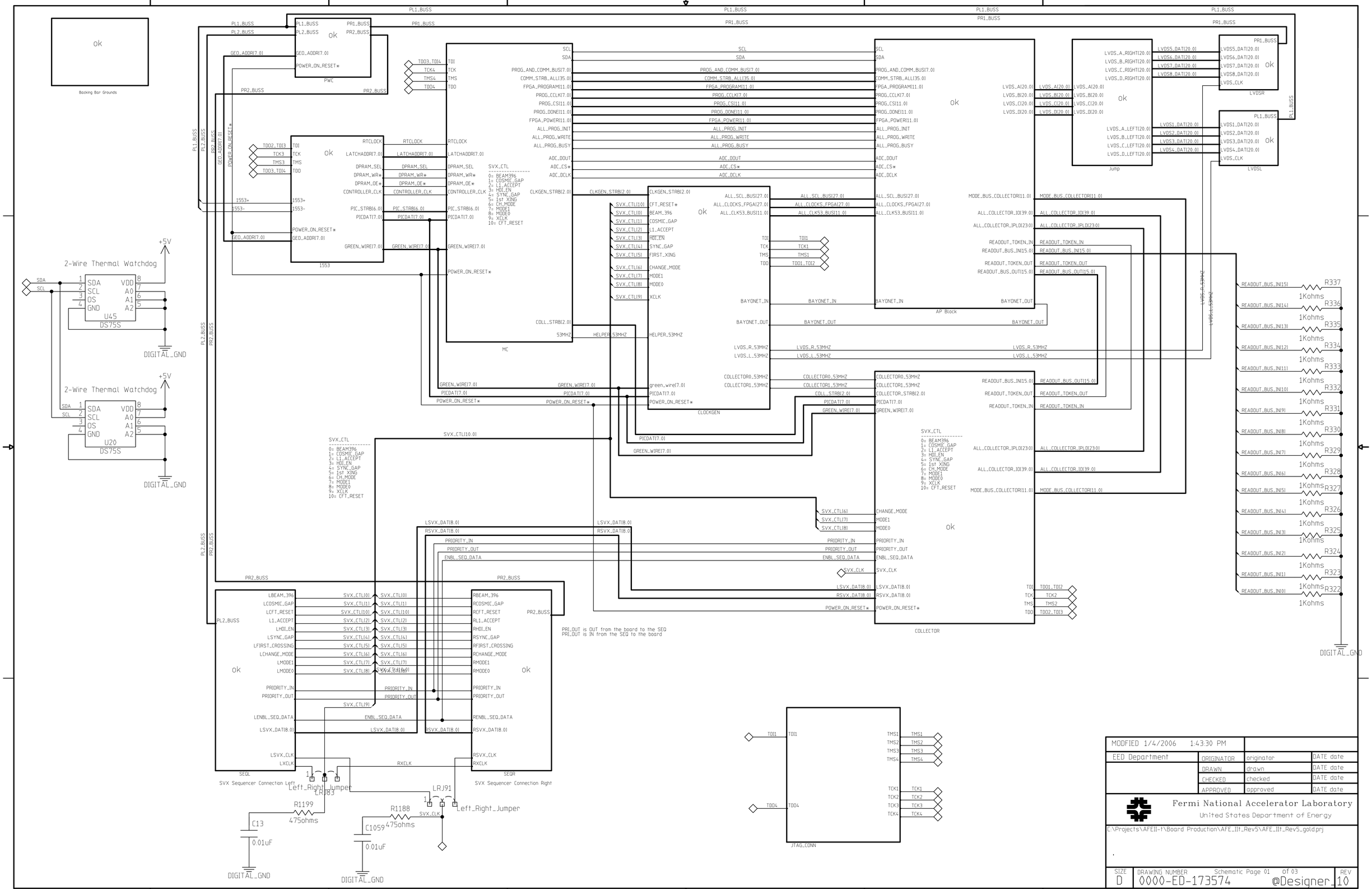

MODIFIED 1/4/2006 1:43:30 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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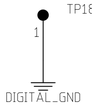
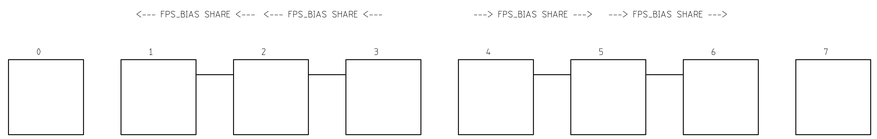
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer	10

H:8ND, V:4LA

Comments go here





Left to right:
CLOCKGEN
COLLECTOR
1553
HELPER

MODFIED 1/4/2006 1:43:30 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_1	0

H=8ND, V=4LA

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EED Department	ORIGINATOR	originator	DATE date
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	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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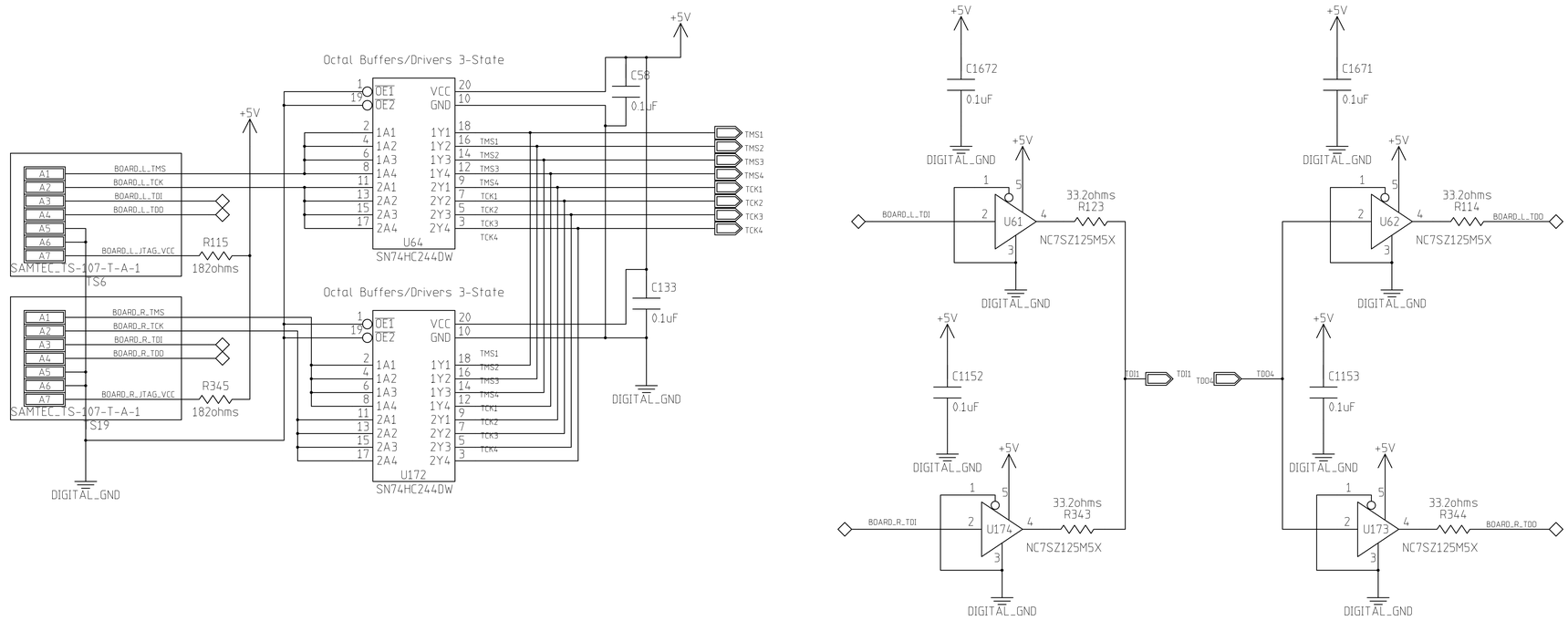
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 03 of 03 @Designer_1	0

H=8ND, V=4LA



MODFIED 12/28/2005 2:50:32 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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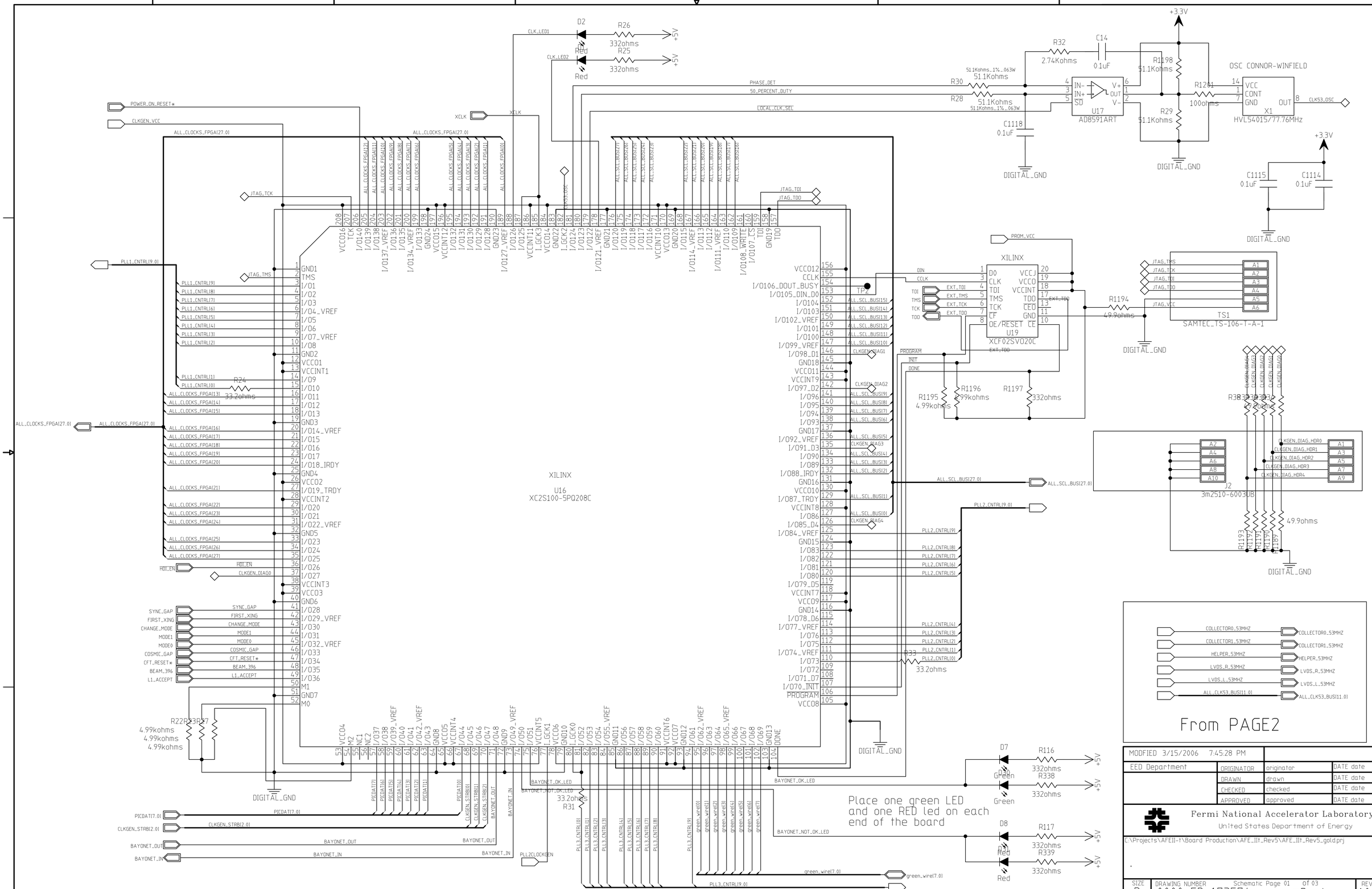
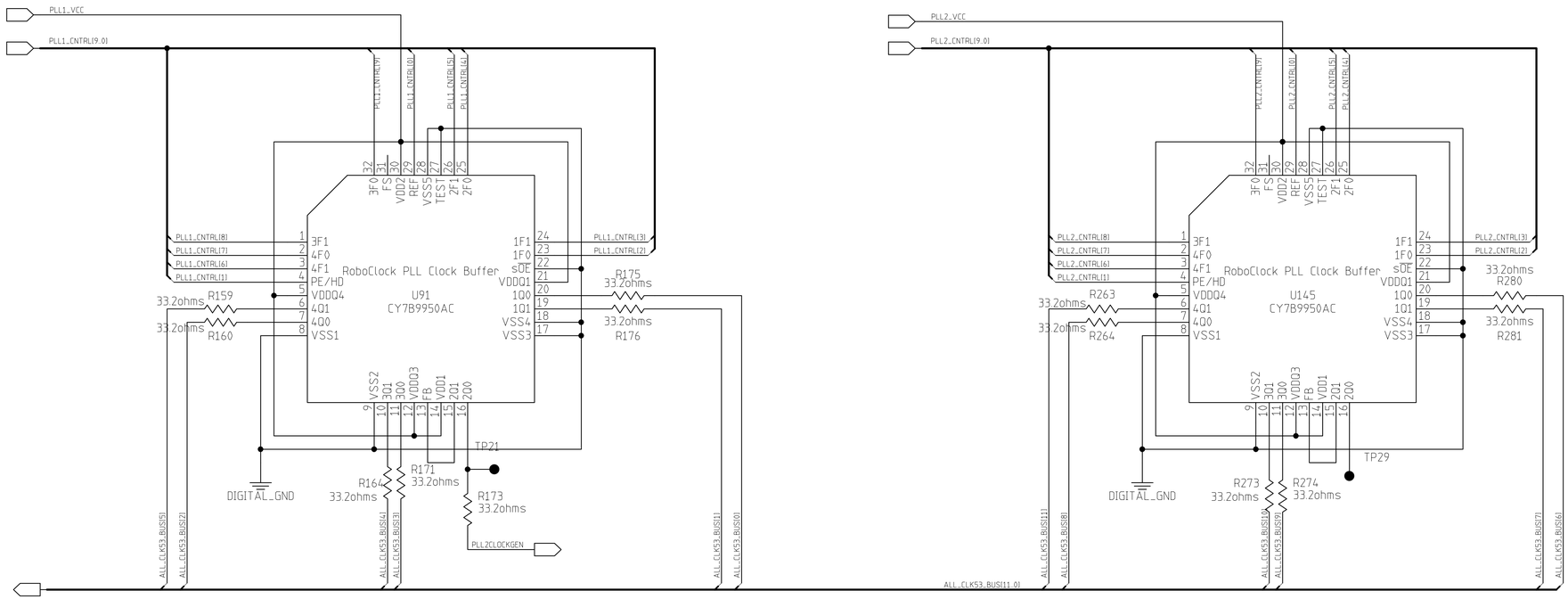
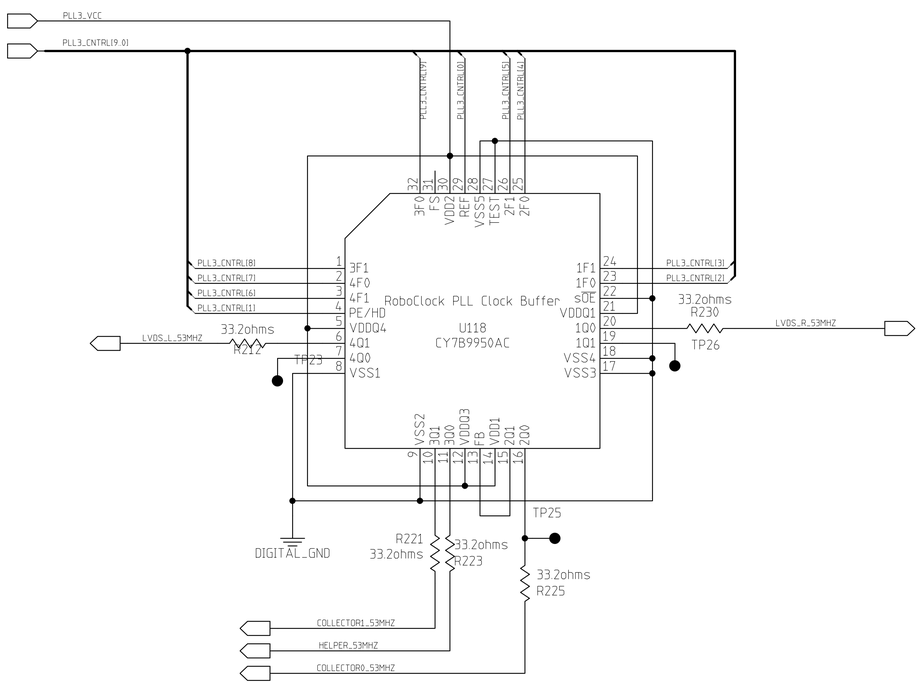
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H:8ND, V:4LA


XILINX
U16
XC2S100-5PQ208C
XILINX
U19
XCF02SVO20C
OSC CONNOR-WINFIELD
X1
HVL54015/77.76MHz
U17
AD8591ART
SAMTEC_TS-106-1-A-1
TS1
3M2510-6003UB
J2
From PAGE2
Place one green LED and one RED led on each end of the board
DIGITAL_GND
+3.3V
+5V
MODIFIED 3/15/2006 7:45.28 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-1\Board Production\AFE_II1_Rev5\AFE_II1_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV





ALL_CLK53_BUS[11..0]

0 = AFPGA0 CLK53
1 = AFPGA1 CLK53
2 = DFPGA01 CLK53
3 = AFPGA2 CLK53
4 = AFPGA3 CLK53
5 = DFPGA23 CLK53
6 = AFPGA4 CLK53
7 = AFPGA5 CLK53
8 = DFPGA45 CLK53
9 = AFPGA6 CLK53
10 = AFPGA7 CLK53
11 = DFPGA67 CLK53

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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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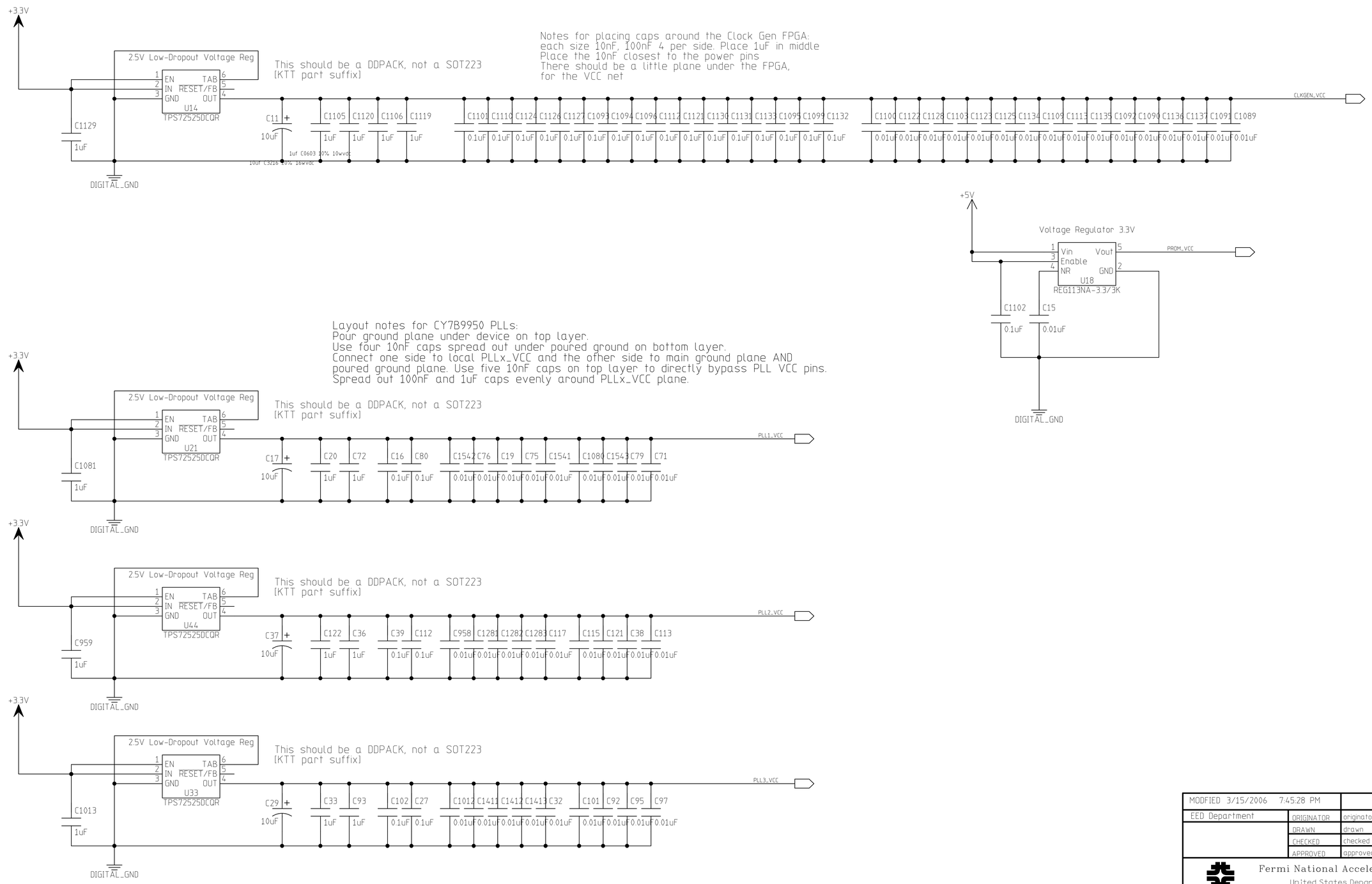
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_	10

H:8ND, V:4LA



MODFIED 3/15/2006 7:45:28 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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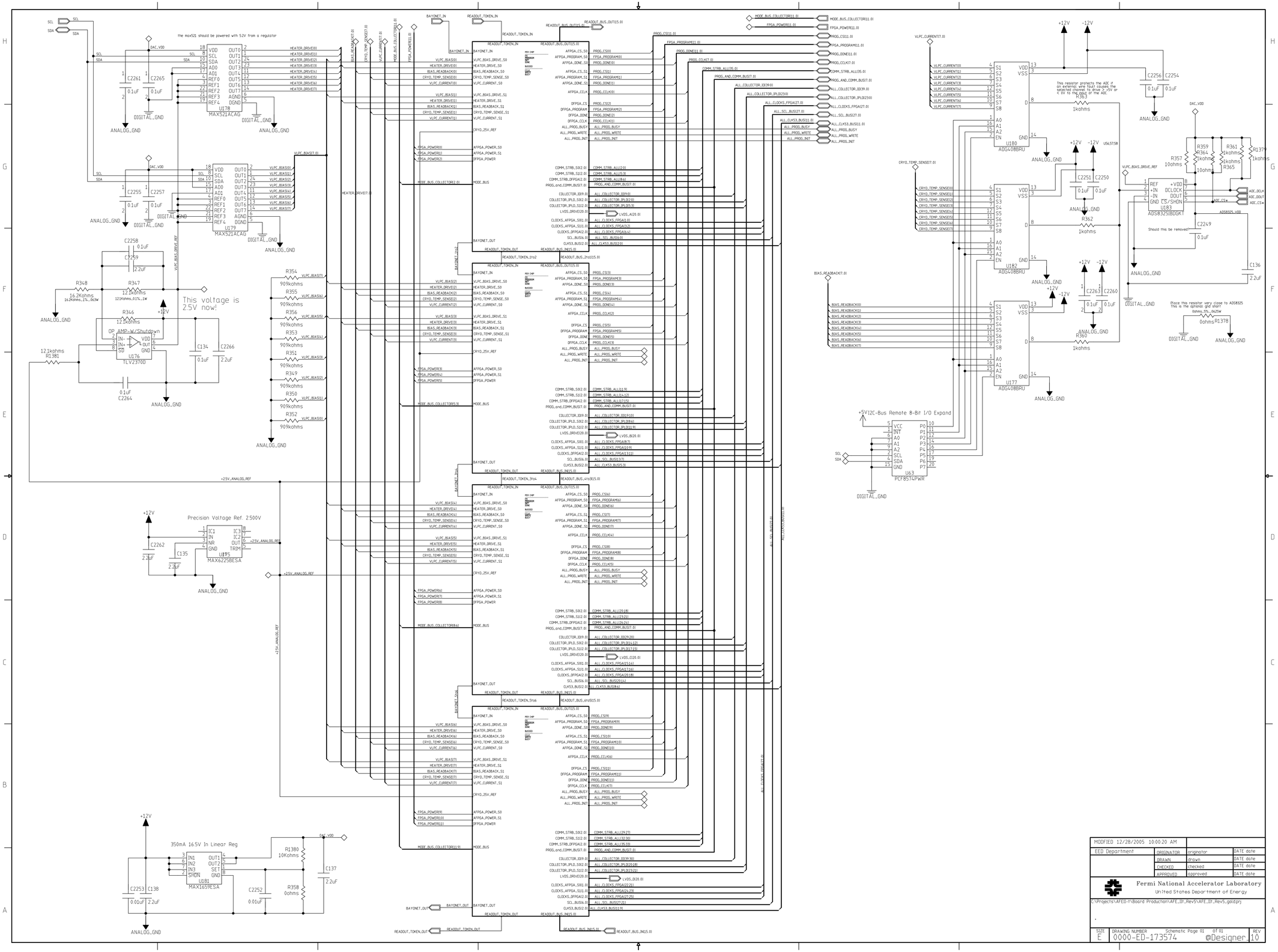
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 03 of 03 @Designer_10	

H=8ND, V=4LA


the max521 should be powered with 5.2V from a regulator
U178 MAX521ACAG
U179 MAX521ACAG
This voltage is 2.5V now!
U176 TLV2370D
Precision Voltage Ref. 2.500V
U175 MAX6225BESA
350mA 16.5V In Linear Reg
U181 MAX1659ESA
+5V I2C-Bus Remote 8-Bit I/O Expand
U63 PCF8574PWR
U180 ADG408BRU
U182 ADG408BRU
U177 ADG408BRU
U183 ADS8325IBDGKT
This resistor protects the ADC if an external wire fault causes the selected channel to drive >-5V or < 0V to the input of the ADC
Should this be removed?
Place this resistor very close to ADS8325 This is the optional gnd short
MODIFIED 12/28/2005 10:00:20 AM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
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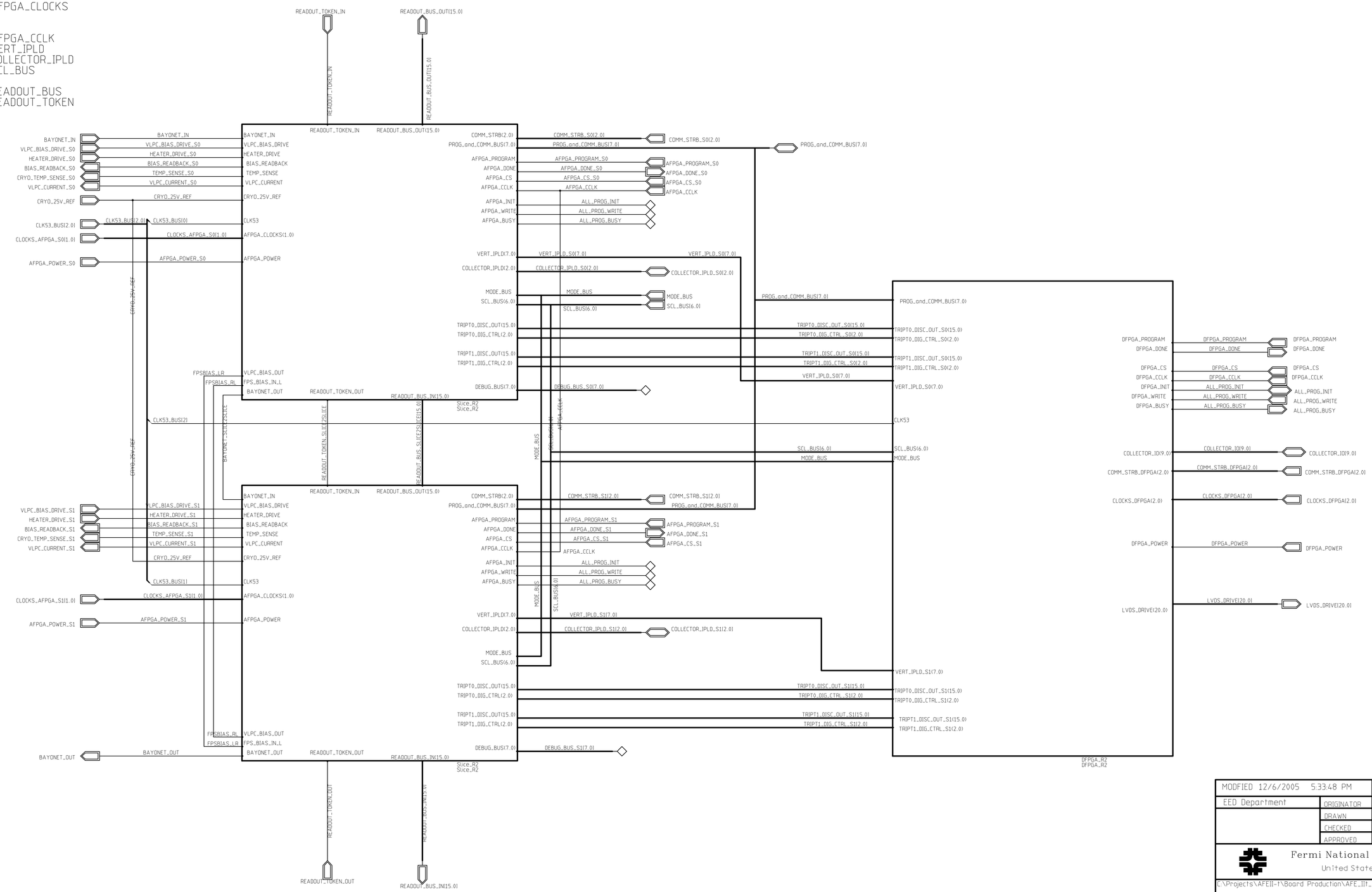
C:\Projects\AFEII-1\Board Production\AFE_III_Rev5\AFE_III_Rev5_gold.prj
SIZE E
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 01
REV @Designer_10

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



MODIFIED 12/6/2005 5:33:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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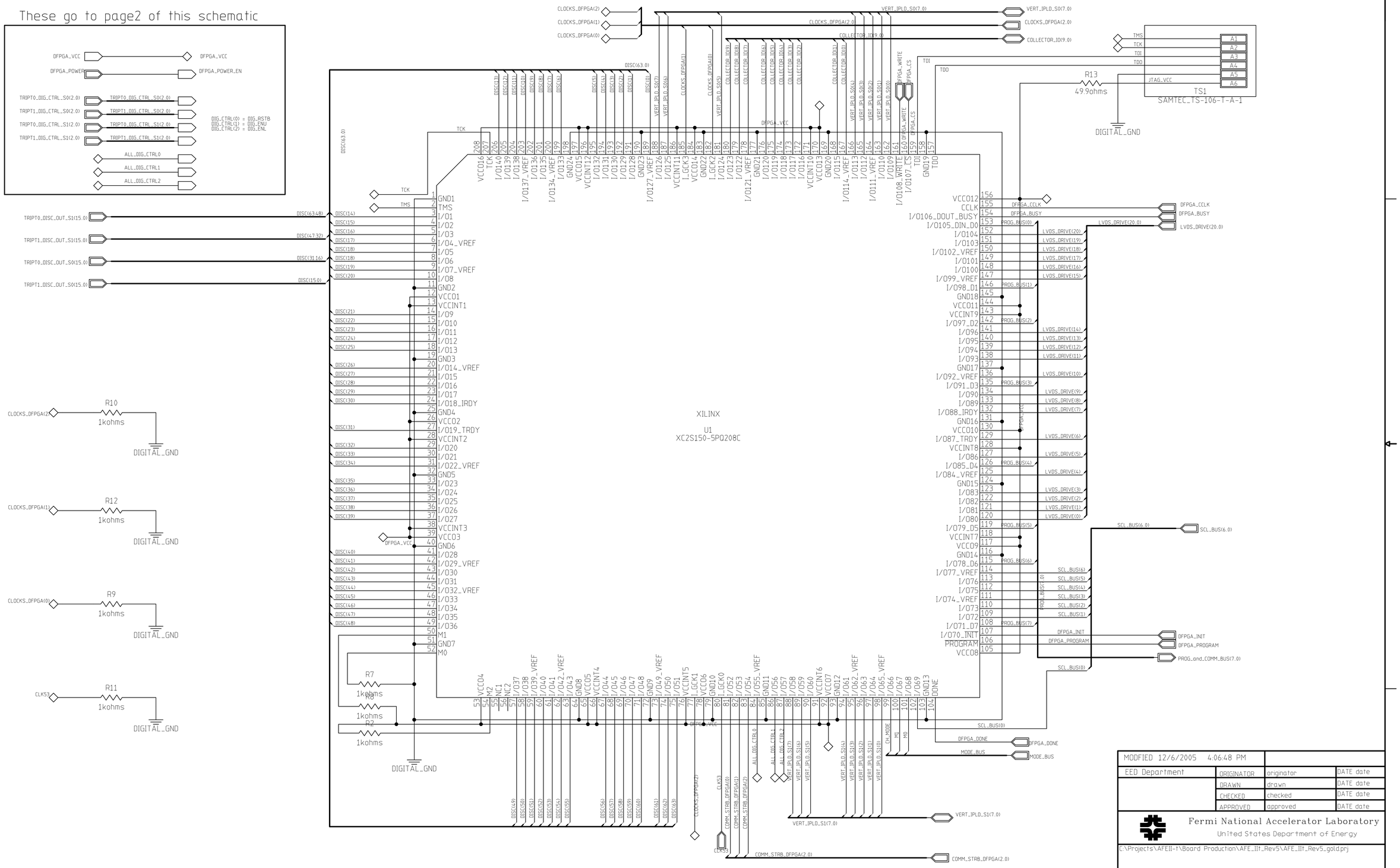
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	10

H:8ND, V:4LA



MODIFIED 12/6/2005 4:06:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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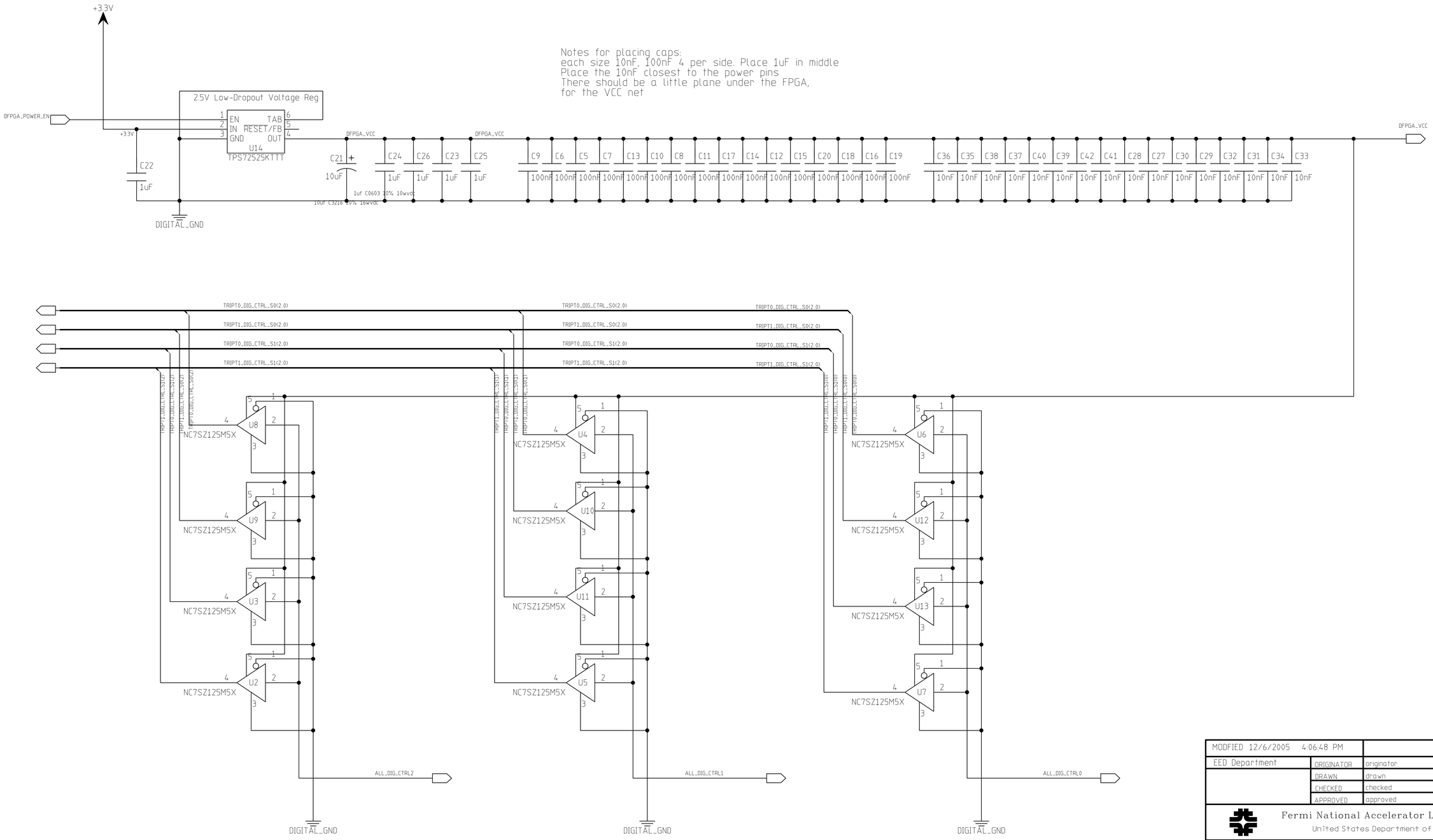
C:\Projects\AFEII-1\Board Production\AFE_II_Rev5\AFE_II_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_1	10

H:8ND, V:4LA



MODFIED 12/6/2005 4:06:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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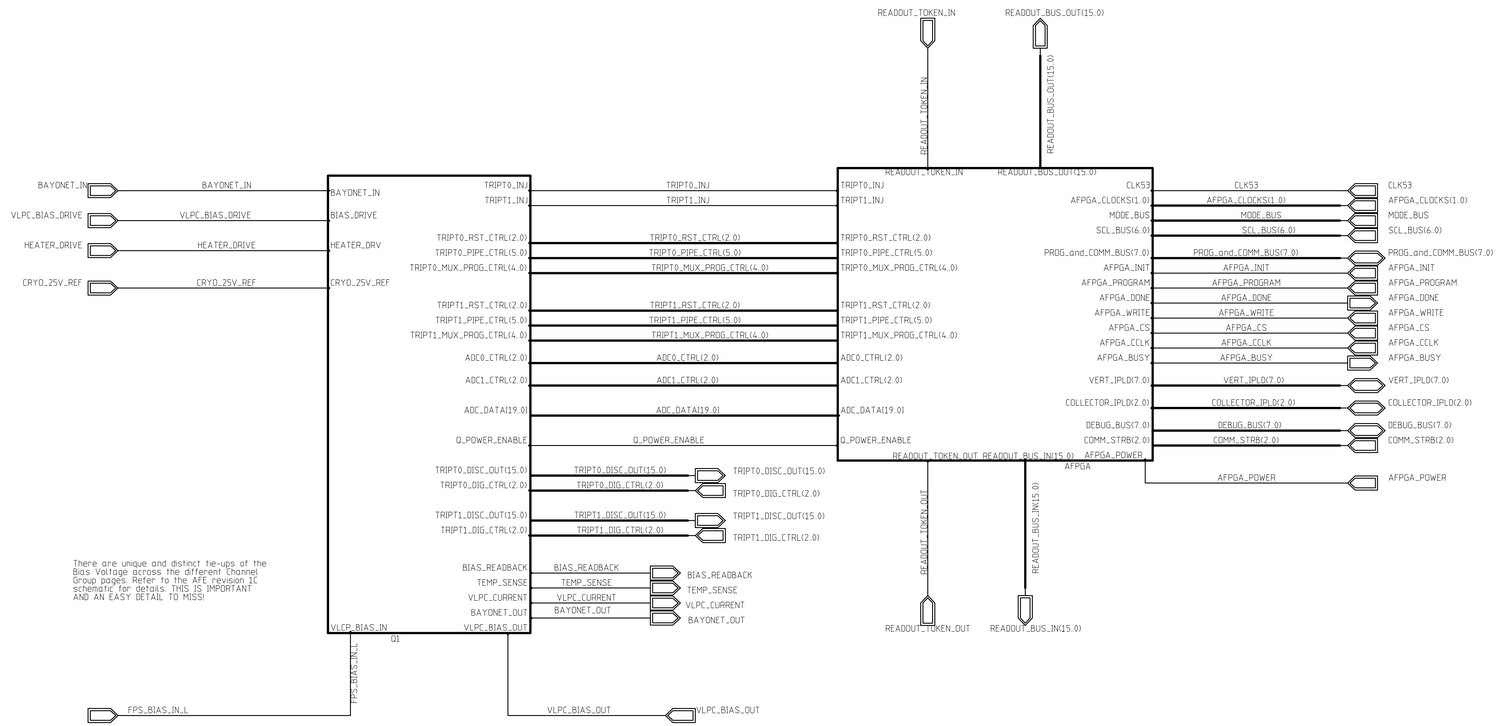
C:\Projects\AFEII-T\Board Production\AFE_II_Rev5\AFE_II_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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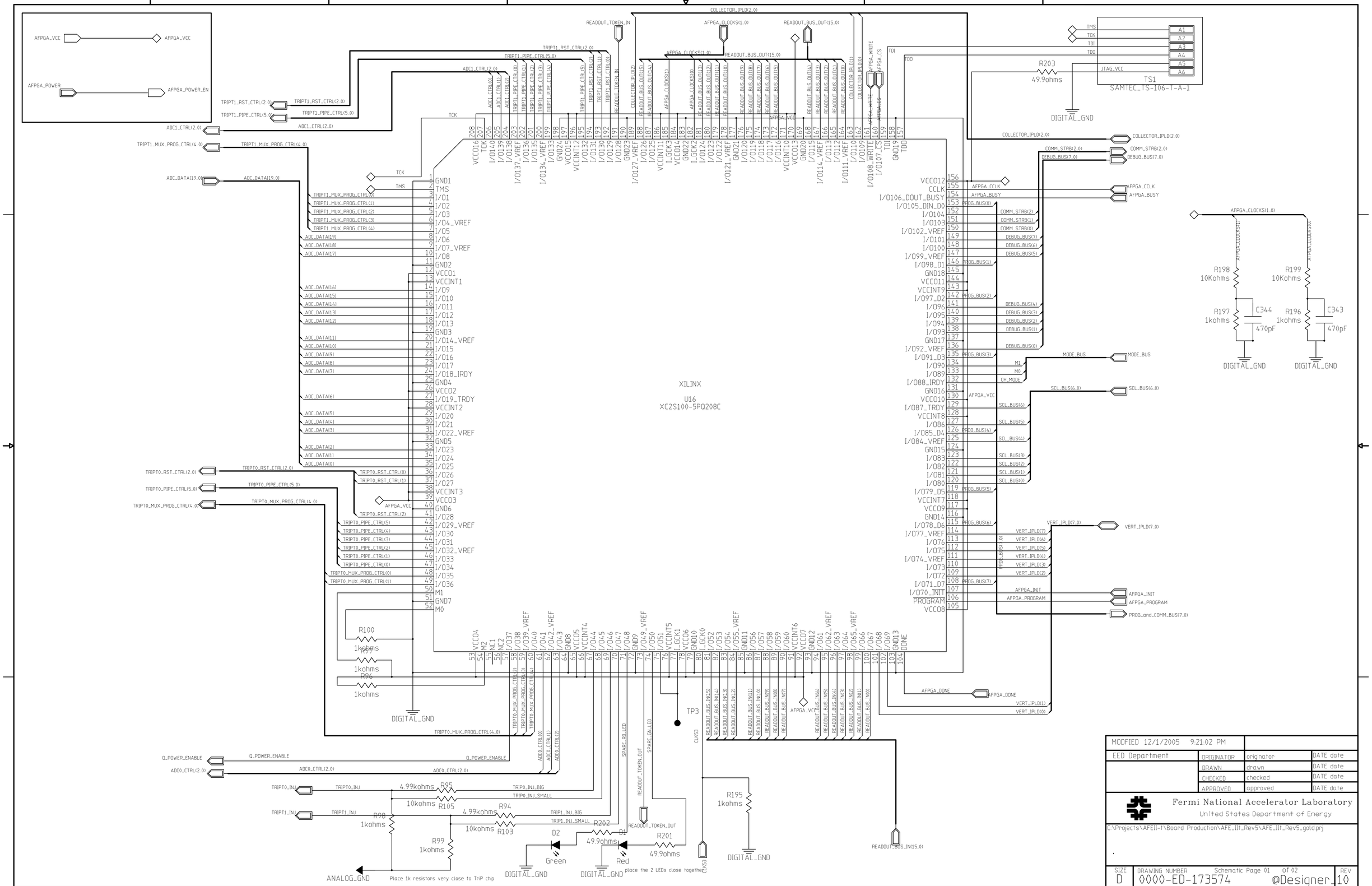
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA


XILINX
U16
XC2S100-5PQ208C
TS1
SAMTEC_TS-106-T-A-1
R203
49.9ohms
R198
10Kohms
R199
10Kohms
R197
1kohms
R196
1kohms
C344
470pF
C343
470pF
R100
1kohms
R97
1kohms
R96
1kohms
R95
4.99kohms
R105
10kohms
R94
4.99kohms
R103
10kohms
R98
1kohms
R99
1kohms
R202
49.9ohms
R201
49.9ohms
R195
1kohms
D1
Red
D2
Green
TP3
DIGITAL_GND
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
EED Department
ORIGINATOR
DRAWN
CHECKED
APPROVED
Fermi National Accelerator Laboratory
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SIZE
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DRAWING NUMBER
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Schematic Page 01 of 02
@Designer
REV
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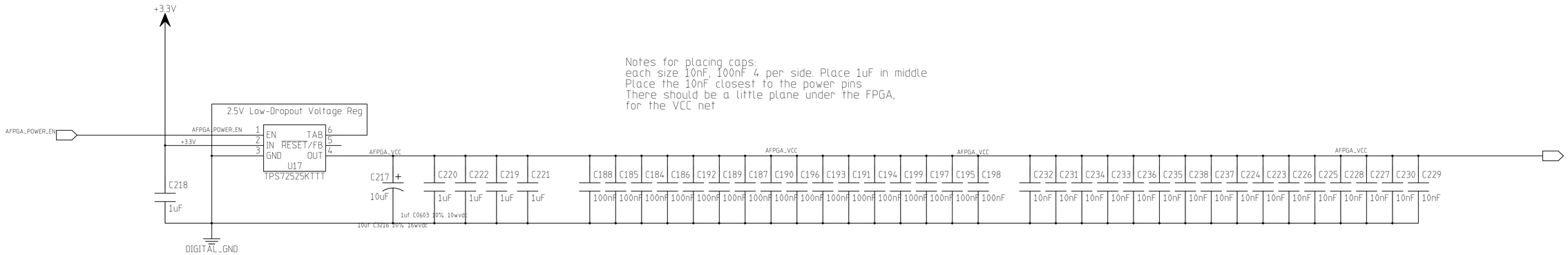

Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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	APPROVED	approved	DATE date

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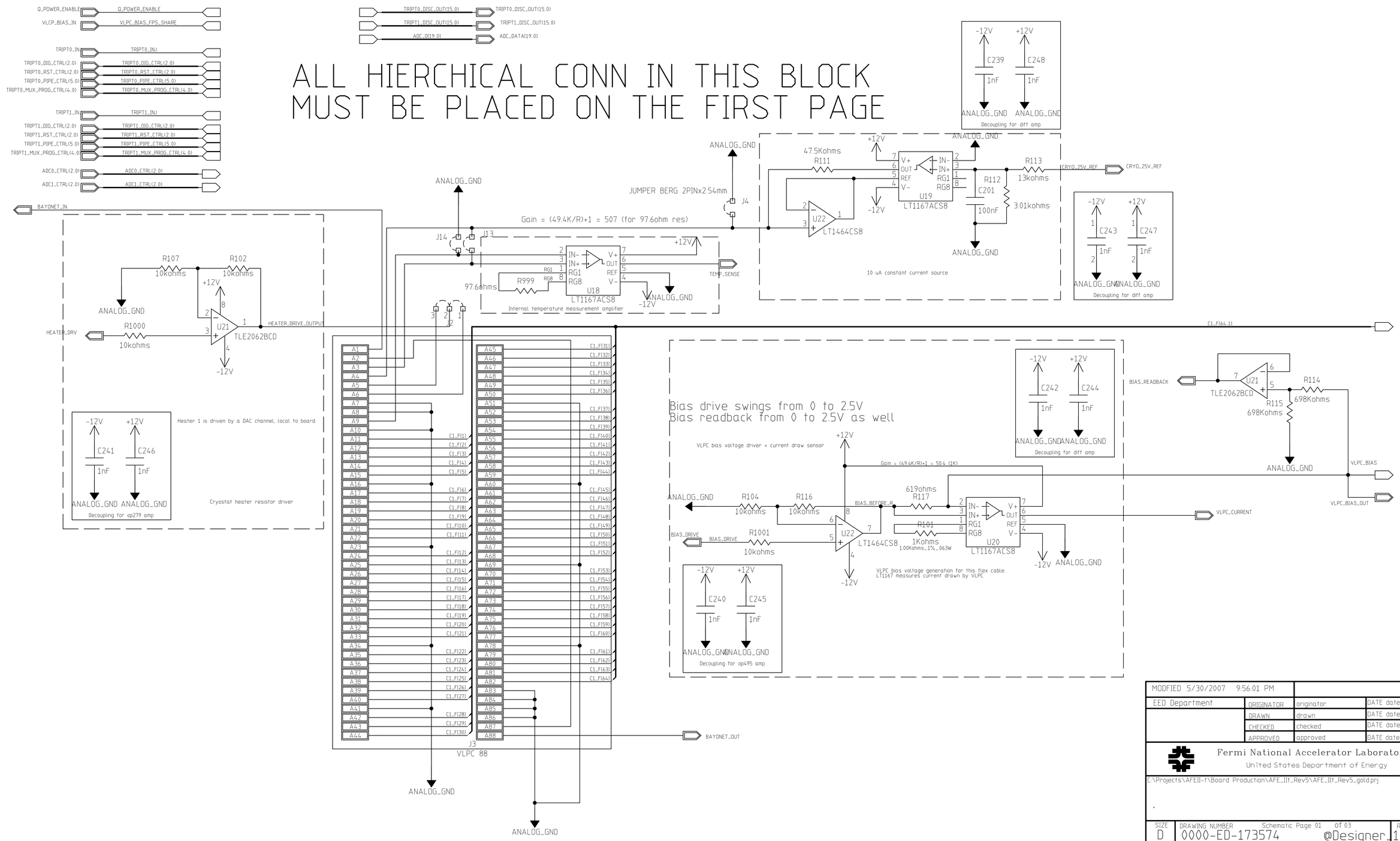
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H:8ND, V:4LA


ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
BAYONET_IN
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DATA(19.0)
ANALOG_GND
R107
10kohms
R102
10kohms
+12V
U21
TLE2062BCD
HEATER_DRIVE_OUTPUT
HEATER_DRV
R1000
10kohms
-12V
C241
C246
1nF
Heater 1 is driven by a DAC channel, local to board
Cryostat heater resistor driver
Decoupling for op279 amp
J14
J13
J2
J3
VLPC 88
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
JUMPER BERG 2PINx2.54mm
J4
97.6ohms
R999
U18
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
47.5Kohms
R111
U22
LT1464CS8
U19
LT1167ACS8
R112
C201
100nF
R113
13kohms
3.01kohms
CRYO_25V_REF
10 uA constant current source
C239
C248
Decoupling for diff amp
C243
C247
C1_FI64.1
BAYONET_OUT
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R104
10kohms
R116
10kohms
BIAS_BEFORE_R
619ohms
R117
R101
1Kohms
1.00Kohms_1%_.063W
R1001
10kohms
BIAS_DRIVE
U20
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
VLPC_CURRENT
C240
C245
Decoupling for op495 amp
C242
C244
BIAS_READBACK
R114
698Kohms
R115
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
MODFIED 5/30/2007 9:56:01 PM
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ORIGINATOR
DRAWN
CHECKED
APPROVED
originator
drawn
checked
approved
DATE date
Fermi National Accelerator Laboratory
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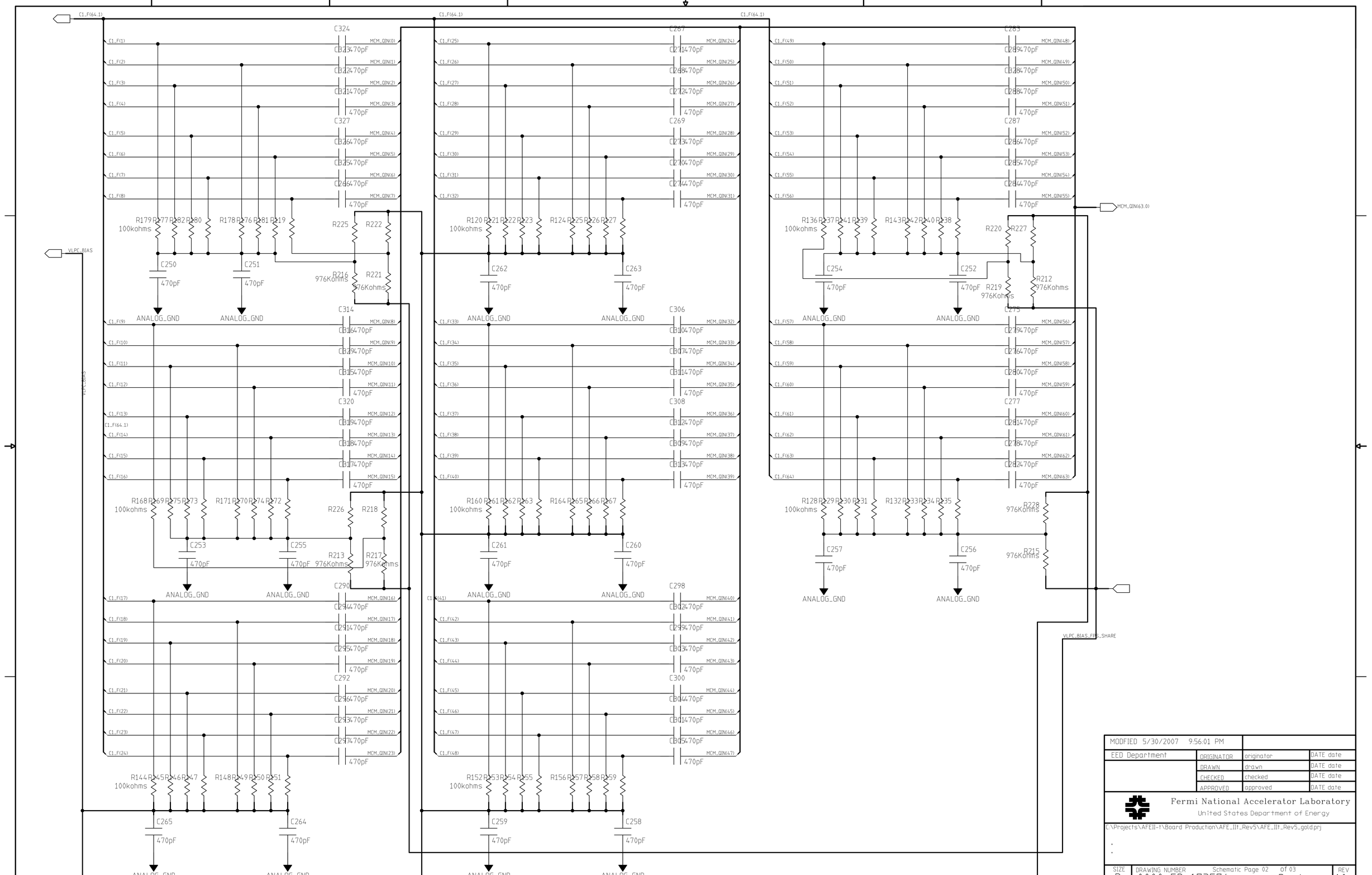
DRAWING NUMBER
0000-ED-173574
Schematic Page 01 of 03
@Designer_1
REV
0
H:8ND, V:4LA


C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
R179 R177 R182 R180 R178 R176 R181 R219 R225 R222 R216 R221
100kohms
976Kohms
R120 R121 R122 R123 R124 R125 R126 R127
R136 R137 R141 R139 R143 R142 R140 R138 R220 R227 R212 R219
R168 R169 R175 R173 R171 R170 R174 R172 R226 R218 R213 R217
R160 R161 R162 R163 R164 R165 R166 R167
R128 R129 R130 R131 R132 R133 R134 R135 R228 R215
R144 R145 R146 R147 R148 R149 R150 R151
R152 R153 R154 R155 R156 R157 R158 R159
470pF
MODFIED 5/30/2007 9:56:01 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
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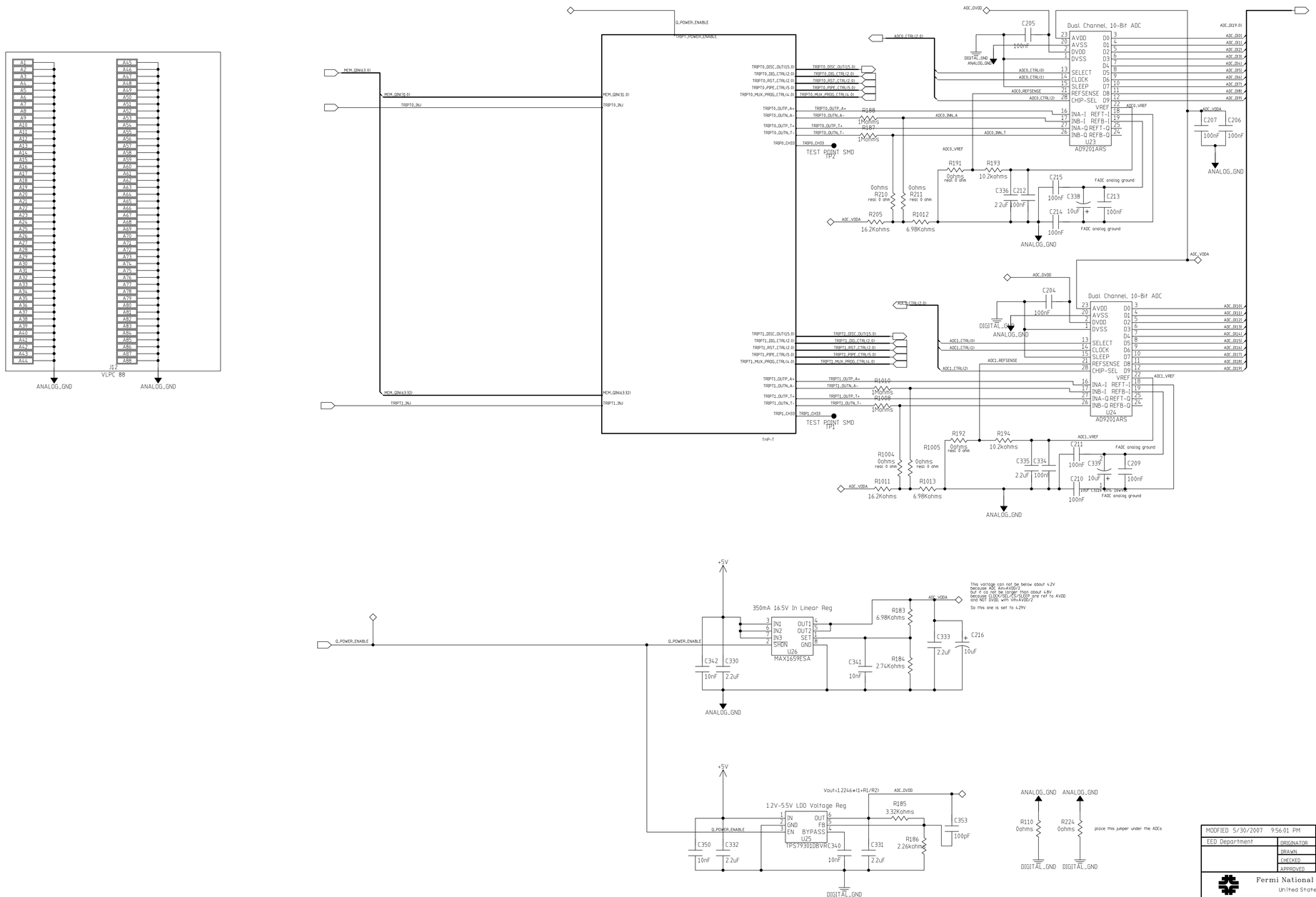
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H=8ND, V=4LA



MODIFIED 5/30/2007 9:56:01 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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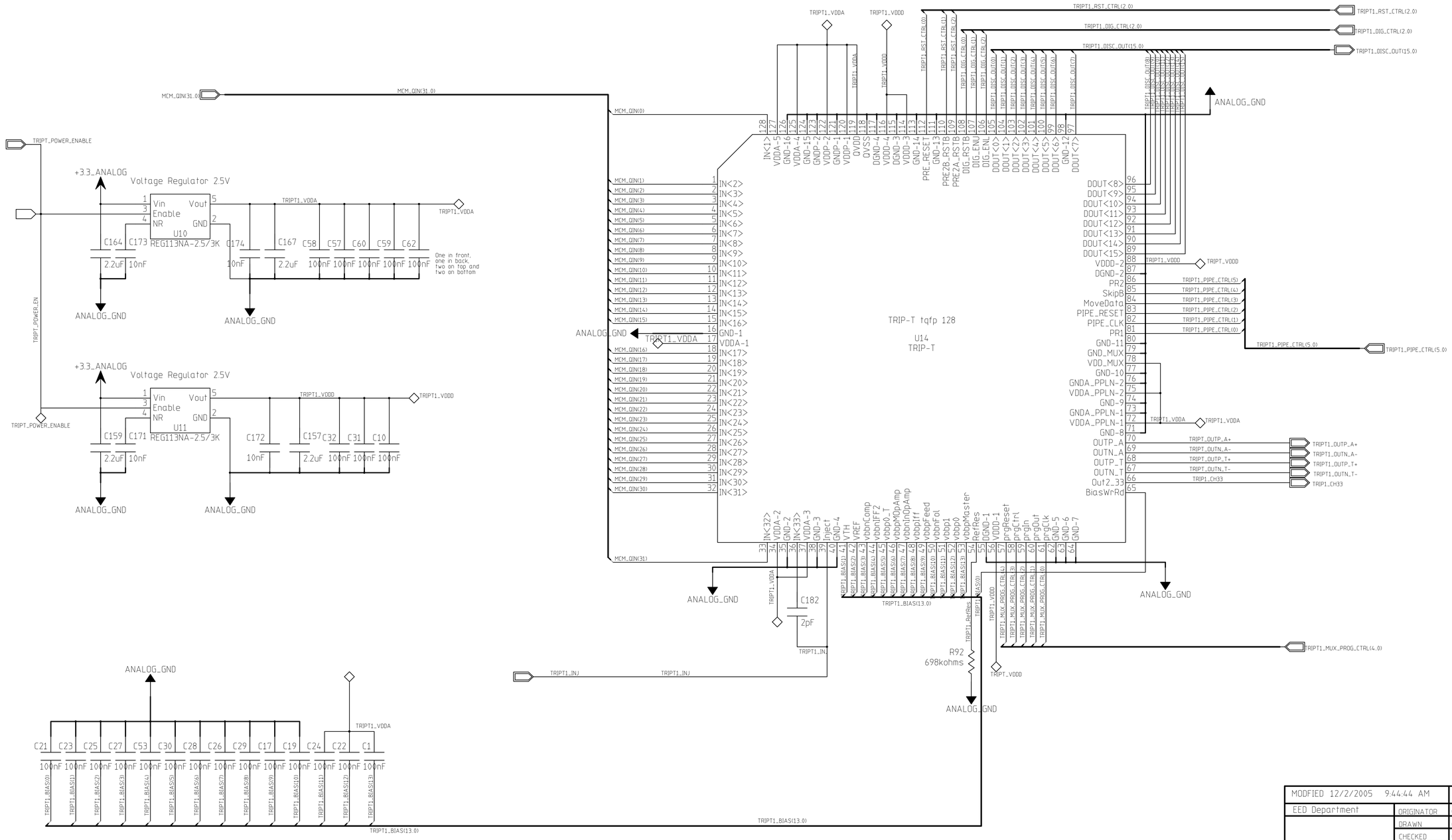
HoBND V=BLA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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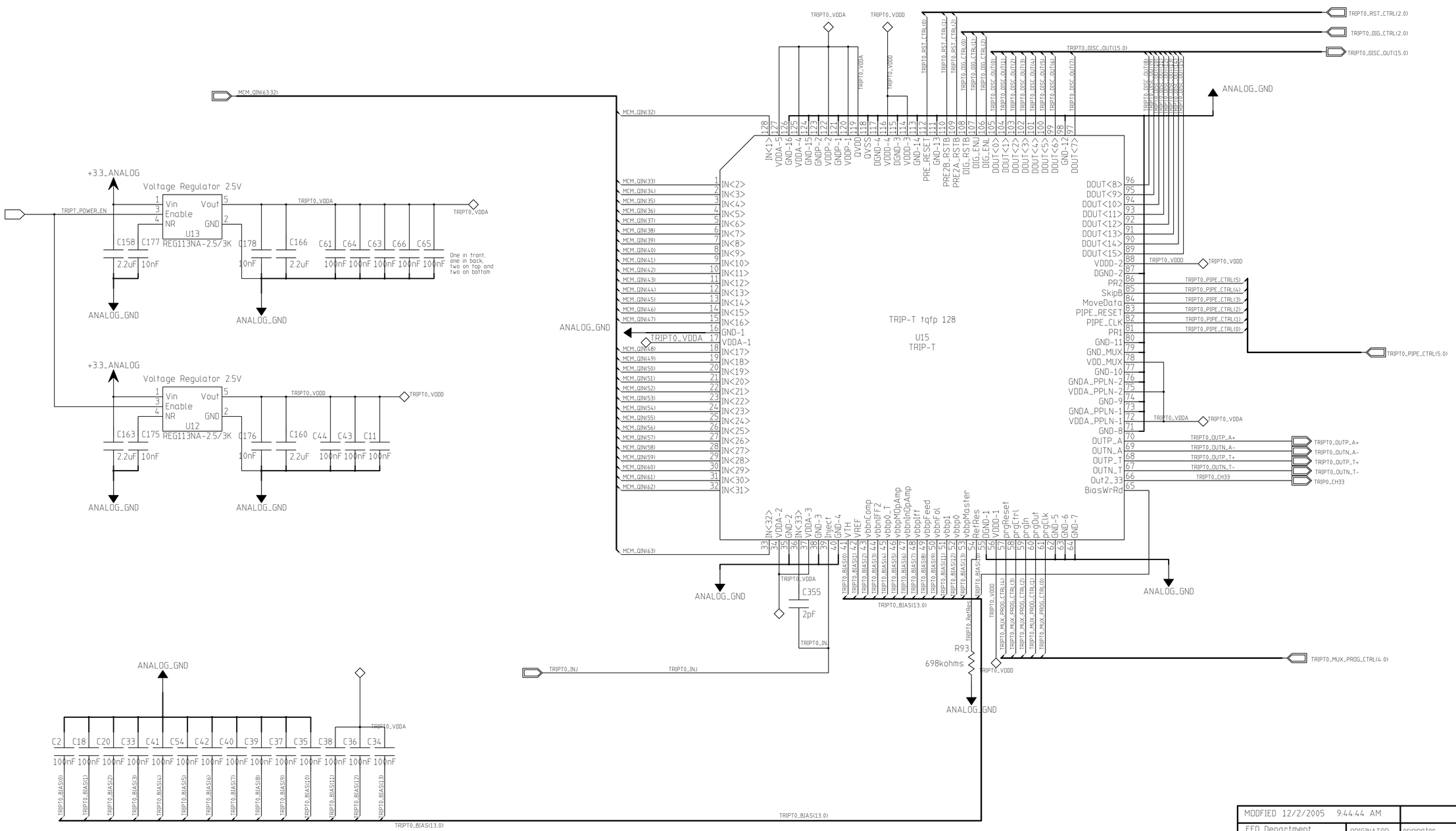
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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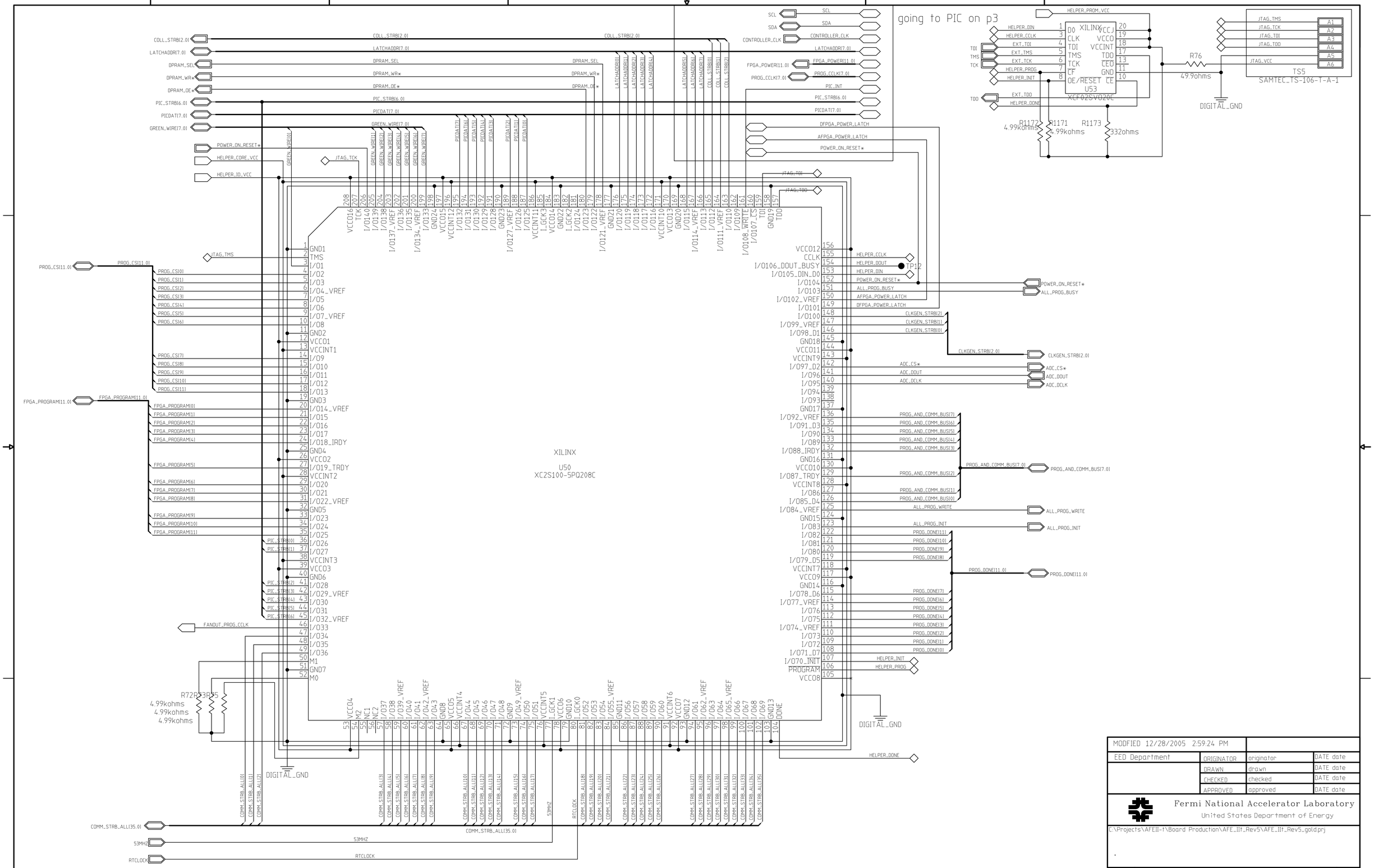
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA


XILINX
U50
XC2S100-5PQ208C
going to PIC on p3
XILINX
U53
XCF02SVO20C
TS5
SAMTEC_TS-106-T-A-1
R76
49.9ohms
R1172
4.99kohms
R1171
4.99kohms
R1173
332ohms
R72R73R75
4.99kohms
4.99kohms
4.99kohms
DIGITAL_GND
TP12
MODFIED 12/28/2005 2:59:24 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
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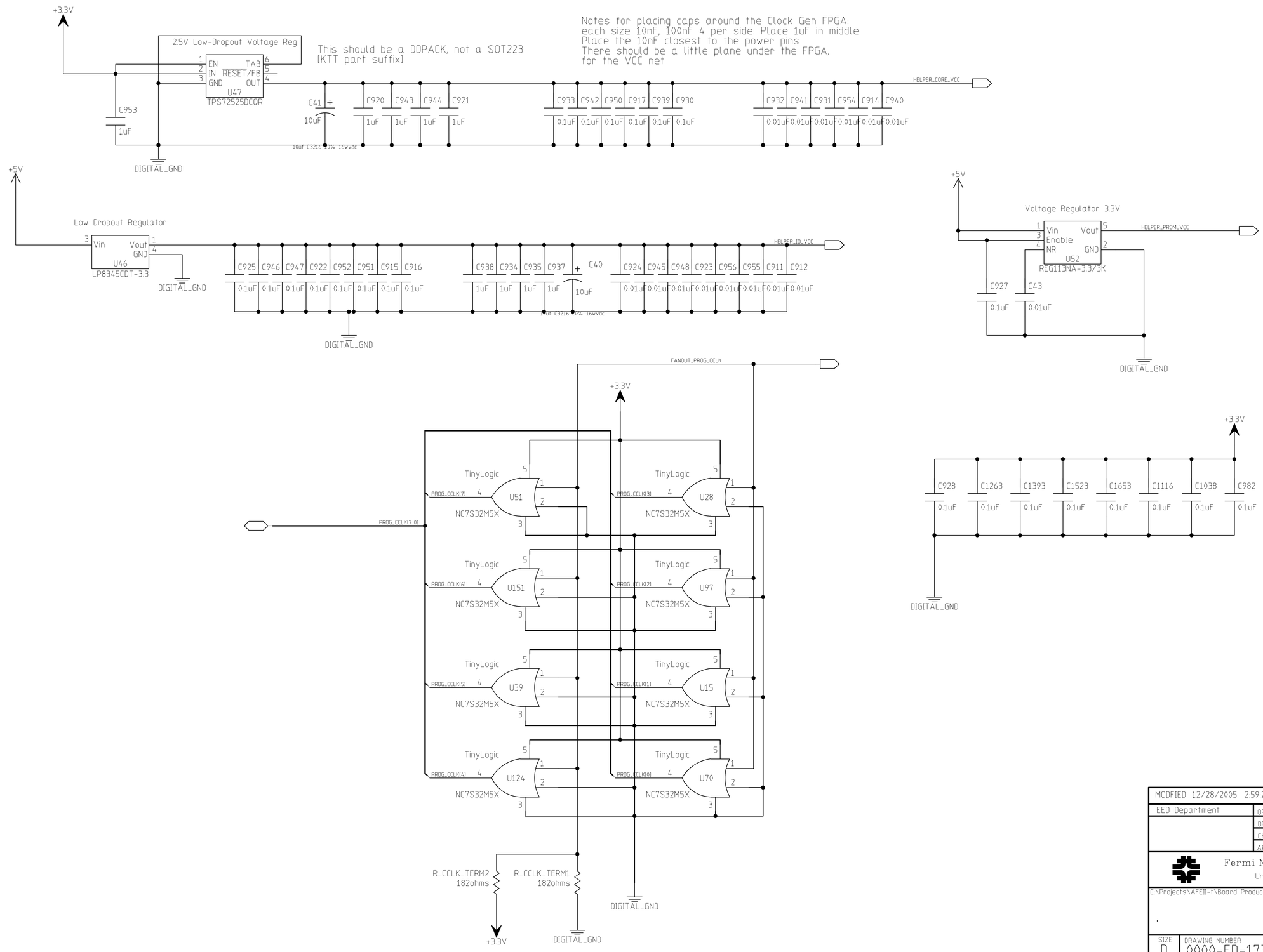
C:\Projects\AFEII-t\Board Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV



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EED Department	ORIGINATOR	originator	DATE date
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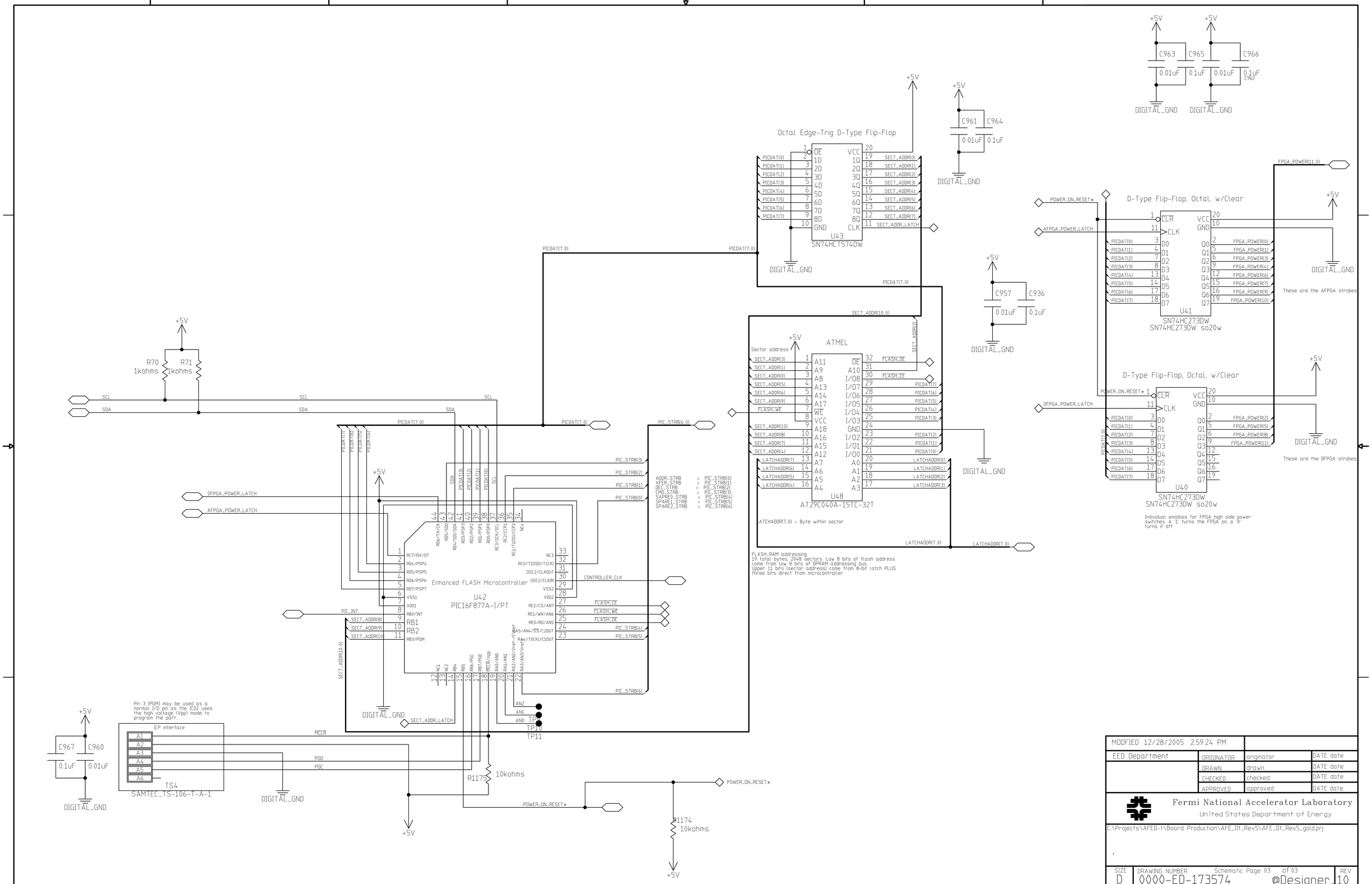
H:8ND, V:4LA


Octal Edge-Trig D-Type Flip-Flop
U43
SN74HCT574DW
ATMEL
U48
AT29C040A-15TC-32T
ATCHADDR[7..0] = Byte within sector
FLASH_RAM addressing
19 total bytes, 2048 sectors. Low 8 bits of flash address come from low 8 bits of DPRAM addressing bus.
Upper 11 bits (sector address) come from 8-bit latch PLUS three bits direct from microcontroller.
D-Type Flip-Flop, Octal, w/Clear
U41
SN74HC273DW
SN74HC273DW so20w
These are the AFPGA strobes
U40
These are the DFPGA strobes
Individual enables for FPGA high side power switches. A '1' turns the FPGA on, a '0' turns it off.
Enhanced FLASH Microcontroller
U42
PIC16F877A-I/PT
ADDR_STRB = PIC_STRB(0)
XFER_STRB = PIC_STRB(1)
DEC_STRB = PIC_STRB(2)
CMD_STRB = PIC_STRB(3)
SAPRE0_STRB = PIC_STRB(4)
SPARE1_STRB = PIC_STRB(5)
SPARE2_STRB = PIC_STRB(6)
Pin 3 (PGM) may be used as a normal I/O pin as the ICD2 uses the high voltage (Vpp) mode to program the part.
ICP interface
TS4
SAMTEC_TS-106-T-A-1
R70 1kohms
R71 1kohms
R1175 10kohms
R1174 10kohms
C963 0.01uF
C965 0.1uF
C966 0.01uF
C962 0.1uF
C961 0.01uF
C964 0.1uF
C957 0.01uF
C936 0.1uF
C967 0.1uF
C960 0.01uF
DIGITAL_GND
+5V
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SIZE D
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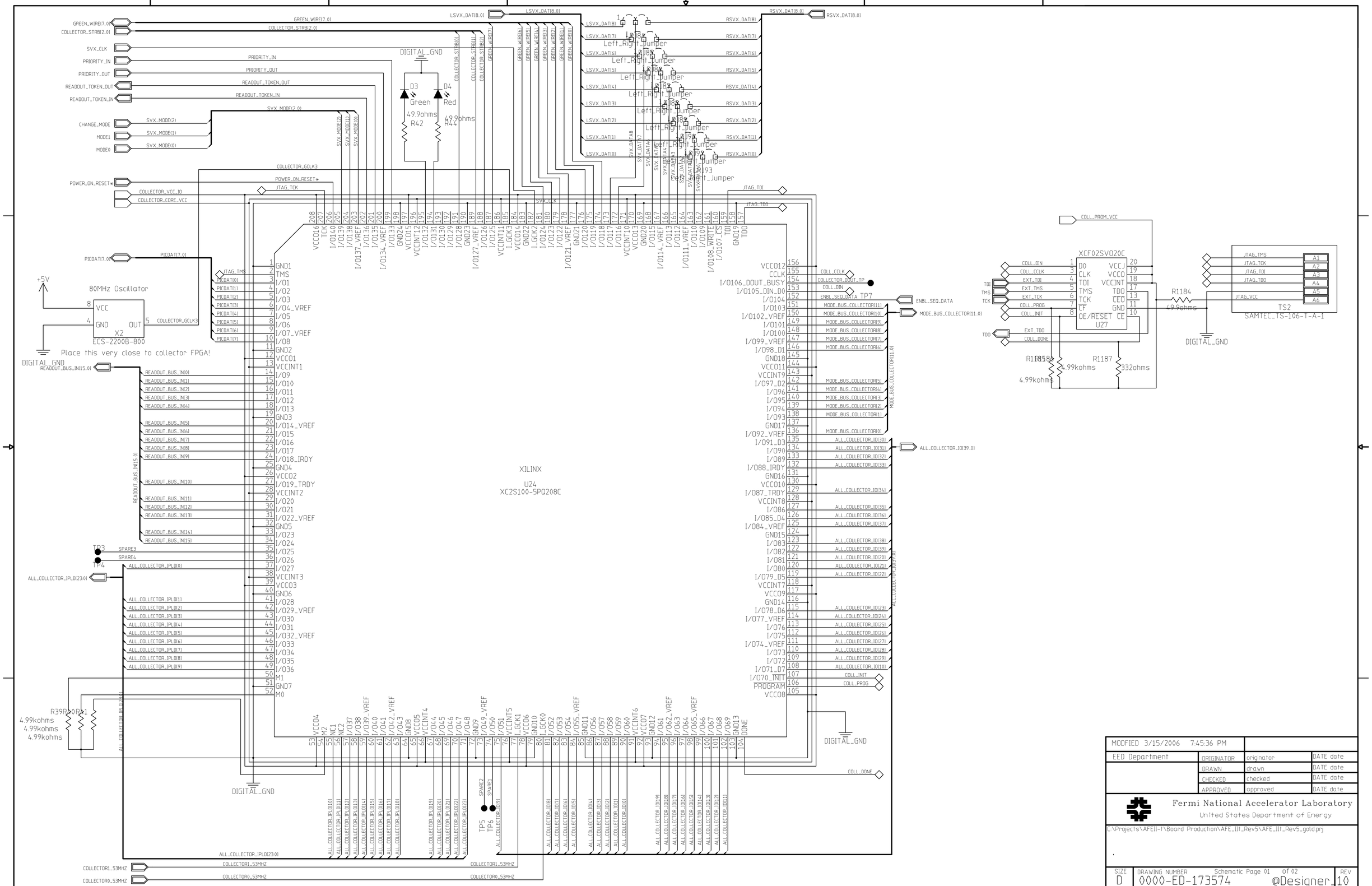
@Designer_10
REV
H=8ND, V=4LA



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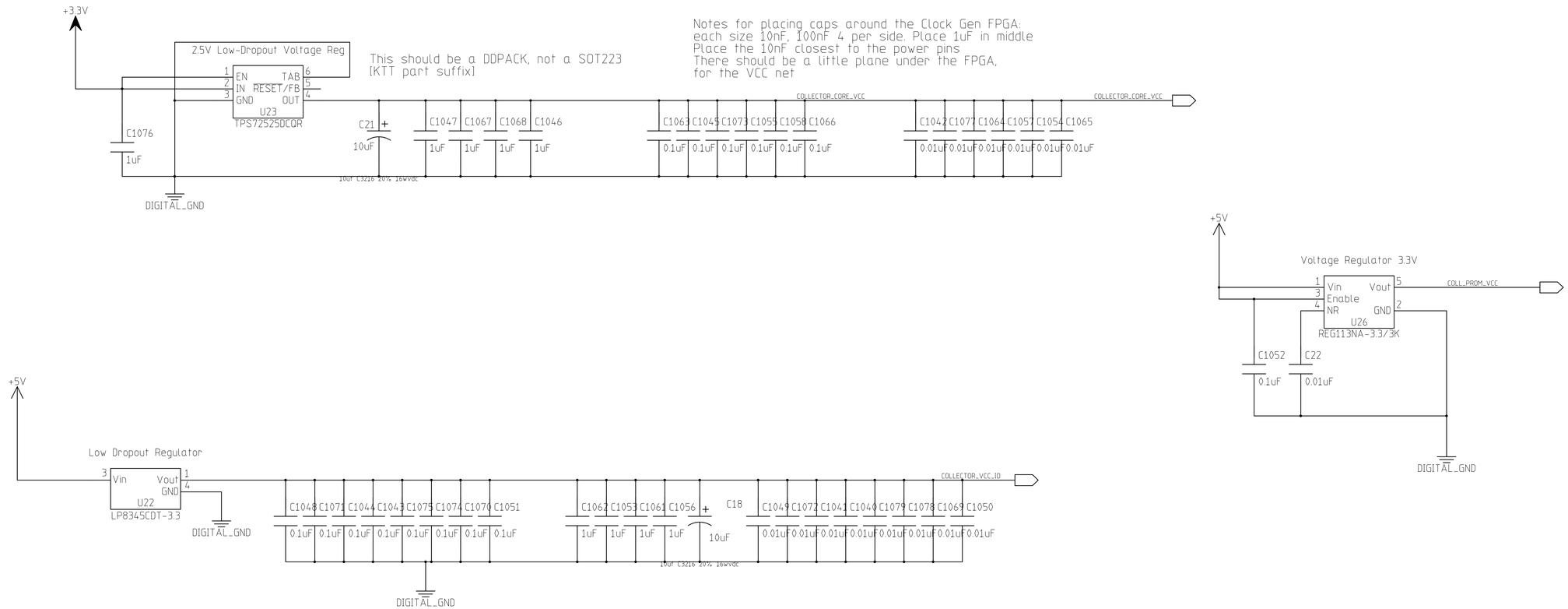
SIZE	DRAWING NUMBER	Schematic Page 01 of 02	REV
D	0000-ED-173574	@Designer_10	



MODFIED 3/15/2006 7:45:36 PM			
EED Department	ORIGINATOR	originator	DATE date
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.

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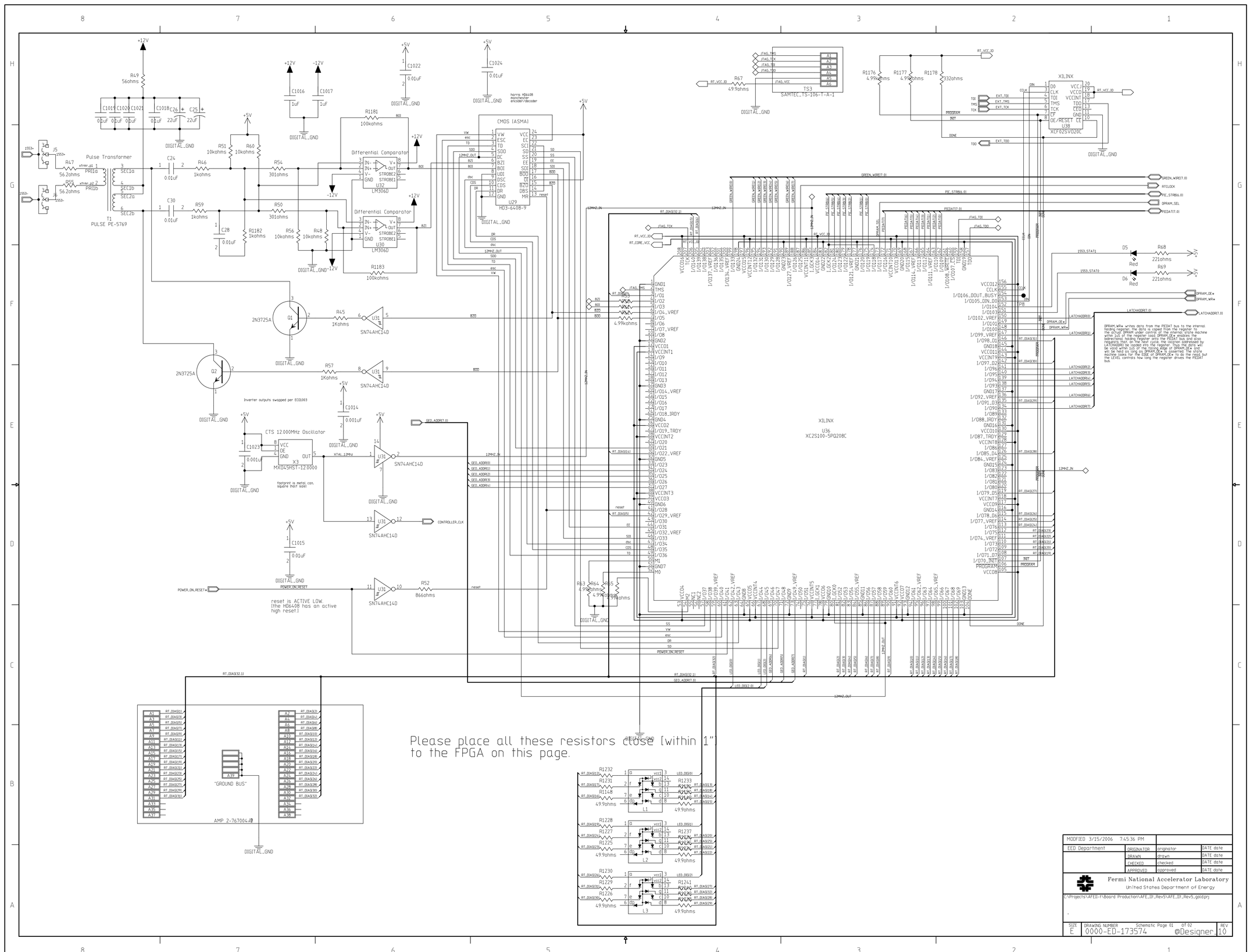
H:8ND, V:4LA



Please place all these resistors close (within 1") to the FPGA on this page.

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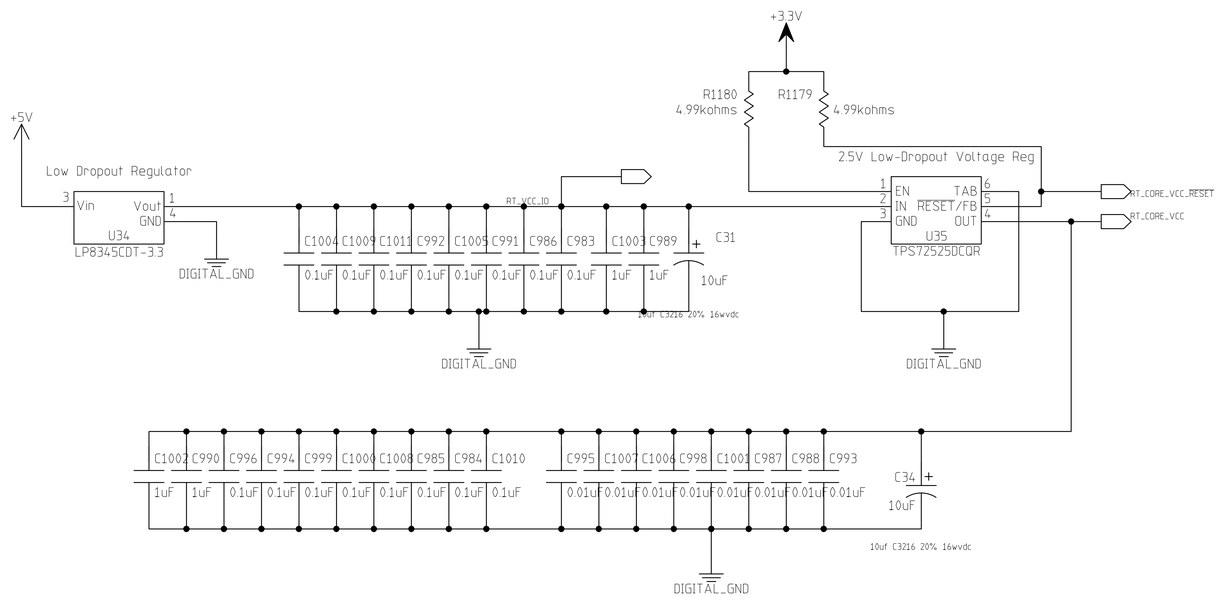

MODFIED 3/15/2006 7:45:36 PM			
EED Department	ORIGINATOR	originator	DATE date
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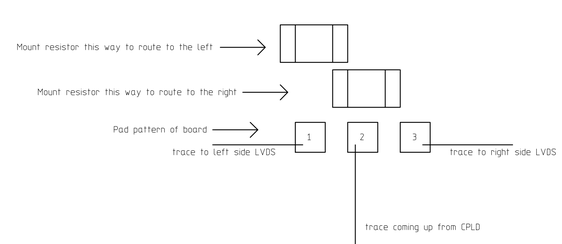
H=8ND, V=4LA

All jumpers are actually 3-pin pad arrays designed to allow installation of a low-resistance 0402 resistor either between pads 1 and 2 or pads 3 and 4, manually routing all eighty bits of the bus to the left-side LDVS drivers or to the right side LVDS drivers. This break removes the long stubs to the unused side allowing the unused side to be unstuffed and eliminating reflection possibilities.

Blowup sketch of how this works



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EED Department	ORIGINATOR	originator	DATE date
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SIZE	DRAWING NUMBER		REV
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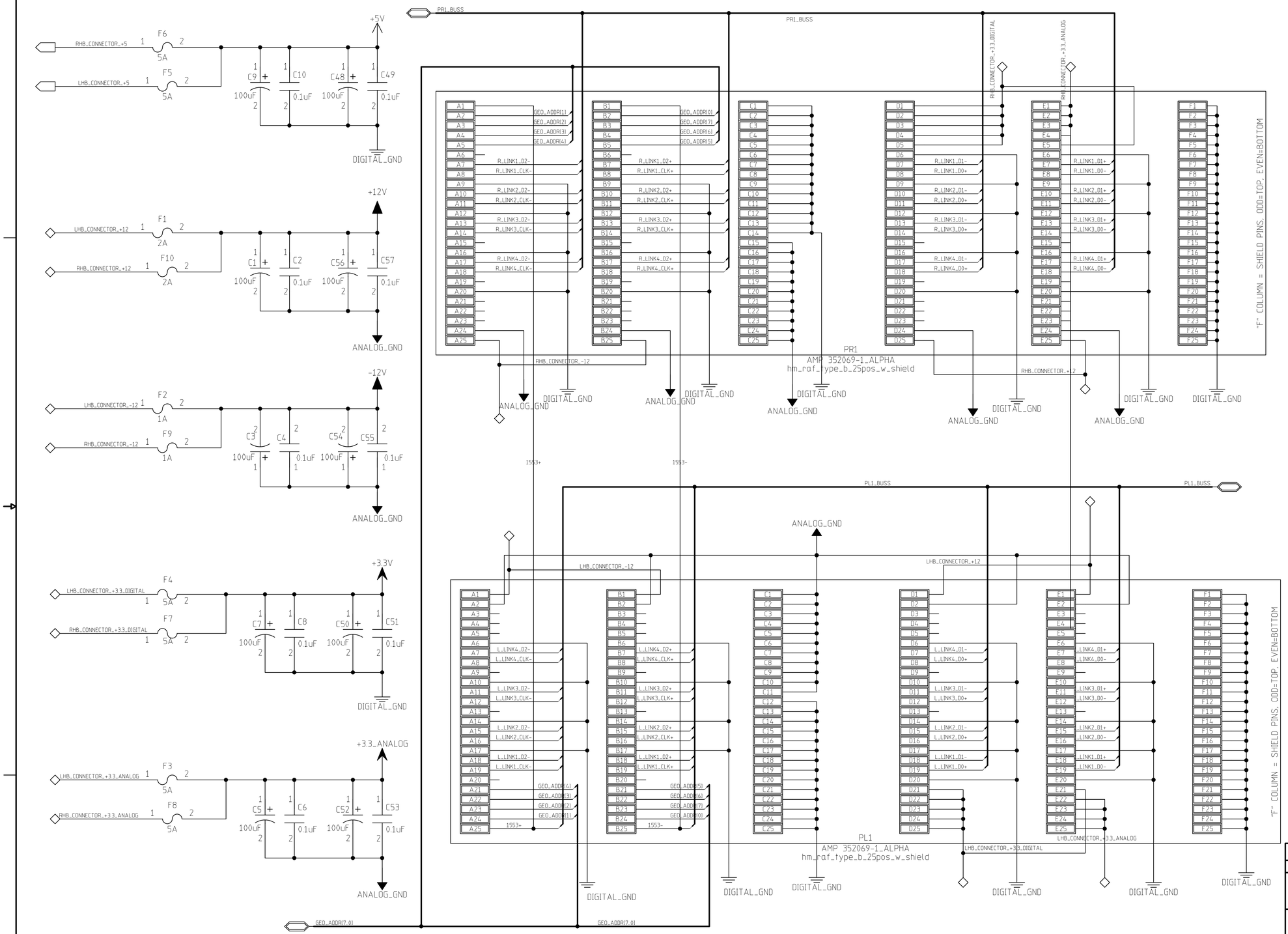
H:8ND, V:4LA



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EED Department	ORIGINATOR	originator	DATE date
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H=8ND, V=4LA

LEFT HAND INSERTION INTO BACKPLANE
PINOUT AS VIEWED FROM BOARD COMPONENT SIDE

CONNECTOR P1

	A	B	C	D	E
25			GND		
24			GND		
22			GND		
21			GND		
20			GND		
19			GND		
18			GND		
17	GND	GND	GND	GND	GND
16			GND		
15			GND		
14	GND	GND	GND	GND	GND
13			GND		
12			GND		
11			GND		
10	GND	GND	GND	GND	GND
9			GND		
8			GND		
7			GND		
6	GND	GND	GND	GND	GND
5			GND		
4			GND		
3			GND		
2	GND	GND	GND	GND	GND
1	-12V	-12V	GND	+12V	+12V

RIGHT HAND INSERTION INTO BACKPLANE
PINOUT AS VIEWED FROM BOARD COMPONENT SIDE

CONNECTOR P1

	E	D	C	B	A
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					

CONNECTOR P2

	A	B	C	D	E
25					
24					
22					
21					
20					
19					
18					
17					
16					
15					

	A	B	C	D	E
11					
10					
9					
8					
7					
6					
5					
4					
3					
2					
1					

	E	D	C	B	A
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					

	E	D	C	B	A
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					

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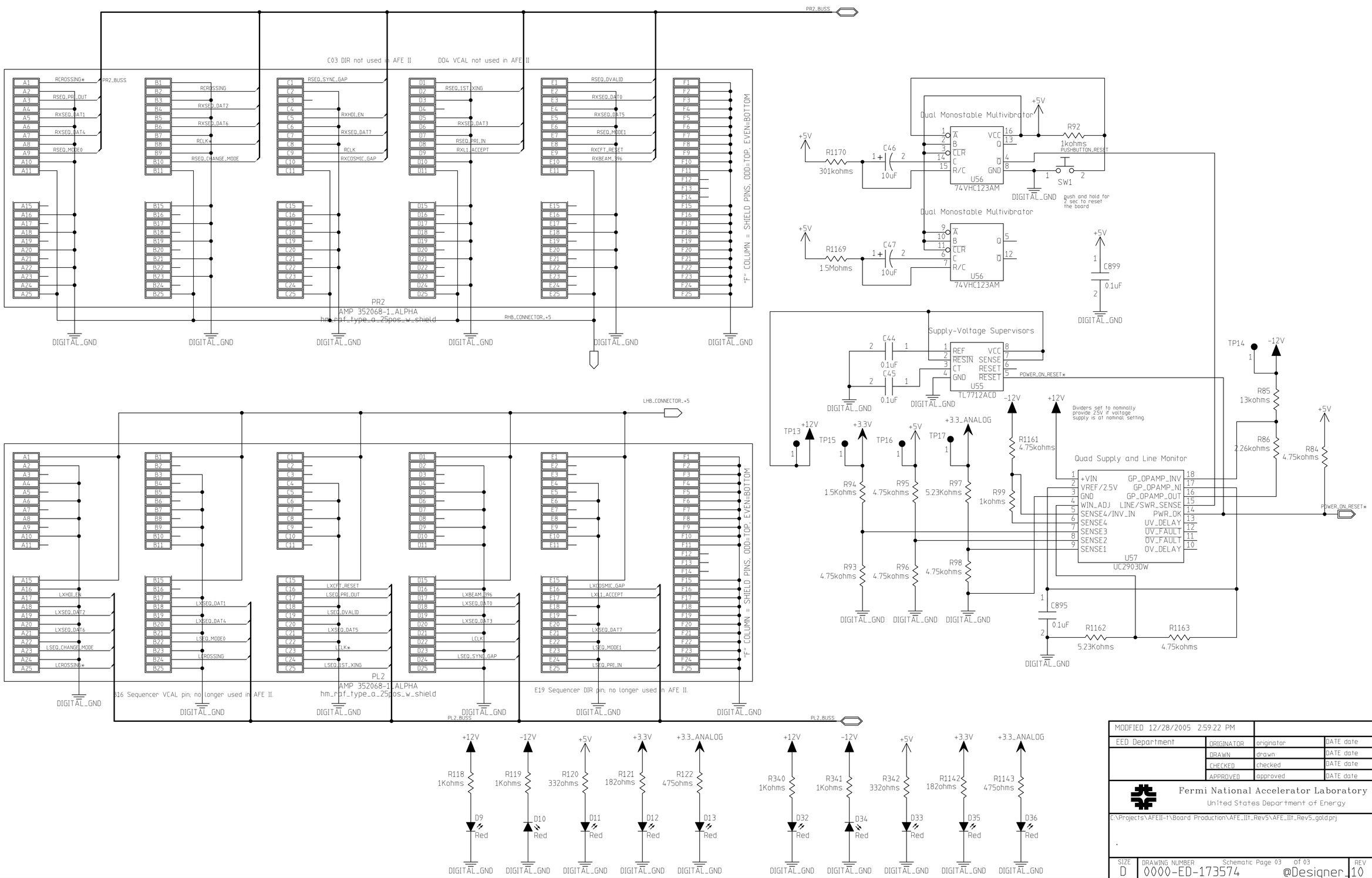
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H:8ND, V:4LA


PR2_BUSS
C03 DIR not used in AFE II
D04 VCAL not used in AFE II
RCROSSING*
RSEQ_PRI_OUT
RXSEQ_DAT1
RXSEQ_DAT4
RSEQ_MODE0
RCROSSING
RXSED_DAT2
RXSED_DAT6
RCLK*
RSEQ_CHANGE_MODE
RSEQ_SYNC_GAP
RXHDI_EN
RXSEQ_DAT7
RCLK
RXCOSMIC_GAP
RSEQ_1ST_XING
RXSEQ_DAT3
RSEQ_PRI_IN
RXL1_ACCEPT
RSEQ_DVALID
RXSEQ_DAT0
RXSEQ_DAT5
RSEQ_MODE1
RXCFT_RESET
RXBEAM_396
"F" COLUMN = SHIELD PINS, ODD=TOP, EVEN=BOTTOM
PR2
AMP 352068-1_ALPHA
hm_raf_type_a_25pos_w_shield
RHB_CONNECTOR_+5
DIGITAL_GND
Dual Monostable Multivibrator
74VHC123AM
U56
R1170
301kohms
C46
10uF
R92
1kohms
PUSHBUTTON_RESET
SW1
push and hold for 2 sec to reset the board
R1169
1.5Mohms
C47
C899
0.1uF
Supply-Voltage Supervisors
TL7712ACD
U55
C44
C45
POWER_ON_RESET*
TP14
-12V
R85
13kohms
R86
2.26kohms
R84
4.75kohms
TP13
TP15
TP16
TP17
+3.3_ANALOG
R1161
4.75kohms
Dividers set to nominally provide 2.5V if voltage supply is at nominal setting.
Quad Supply and Line Monitor
UC2903DW
U57
+VIN
VREF/2.5V
GND
WIN_ADJ
SENSE4/INV_IN
SENSE4
SENSE3
SENSE2
SENSE1
GP_OPAMP_INV
GP_OPAMP_NI
GP_OPAMP_OUT
LINE/SWR_SENSE
PWR_OK
UV_DELAY
UV_FAULT
OV_FAULT
OV_DELAY
R94
1.5Kohms
R95
4.75kohms
R97
5.23Kohms
R99
1kohms
R93
4.75kohms
R96
4.75kohms
R98
4.75kohms
C895
R1162
5.23Kohms
R1163
4.75kohms
LHB_CONNECTOR_+5
PL2
AMP 352068-1_ALPHA
hm_raf_type_a_25pos_w_shield
LXCFT_RESET
LSEQ_PRI_OUT
LSEQ_DVALID
LXSEQ_DAT5
LCLK*
LSEQ_1ST_XING
LXCOSMIC_GAP
LXL1_ACCEPT
LXSEQ_DAT7
LSEQ_MODE1
LSEQ_PRI_IN
LXHDI_EN
LXSEQ_DAT2
LXSEQ_DAT6
LSEQ_CHANGE_MODE
LCROSSING*
LXSEQ_DAT1
LXSEQ_DAT4
LSEQ_MODE0
LCROSSING
LXBEAM_396
LXSEQ_DAT0
LXSEQ_DAT3
LCLK
LSEQ_SYNC_GAP
B16 Sequencer VCAL pin, no longer used in AFE II.
E19 Sequencer DIR pin, no longer used in AFE II.
PL2_BUSS
+12V
-12V
+5V
+3.3V
+3.3_ANALOG
R118
1Kohms
R119
1Kohms
R120
332ohms
R121
182ohms
R122
475ohms
D9
D10
D11
D12
D13
Red
R340
1Kohms
R341
1Kohms
R342
332ohms
R1142
182ohms
R1143
475ohms
D32
D34
D33
D35
D36
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SIZE
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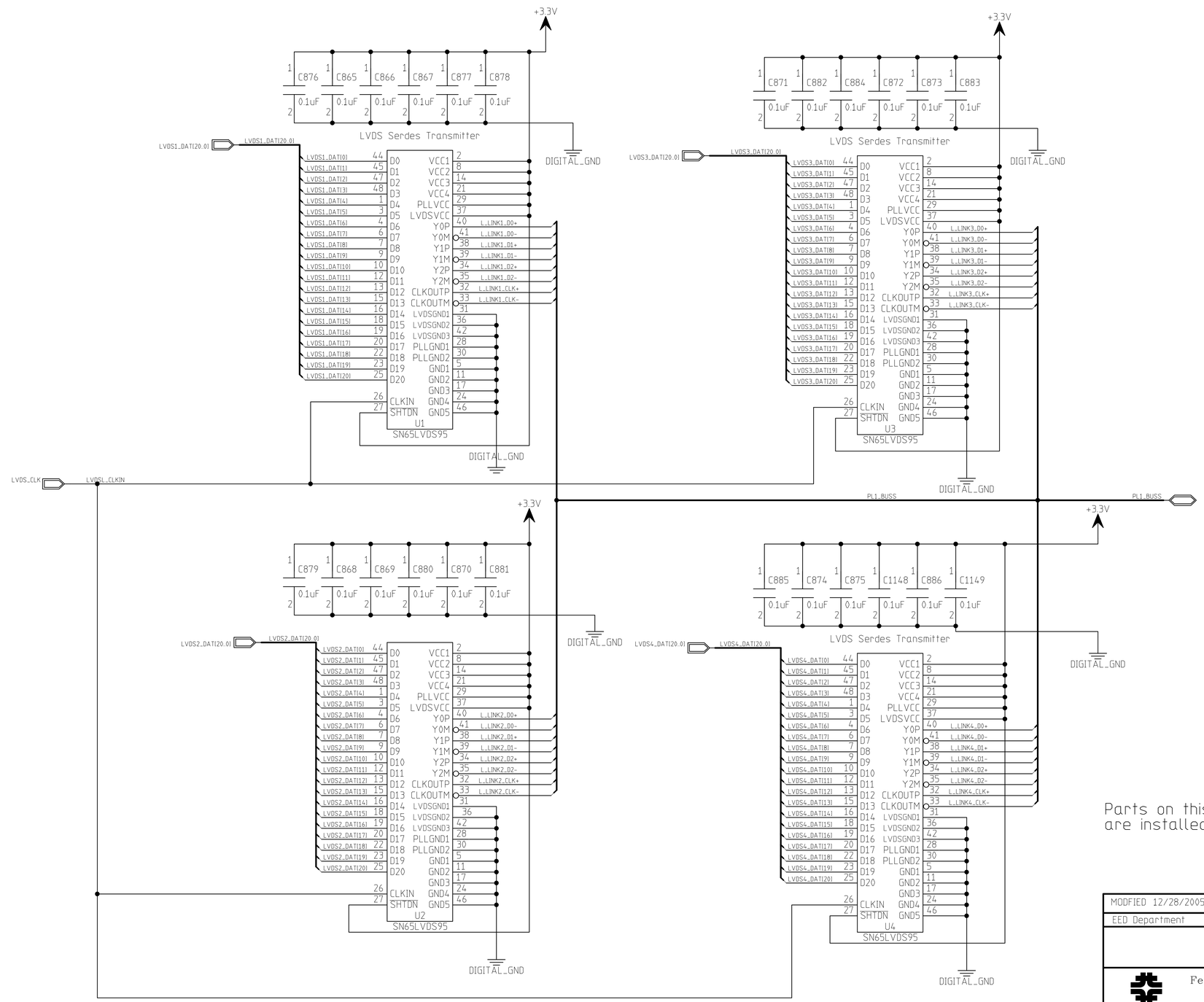
@Designer_10
REV
H:8ND, V:4LA



Parts on this page, if installed, are installed onto left-hand

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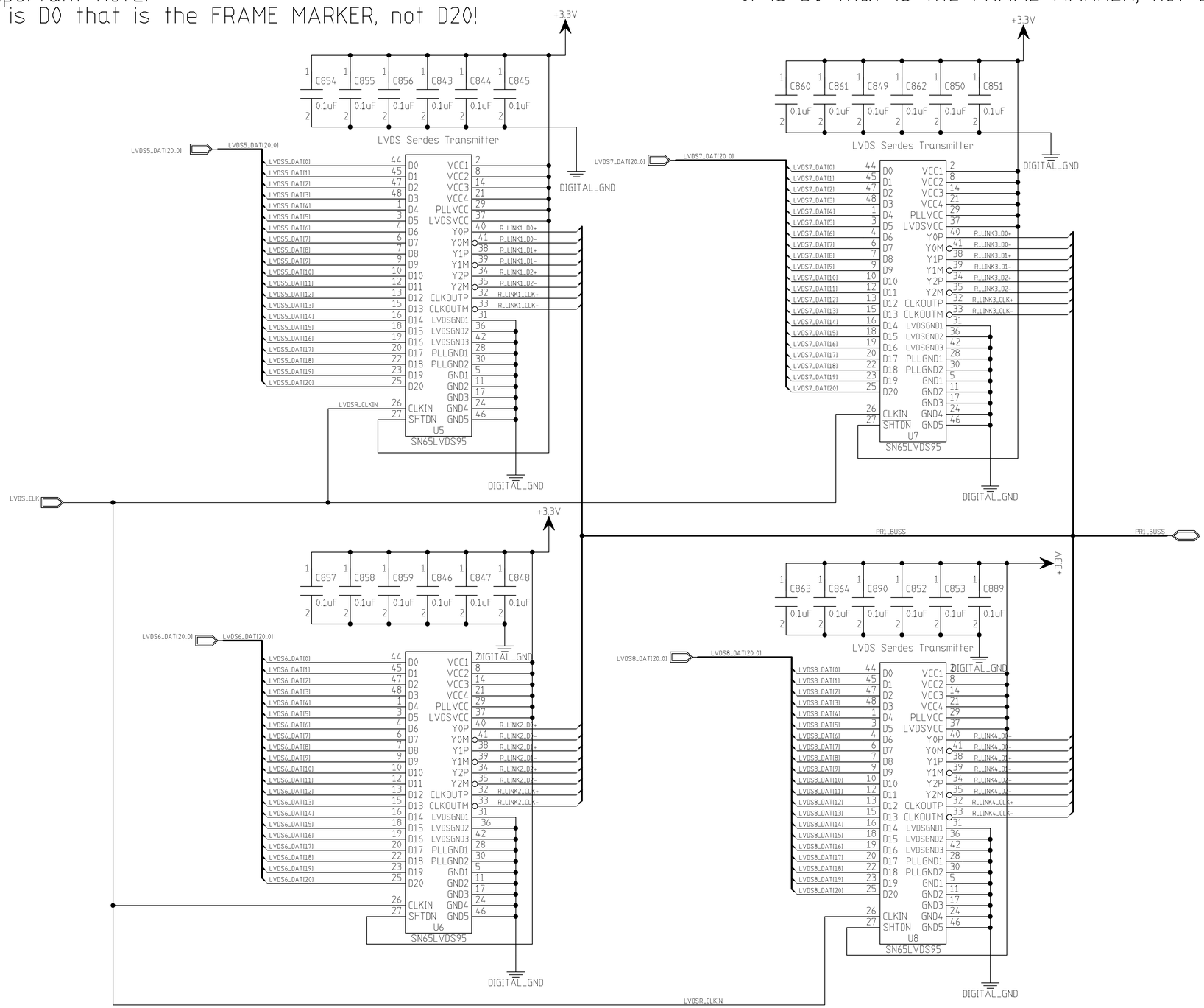
H=8ND, V=4LA

Important Note:
It is D0 that is the FRAME MARKER, not D20!

Important Note:
It is D0 that is the FRAME MARKER, not D20!



MODIFIED 12/28/2005 2:59:20 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
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	APPROVED	approved	DATE date

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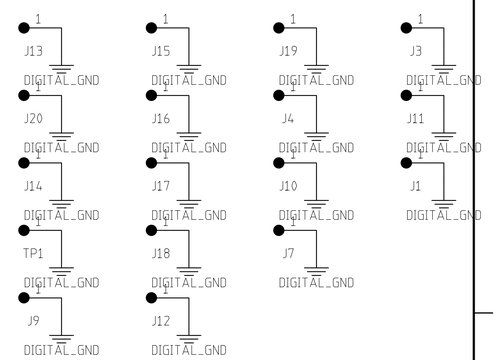
H=8ND, V=4LA



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EED Department	ORIGINATOR	originator	DATE date
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.

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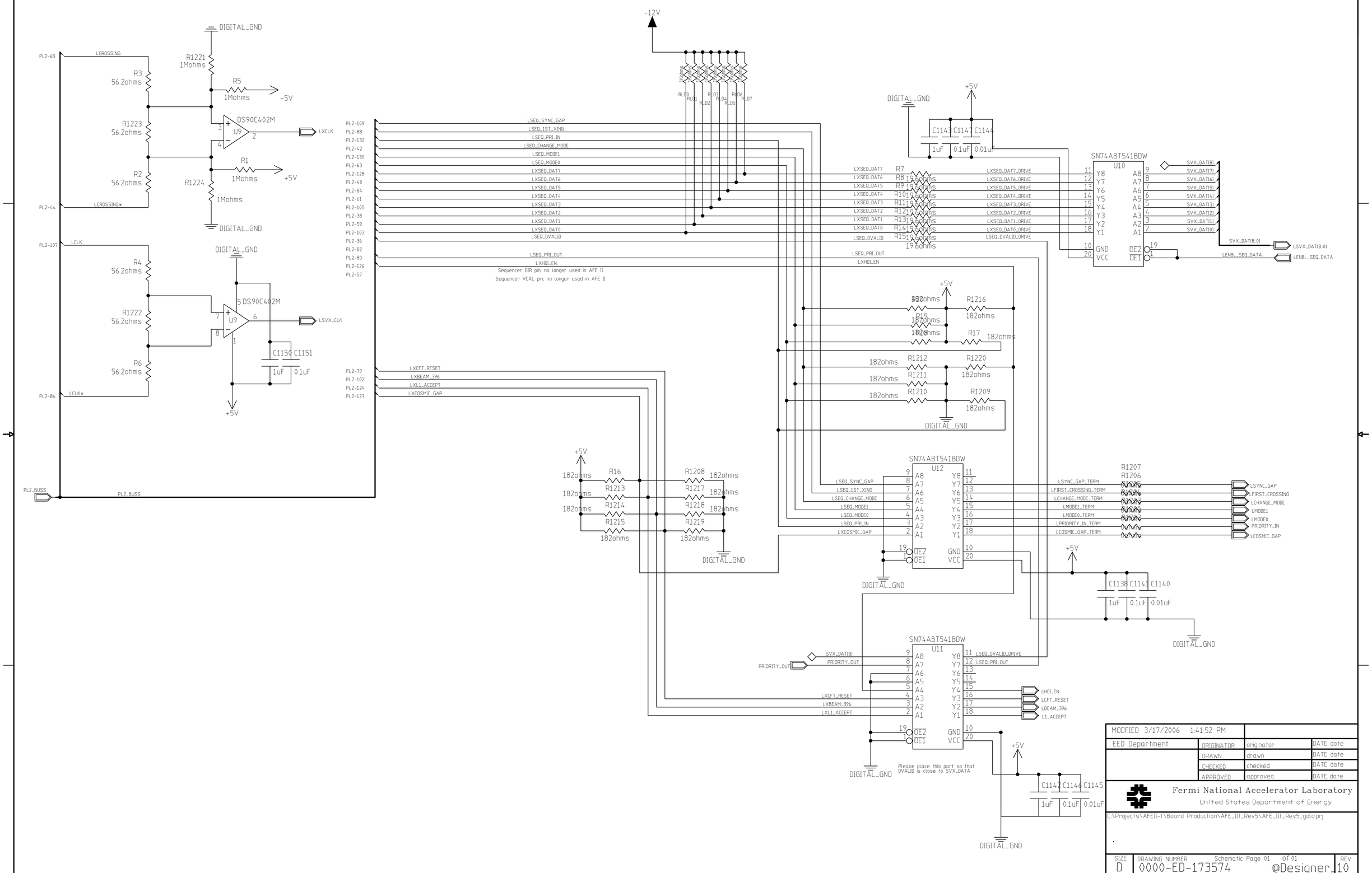
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA



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EED Department	ORIGINATOR	originator	DATE date
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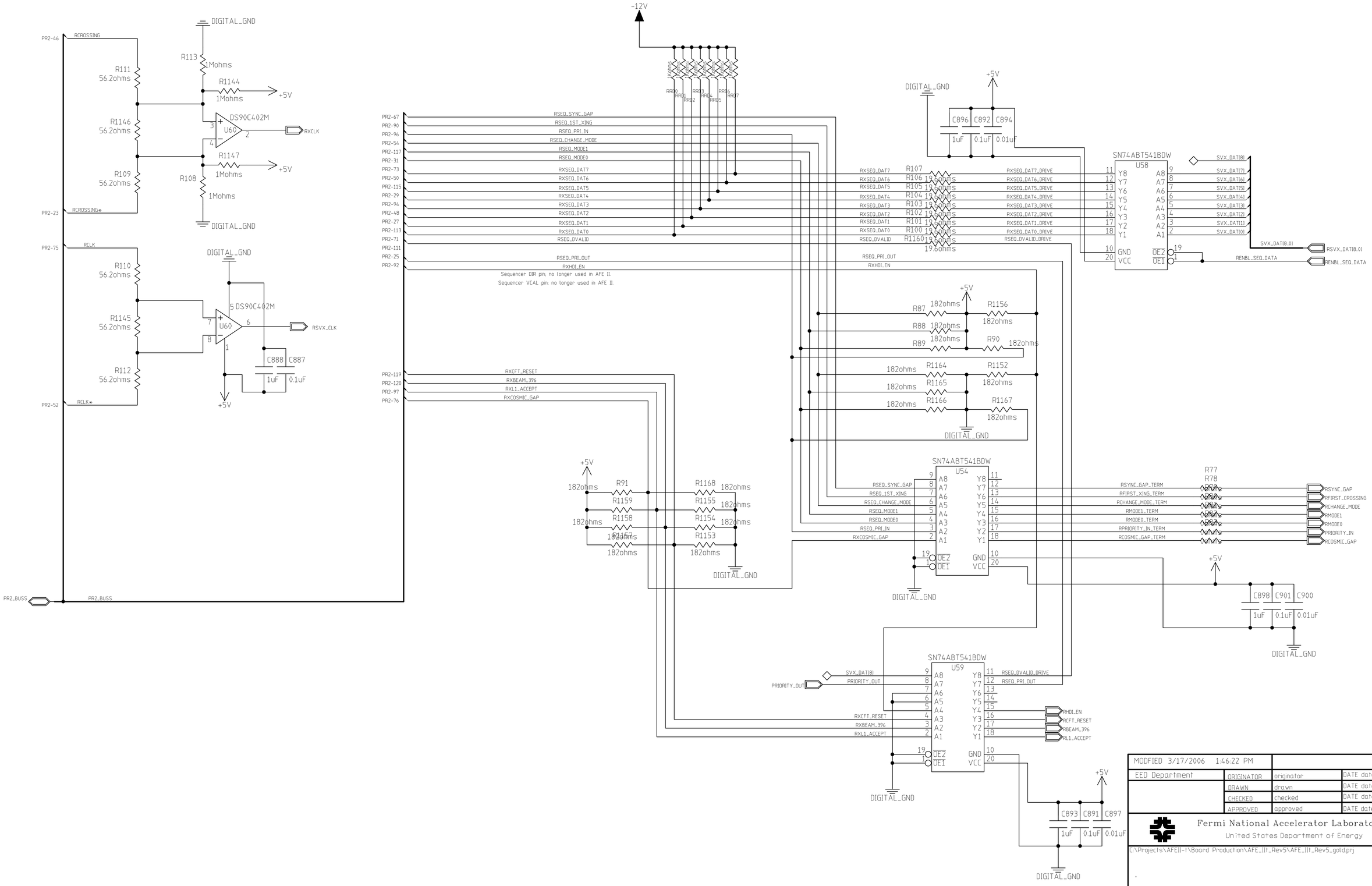
D	0000-ED-173574	@Designer_1	0

H=8ND, V=4LA



MODFIED 3/17/2006 1:46:22 PM			
EED Department	ORIGINATOR	originator	DATE date
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