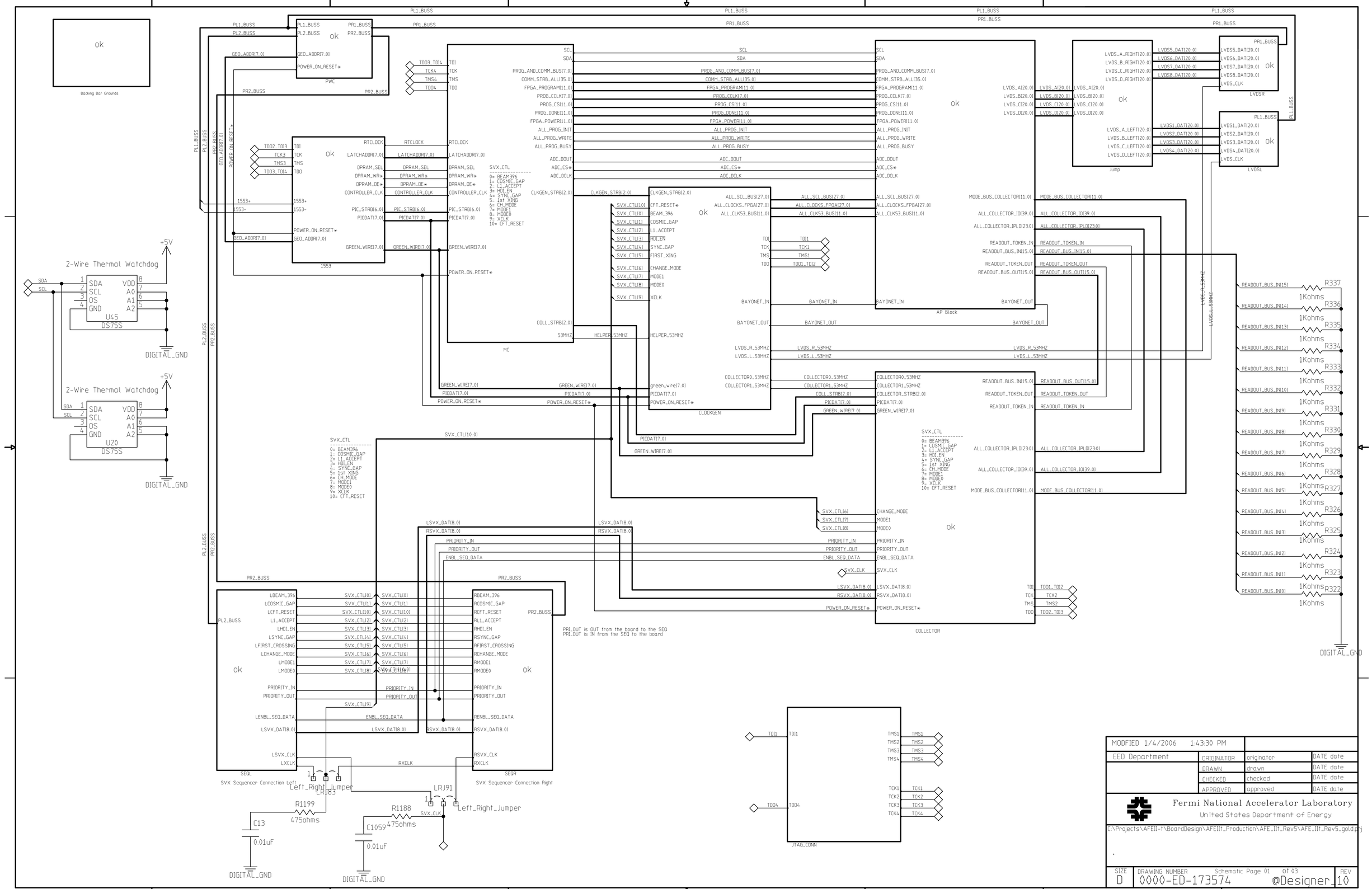

Backing Bar Grounds
PWC
1553
MC
CLOCKGEN
AP Block
Jump
LVDSR
LVDSL
COLLECTOR
SEQL
SVX Sequencer Connection Left
SEQR
SVX Sequencer Connection Right
JTAG_CONN
2-Wire Thermal Watchdog
U45
DS75S
U20
DS75S
DIGITAL_GND
Left_Right_Jumper
LRJ83
LRJ91
R1199
475ohms
R1188
475ohms
C13
0.01uF
C1059
0.01uF
R337
R336
R335
R334
R333
R332
R331
R330
R329
R328
R327
R326
R325
R324
R323
R322
1Kohms
MODIFIED 1/4/2006 1:43:30 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV
H=8ND; V=4LA

These go to page2 of this schematic

DFPGA_VCC → DFPGA_VCC
DFPGA_POWER → DFPGA_POWER_EN
TRIPT0_DIG_CTRL_S0(2.0) → TRIPT0_DIG_CTRL_S0(2.0)
TRIPT1_DIG_CTRL_S0(2.0) → TRIPT1_DIG_CTRL_S0(2.0)
TRIPT0_DIG_CTRL_S1(2.0) → TRIPT0_DIG_CTRL_S1(2.0)
TRIPT1_DIG_CTRL_S1(2.0) → TRIPT1_DIG_CTRL_S1(2.0)
DIG_CTRL(0) = DIG_RSTB
DIG_CTRL(1) = DIG_ENU
DIG_CTRL(2) = DIG_ENL
ALL_DIG_CTRL0
ALL_DIG_CTRL1
ALL_DIG_CTRL2

TRIPT0_DISC_OUT_S1(15.0) — DISC(63:48)
TRIPT1_DISC_OUT_S1(15.0) — DISC(47:32)
TRIPT0_DISC_OUT_S0(15.0) — DISC(31:16)
TRIPT1_DISC_OUT_S0(15.0) — DISC(15:0)

CLOCKS_DFPGA(2) — R10 1kohms — DIGITAL_GND
CLOCKS_DFPGA(1) — R12 1kohms — DIGITAL_GND
CLOCKS_DFPGA(0) — R9 1kohms — DIGITAL_GND
CLK53 — R11 1kohms — DIGITAL_GND
R7 1kohms — DIGITAL_GND
R8 1kohms
R2 1kohms

XILINX
U1
XC2S150-5PQ208C

TS1
SAMTEC_TS-106-T-A-1
R13 49.9ohms — DIGITAL_GND

DFPGA_CCLK
DFPGA_BUSY
LVDS_DRIVE(20.0)
SCL_BUS(6.0)
DFPGA_INIT
DFPGA_PROGRAM
PROG_and_COMM_BUS(7.0)
DFPGA_DONE
MODE_BUS
VERT_IPLD_S1(7.0)
COMM_STRB_DFPGA(2.0)

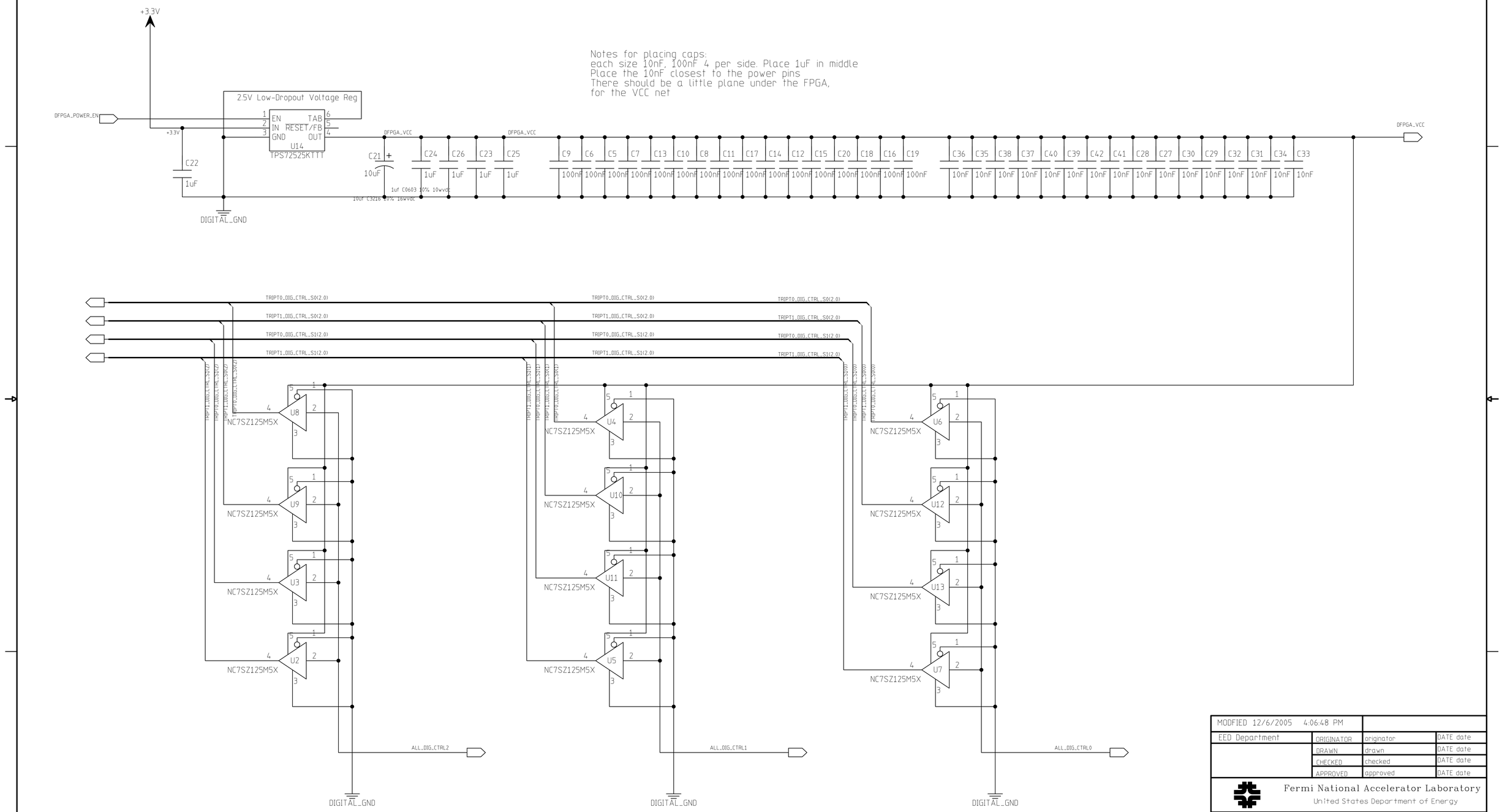
MODIFIED 12/6/2005 4:06:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-1\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer	10

H:8ND, V:4LA



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

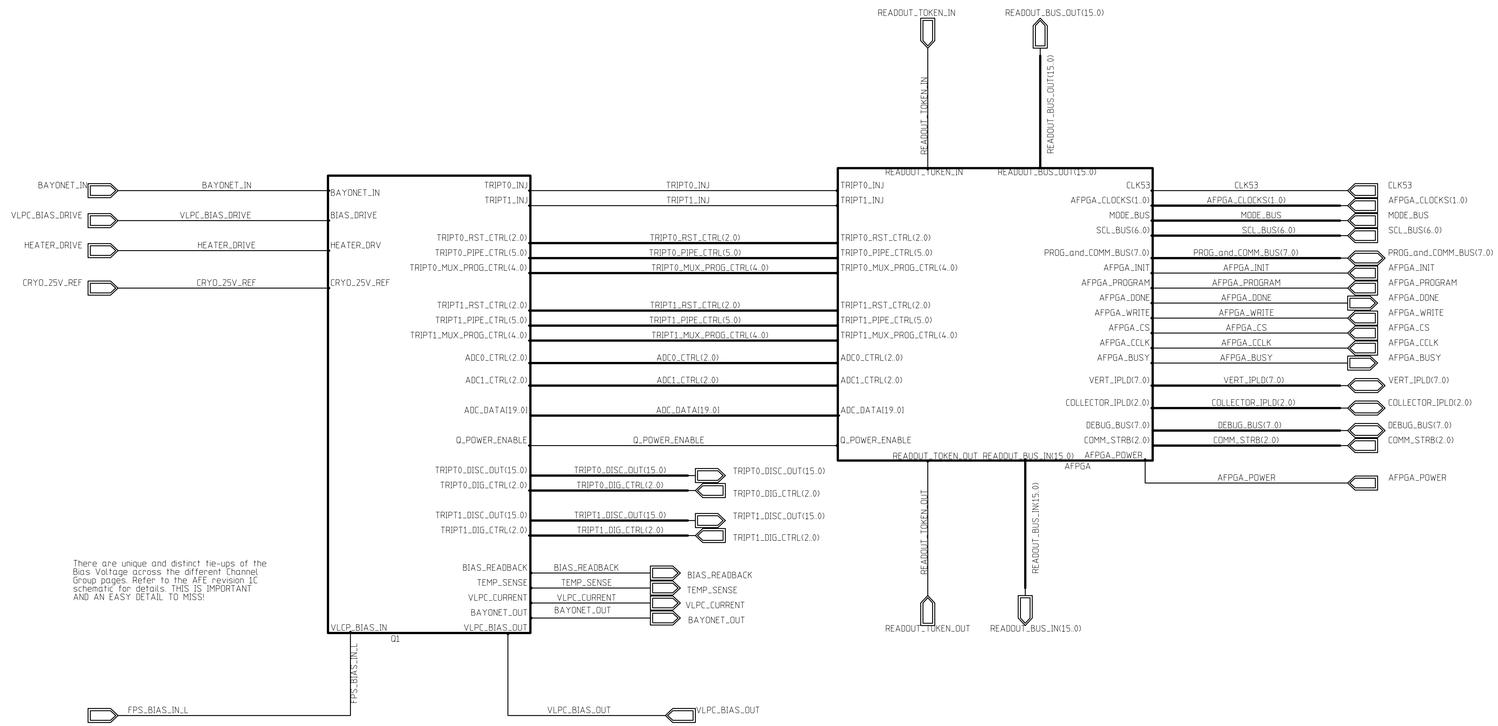
MODFIED 12/6/2005 4:06:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-1\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA



MODFIED 11/29/2005 10:13:28 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

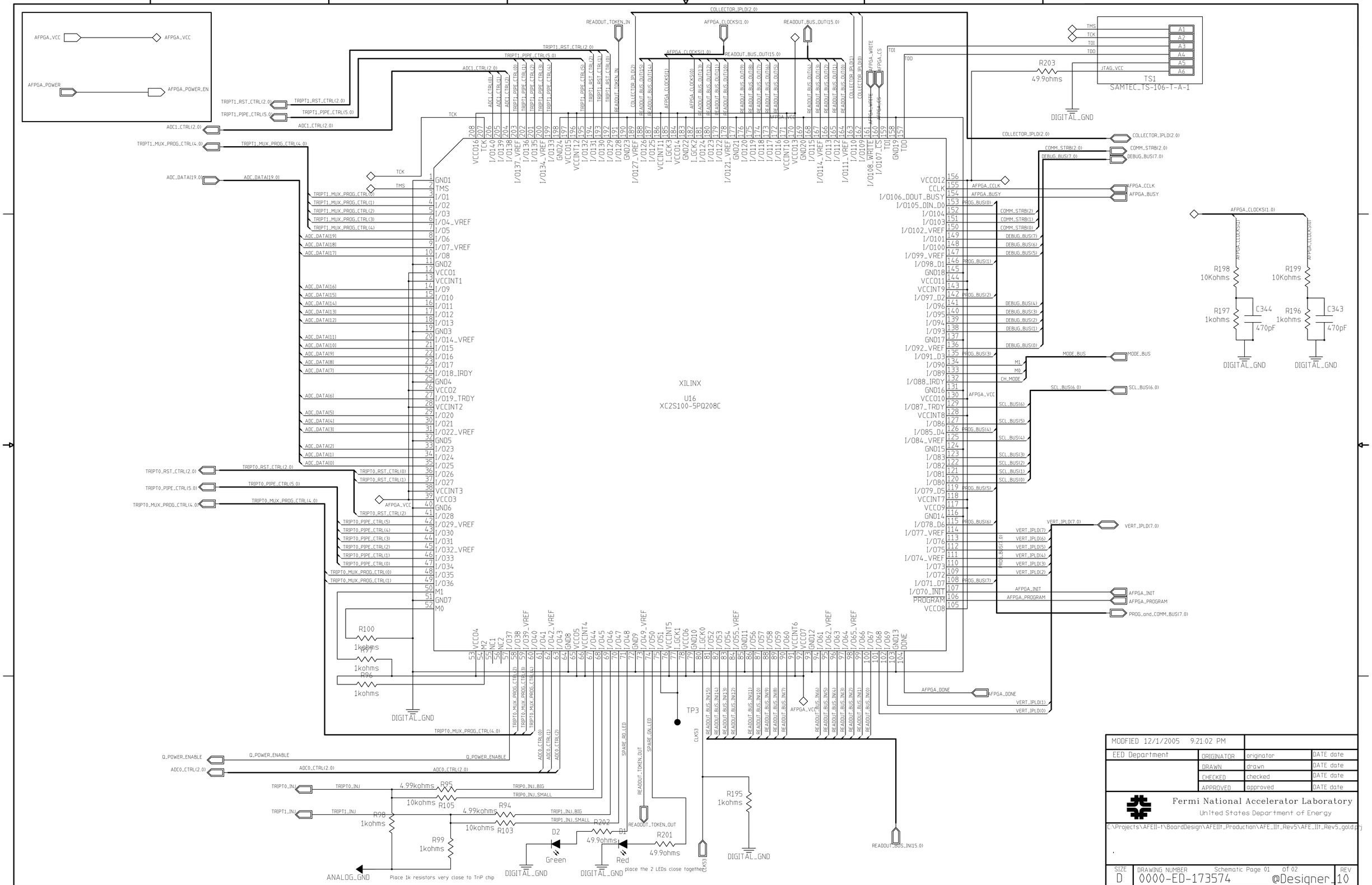
Fermi National Accelerator Laboratory
United States Department of Energy

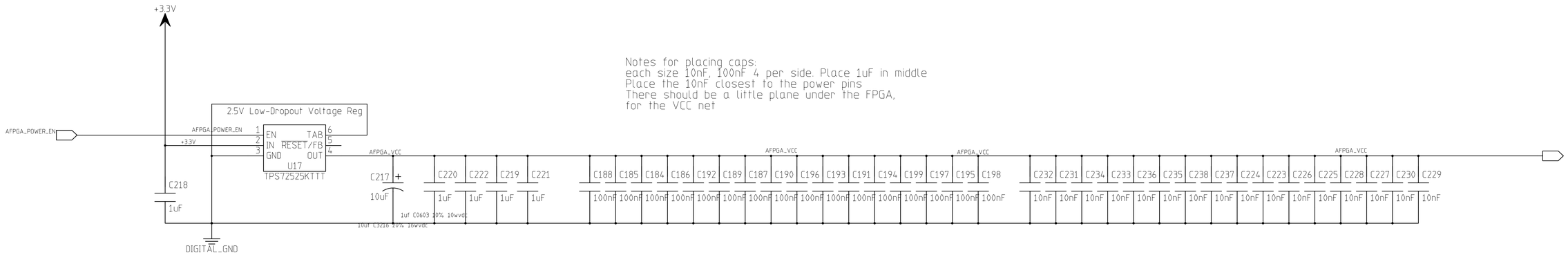
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H=8ND, V=4LA


XILINX
U16
XC2S100-5PQ208C
SAMTEC_TS-106-T-A-1
TS1
R203
49.9ohms
DIGITAL_GND
R198
10Kohms
R199
10Kohms
R197
1kohms
R196
1kohms
C344
470pF
C343
470pF
R100
1kohms
R97
1kohms
R96
1kohms
R95
4.99kohms
R105
10kohms
R94
4.99kohms
R103
10kohms
R98
1kohms
R99
1kohms
R202
49.9ohms
R201
49.9ohms
R195
1kohms
D2
Green
D1
Red
TP3
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-T\BoardDesign\AFEIIT_Production\AFE_IIT_Rev5\AFE_IIT_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 02
@Designer_10
REV
H=8ND, V=4LA



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

MODFIED 12/1/2005 9:21:02 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

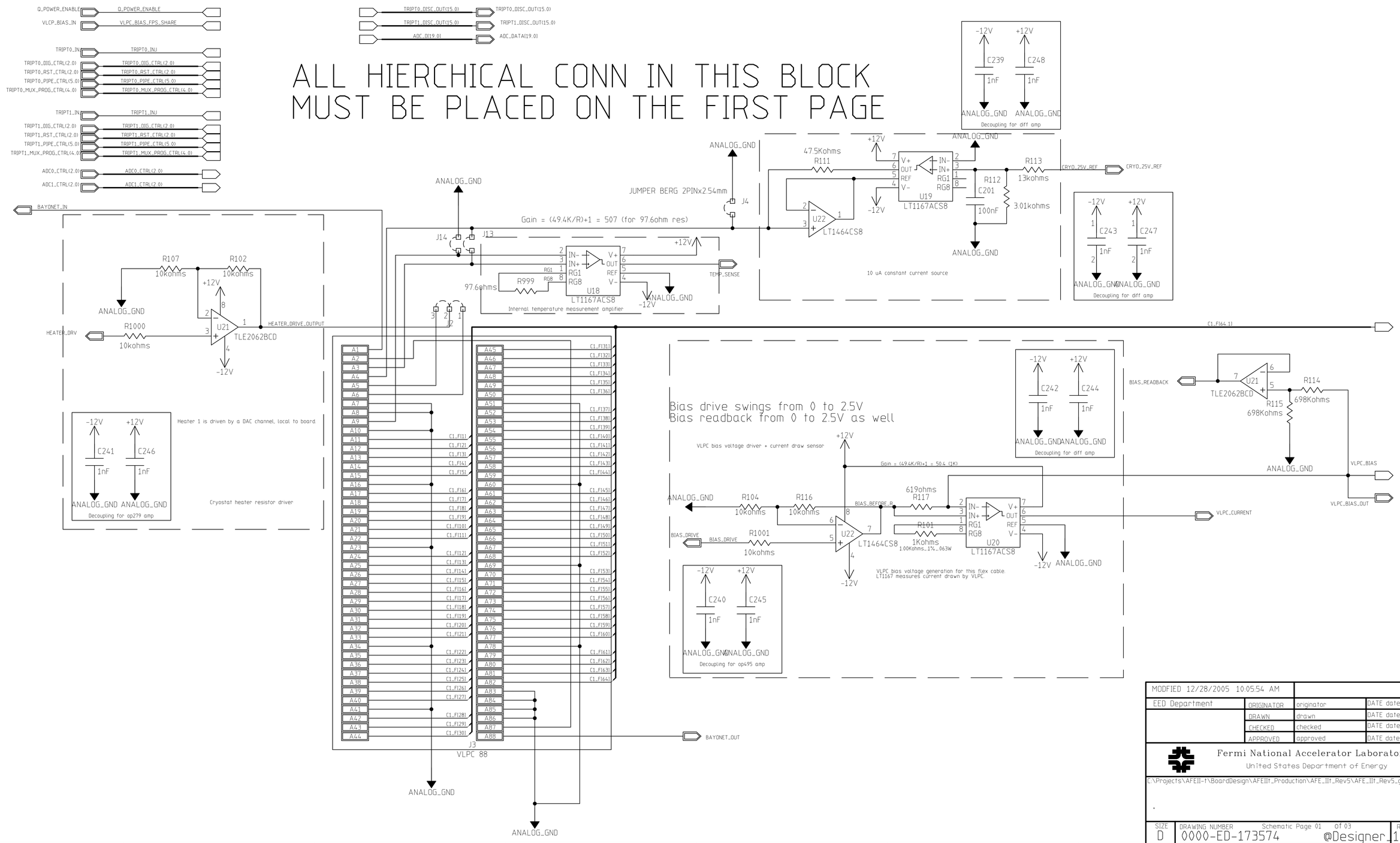
Fermi National Accelerator Laboratory
United States Department of Energy

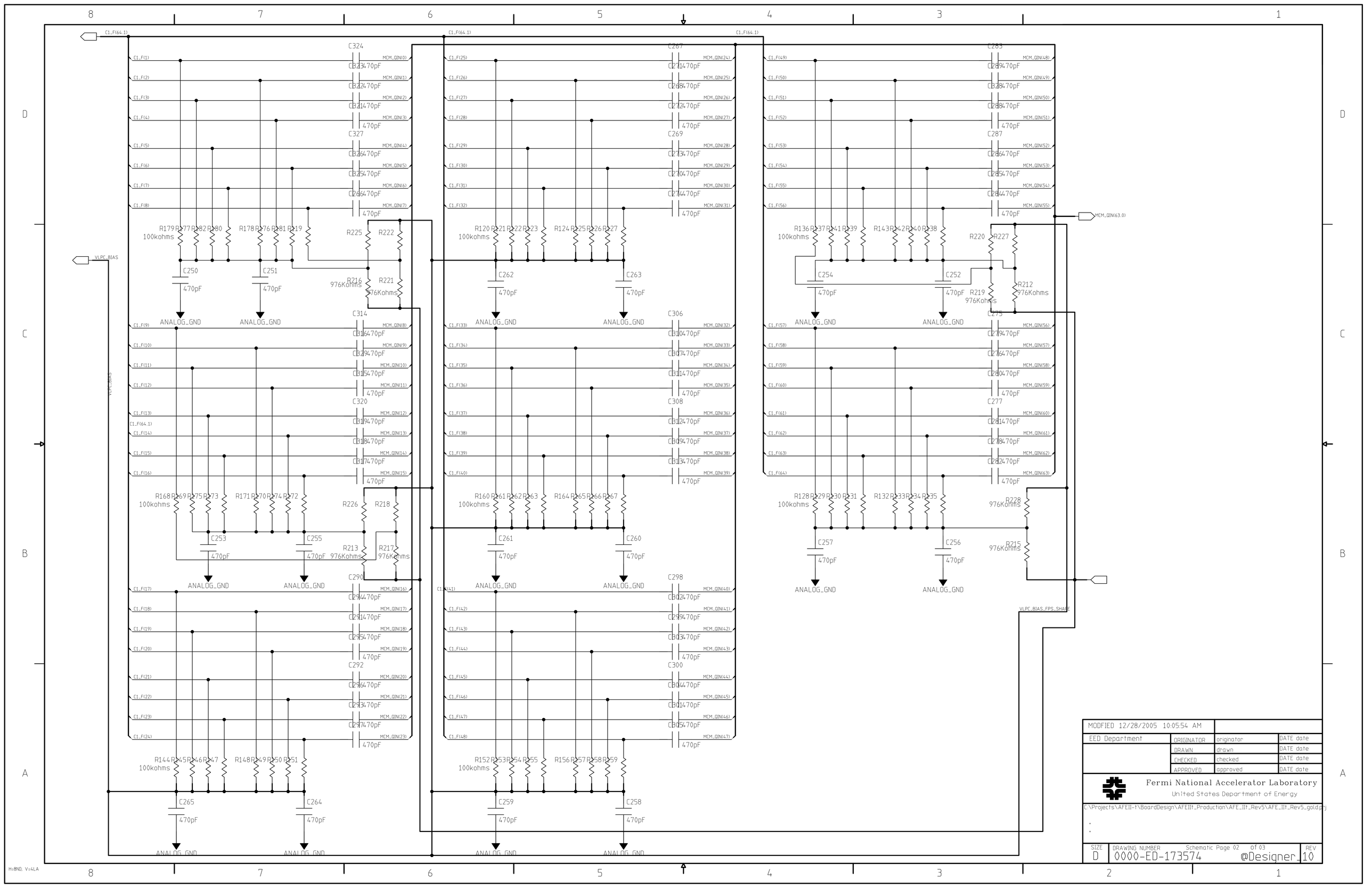
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

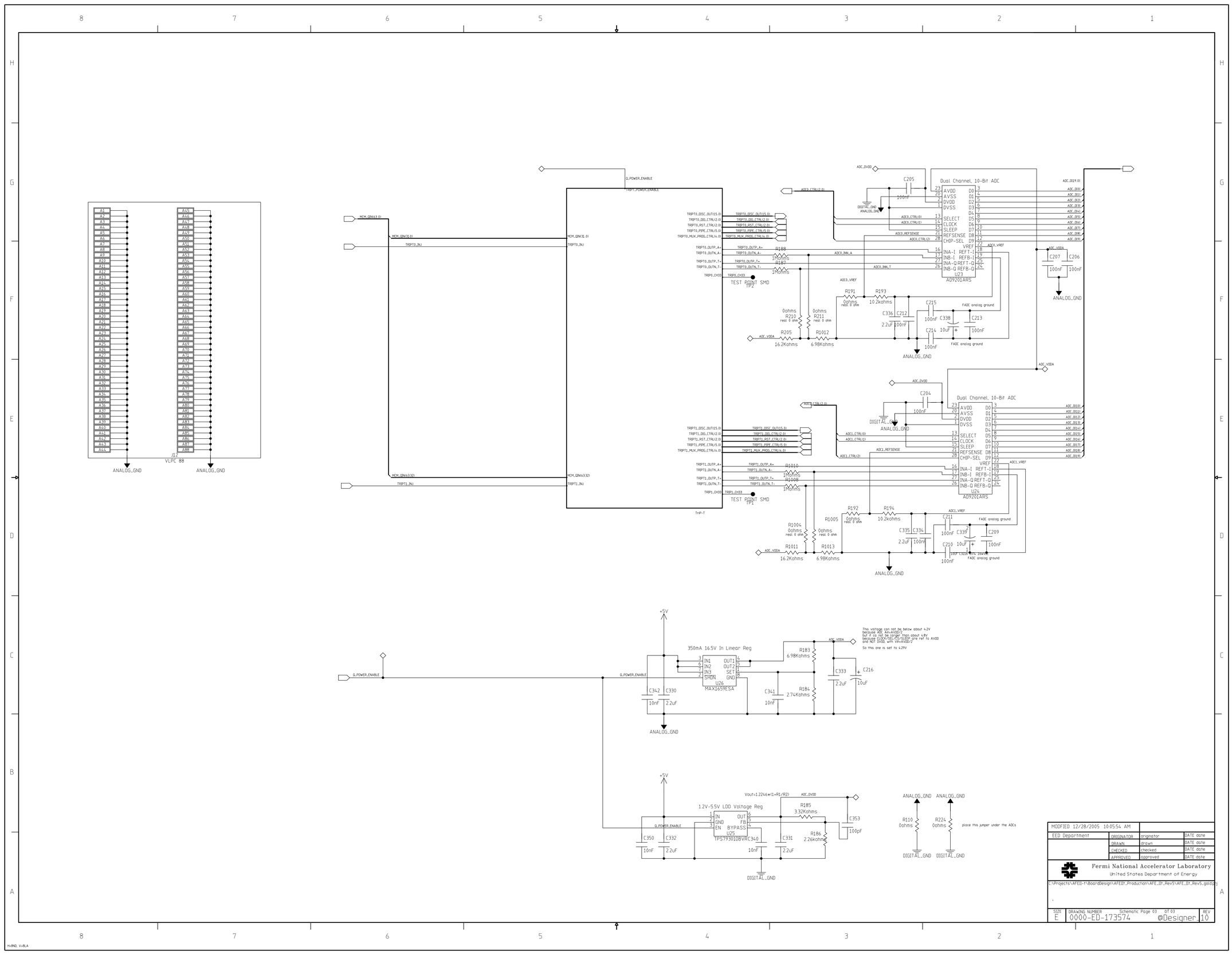
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA


ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
BAYONET_IN
ANALOG_GND
HEATER_DRV
R1000
10kohms
R107
R102
U21
TLE2062BCD
HEATER_DRIVE_OUTPUT
Heater 1 is driven by a DAC channel, local to board.
C241
C246
1nF
Decoupling for op279 amp
Cryostat heater resistor driver
J14
J13
J2
J3
VLPC 88
BAYONET_OUT
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
97.6ohms
R999
U18
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
JUMPER BERG 2PINx2.54mm
J4
47.5Kohms
R111
U22
LT1464CS8
U19
LT1167ACS8
R112
C201
100nF
R113
13kohms
3.01kohms
CRYO_25V_REF
10 uA constant current source
C239
C248
Decoupling for diff amp
C243
C247
C1_FI64.1
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R104
R116
BIAS_BEFORE_R
619ohms
R117
R101
1Kohms
1.00Kohms_1%_.063W
U20
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
BIAS_DRIVE
R1001
C240
C245
Decoupling for op495 amp
C242
C244
BIAS_READBACK
R114
R115
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
VLPC_CURRENT
MODIFIED 12/28/2005 10:05:54 AM
EED Department
ORIGINATOR
DRAWN
CHECKED
APPROVED
originator
drawn
checked
approved
DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.pcb
SIZE
D
DRAWING NUMBER
0000-ED-173574
Schematic Page 01
of 03
@Designer
REV
10
H=8ND, V=4LA



C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHAPE
ANALOG_GND
100kohms
976Kohms
470pF
MODFIED 12/28/2005 10:05:54 AM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H=8ND, V=4LA



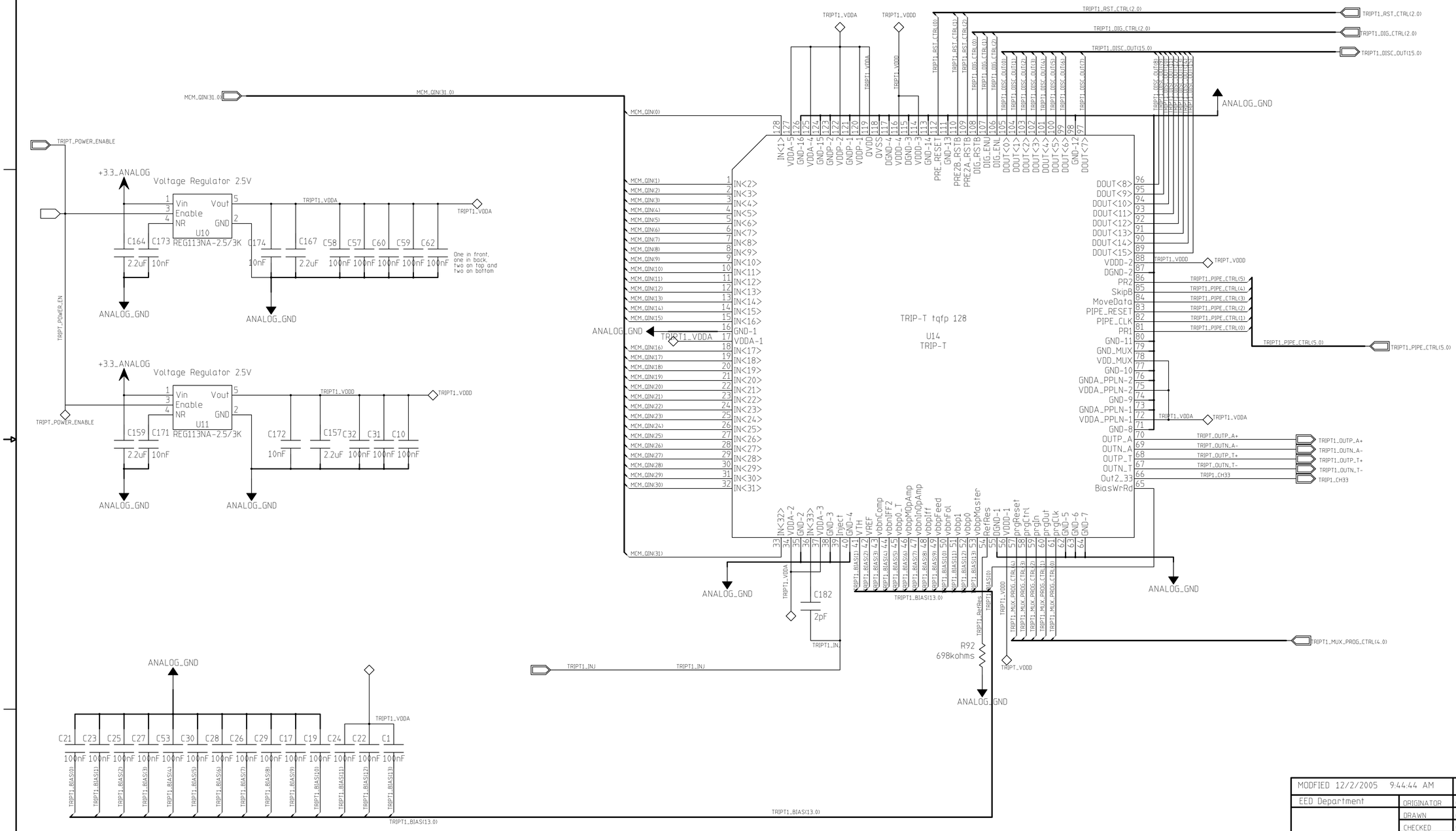
MODFIED 12/28/2005 10:05:54 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-1\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5.goldprj

SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

H=BND, V=BLA



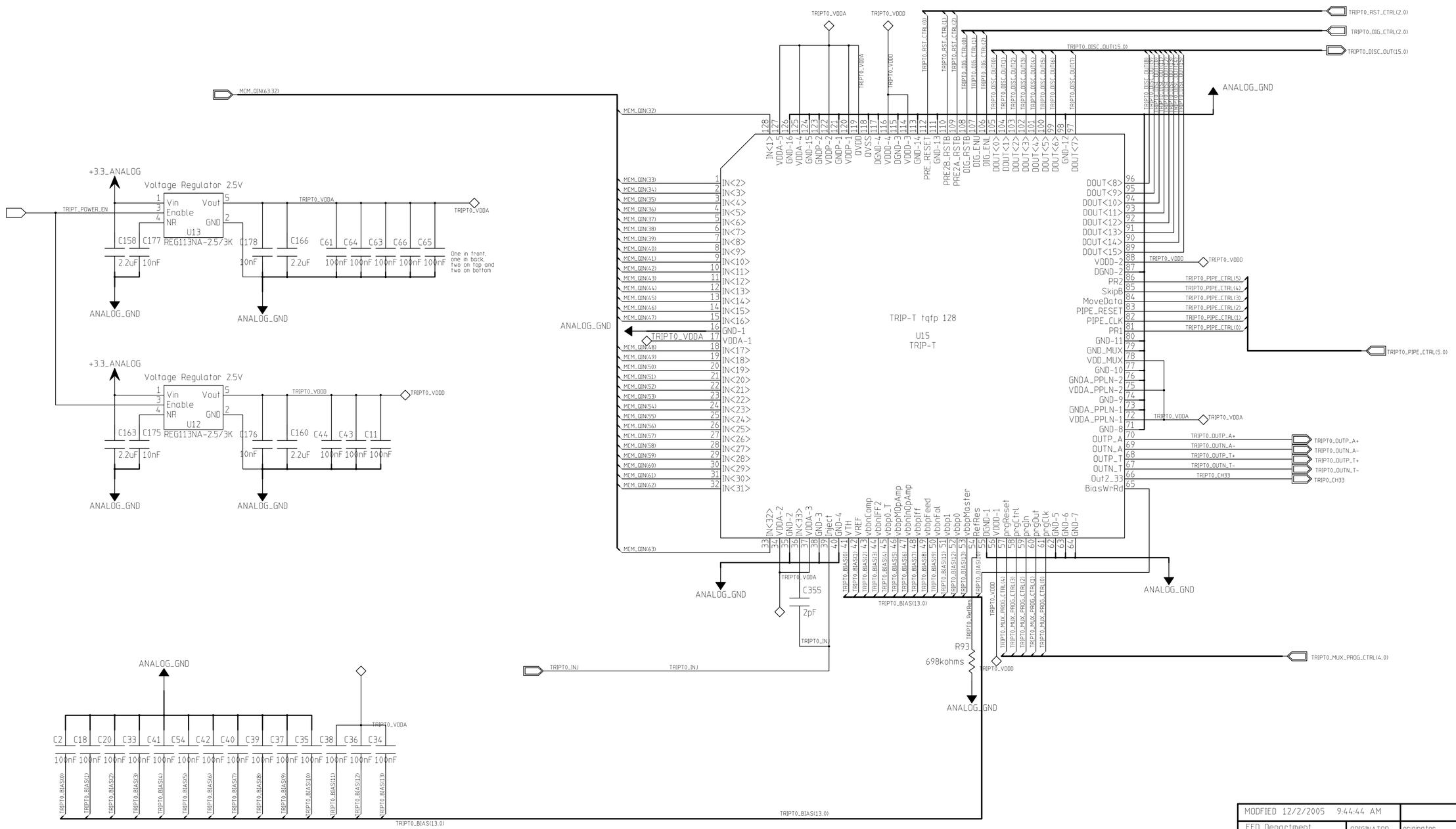
MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



MODIFIED 12/2/2005 9:44:44 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

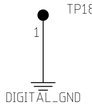
Fermi National Accelerator Laboratory
United States Department of Energy

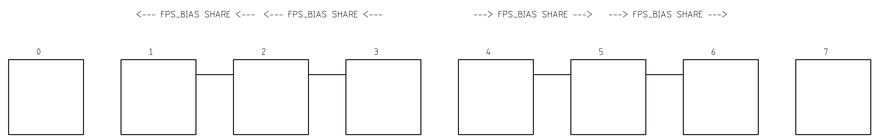
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H:8ND, V:4LA

Comments go here





Left to right:
CLOCKGEN
COLLECTOR
1553
HELPER

MODFIED 1/4/2006 1:43:30 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

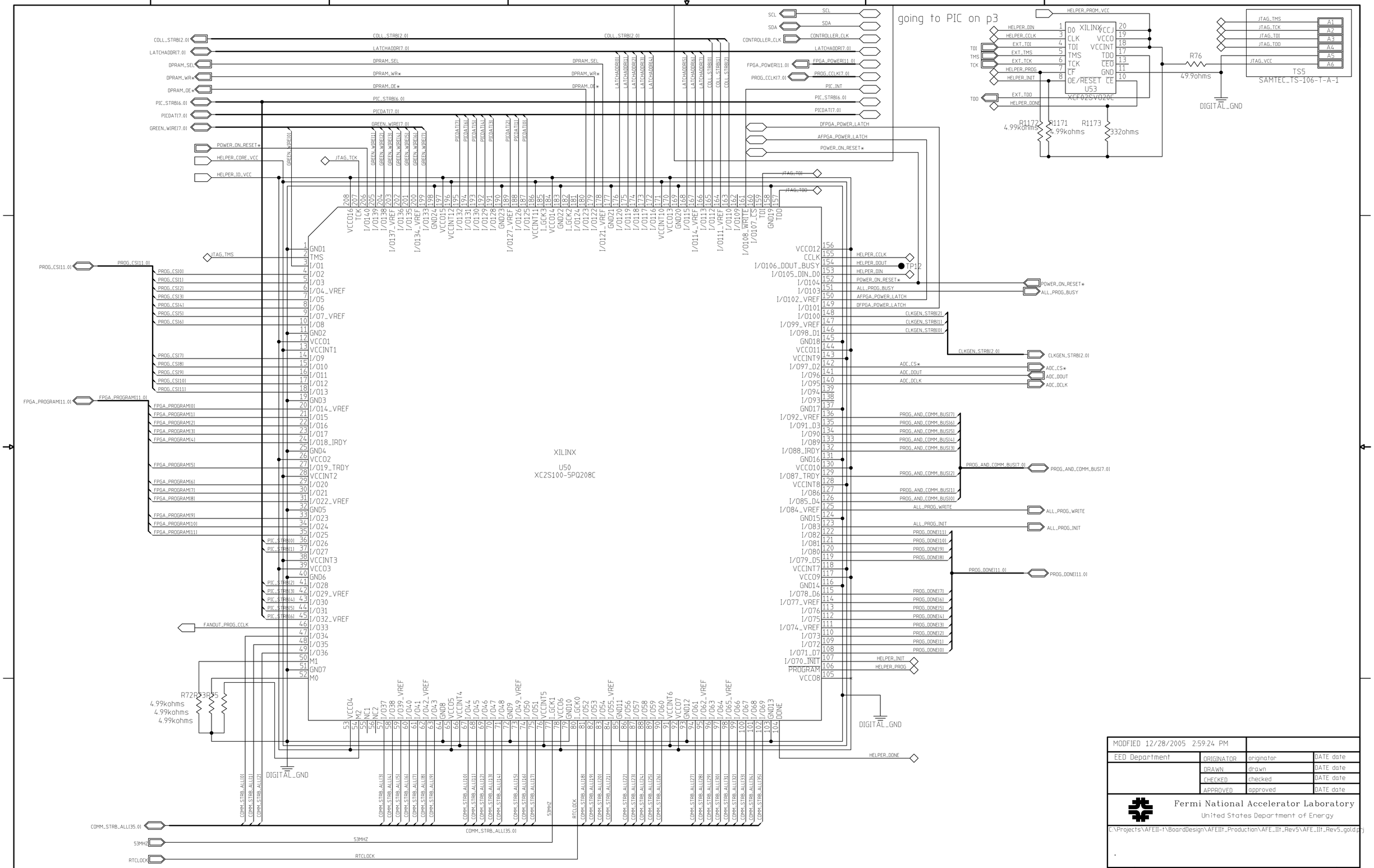
Fermi National Accelerator Laboratory
United States Department of Energy

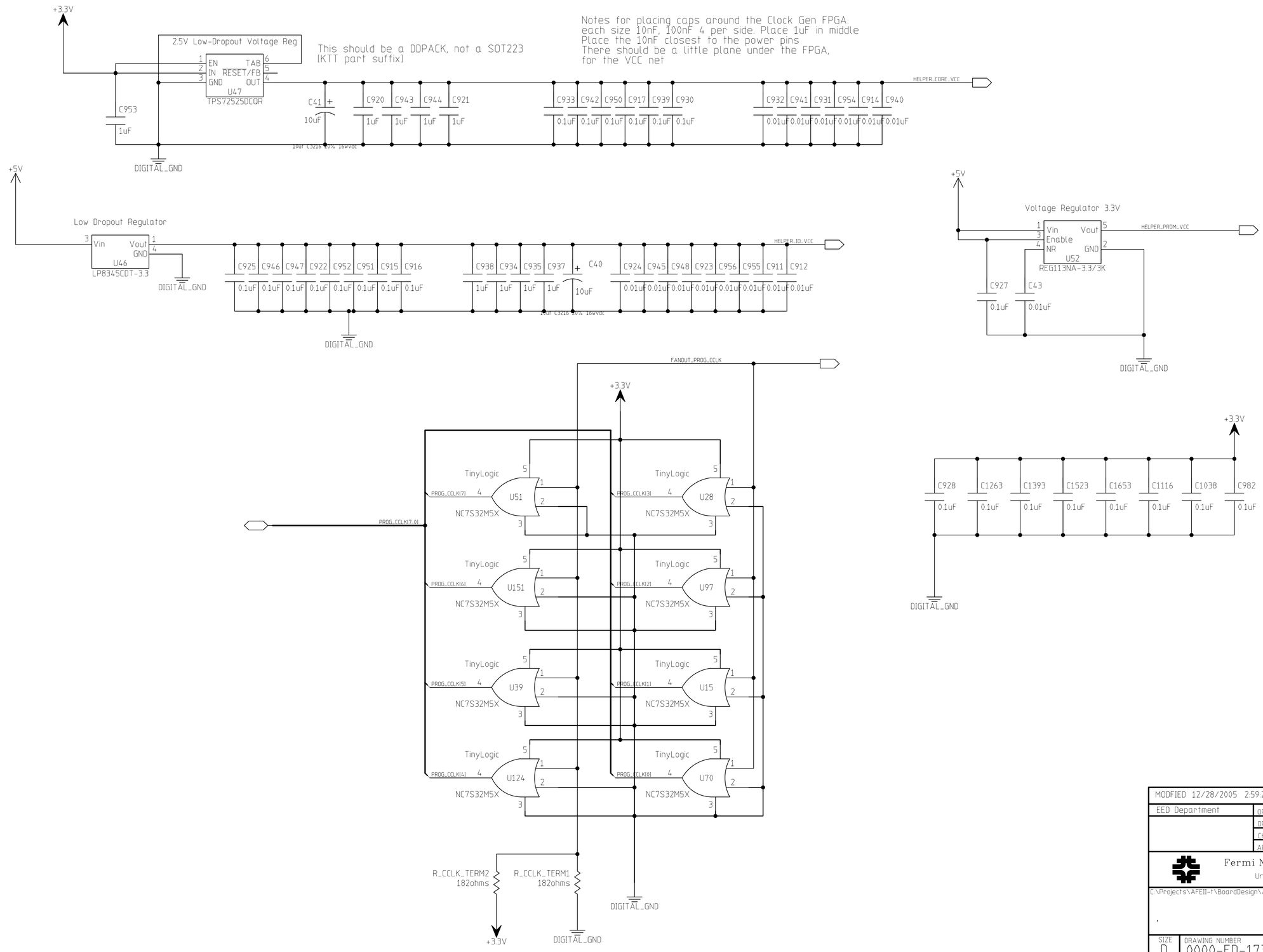
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H=8ND, V=4LA


XILINX
U50
XC2S100-5PQ208C
XILINX
U53
XCF02SVO20C
going to PIC on p3
TS5
SAMTEC_TS-106-T-A-1
R76
49.9ohms
R1172
4.99kohms
R1171
4.99kohms
R1173
332ohms
R72R73R75
4.99kohms
4.99kohms
4.99kohms
DIGITAL_GND
TP12
MODFIED 12/28/2005 2:59:24 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV
H:8ND, V:4LA



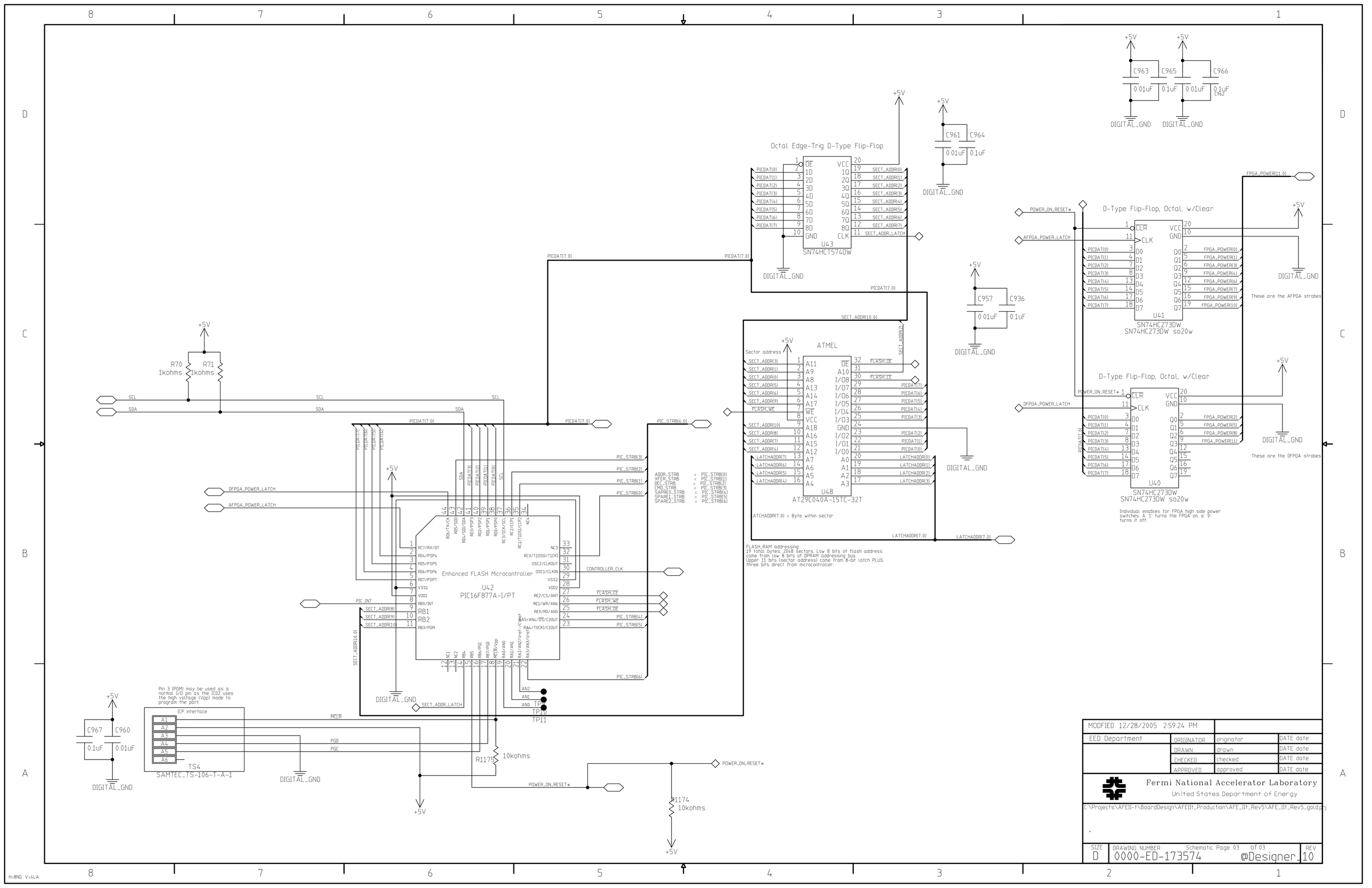
MODIFIED 12/28/2005 2:59:24 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

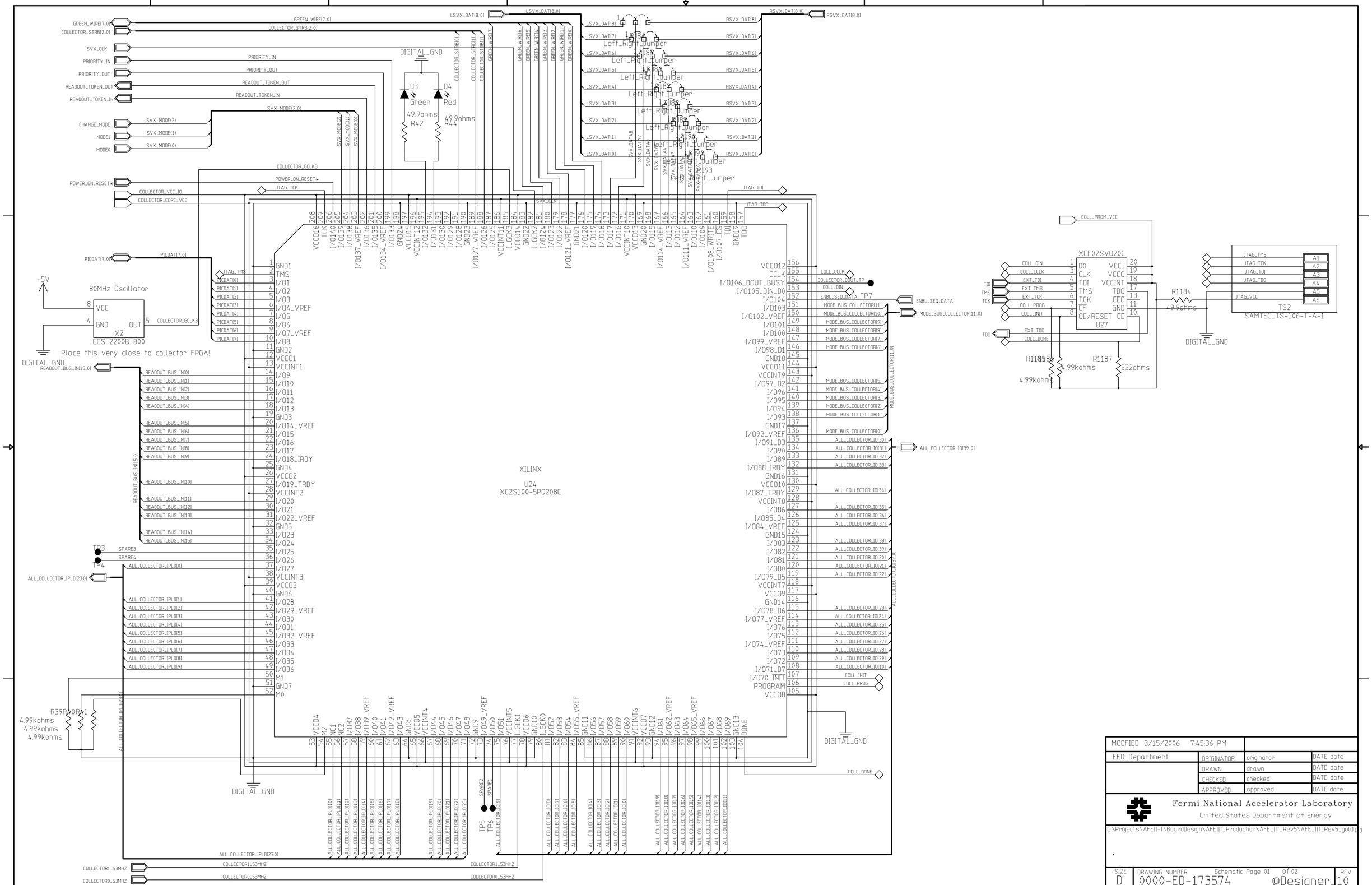
C:\Projects\AFEII-1\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_1	0

H:8ND; V:4LA



Octal Edge-Trig D-Type Flip-Flop
U43
SN74HCT574DW
ATMEL
U48
AT29C040A-15TC-32T
Sector address
D-Type Flip-Flop, Octal, w/Clear
U41
SN74HC273DW
SN74HC273DW so20w
D-Type Flip-Flop, Octal, w/Clear
U40
SN74HC273DW
SN74HC273DW so20w
These are the AFPGA strobes
These are the DFPGA strobes
Individual enables for FPGA high side power switches. A '1' turns the FPGA on, a '0' turns it off.
FLASH_RAM addressing.
19 total bytes, 2048 sectors. Low 8 bits of flash address come from low 8 bits of DPRAM addressing bus.
Upper 11 bits (sector address) come from 8-bit latch PLUS three bits direct from microcontroller.
Enhanced FLASH Microcontroller
U42
PIC16F877A-I/PT
ICP interface
TS4
SAMTEC_TS-106-T-A-1
Pin 3 (PGM) may be used as a normal I/O pin as the ICD2 uses the high voltage (Vpp) mode to program the part.
R70 1kohms
R71 1kohms
R1175 10kohms
R1174 10kohms
C967 0.1uF
C960 0.01uF
C963 0.01uF
C965 0.1uF
C966 0.01uF
C962 0.1uF
C961 0.01uF
C964 0.1uF
C957 0.01uF
C936 0.1uF
DIGITAL_GND
+5V
MODIFIED 12/28/2005 2:59:24 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 03 of 03
@Designer_10
REV 10



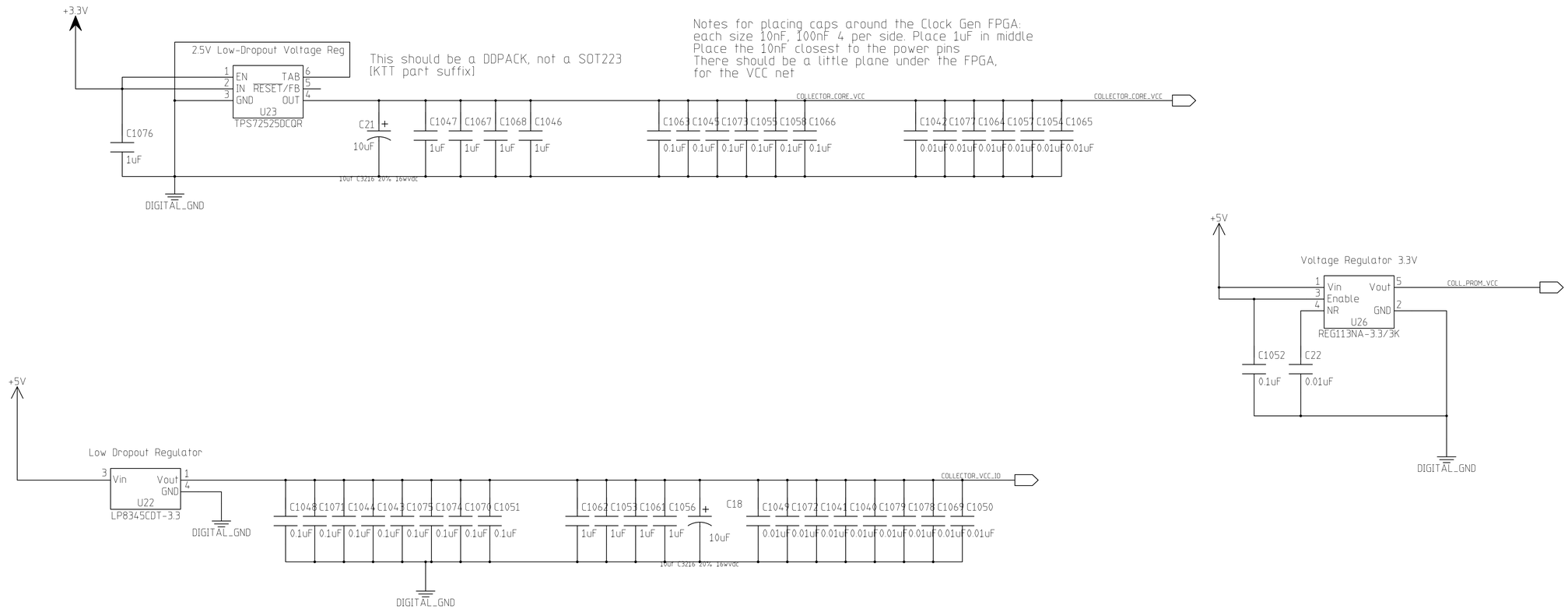
MODIFIED 3/15/2006 7:45:36 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H:8ND, V:4LA



MODFIED 3/15/2006 7:45:36 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

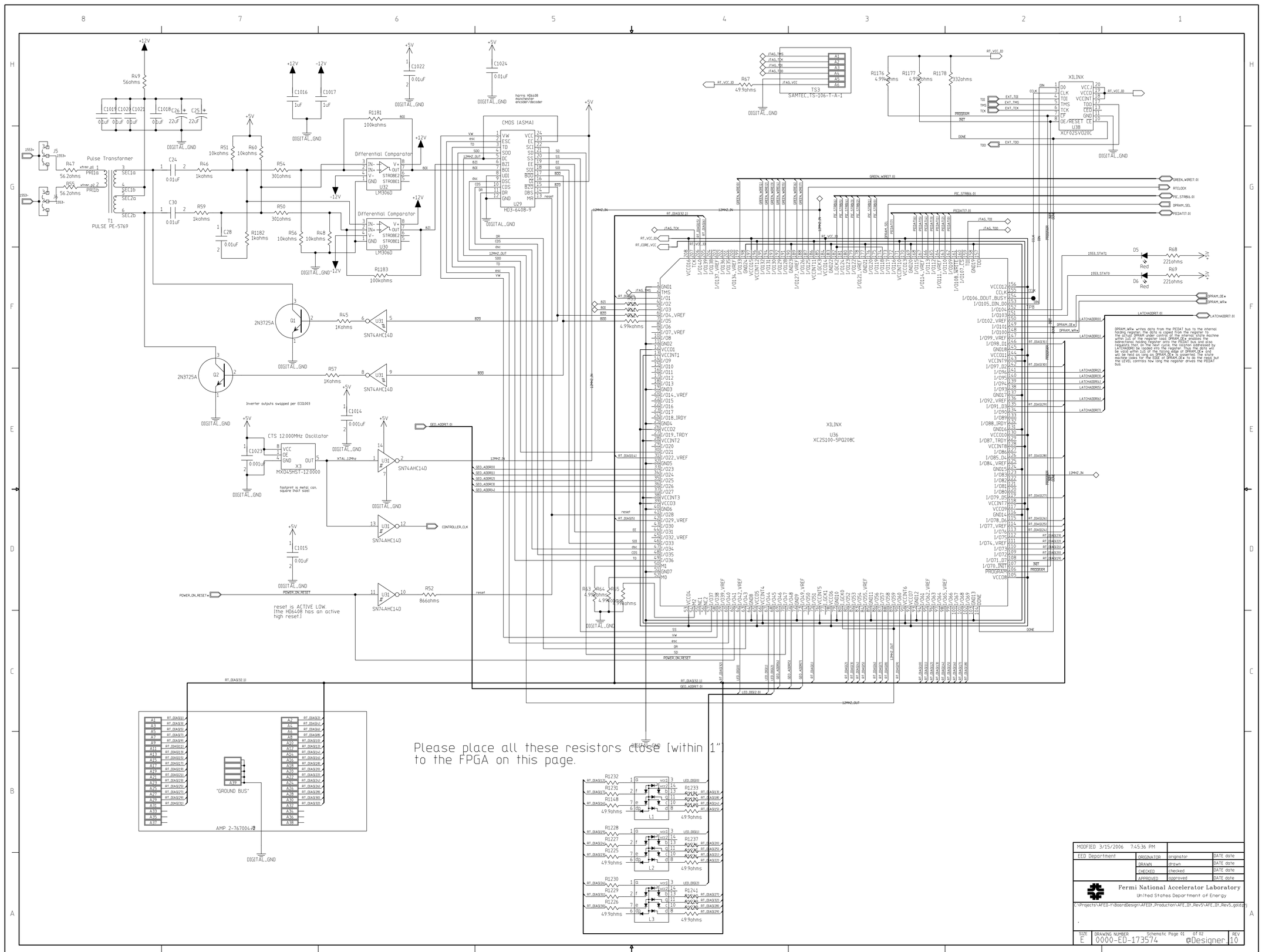
Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

H:8ND, V:4LA

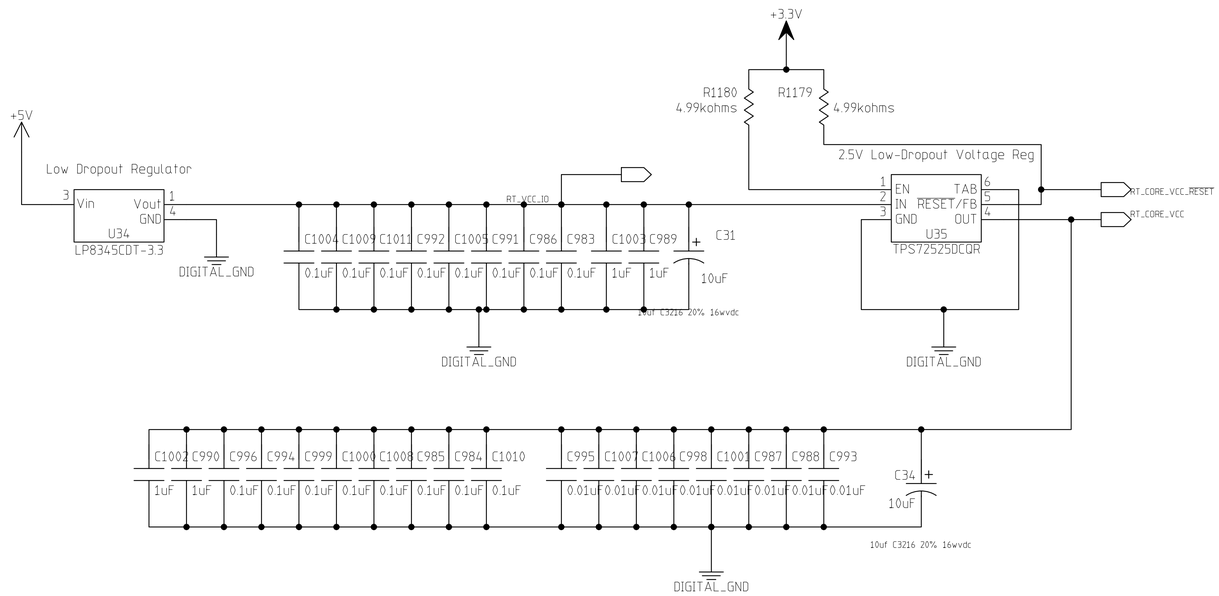


MODFIED 3/15/2006 7:45:36 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-1\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5.goldprj

SIZE	DRAWING NUMBER	Schematic Page 01 of 02	REV
E	0000-ED-173574	@Designer_10	



MODFIED 3/15/2006 7:45:36 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

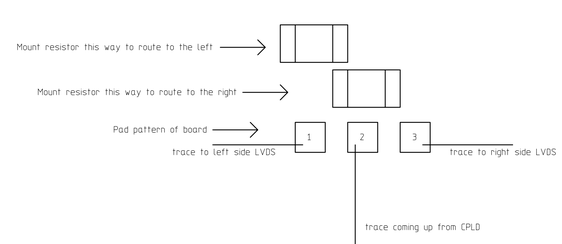
C:\Projects\AFEII-1\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA

All jumpers are actually 3-pin pad arrays designed to allow installation of a low-resistance 0402 resistor either between pads 1 and 2 or pads 3 and 4 manually routing all eighty bits of the bus to the left-side LDVS drivers or to the right side LVDS drivers. This break removes the long stubs to the unused side allowing the unused side to be unstuffed and eliminating reflection possibilities.

Blowup sketch of how this works



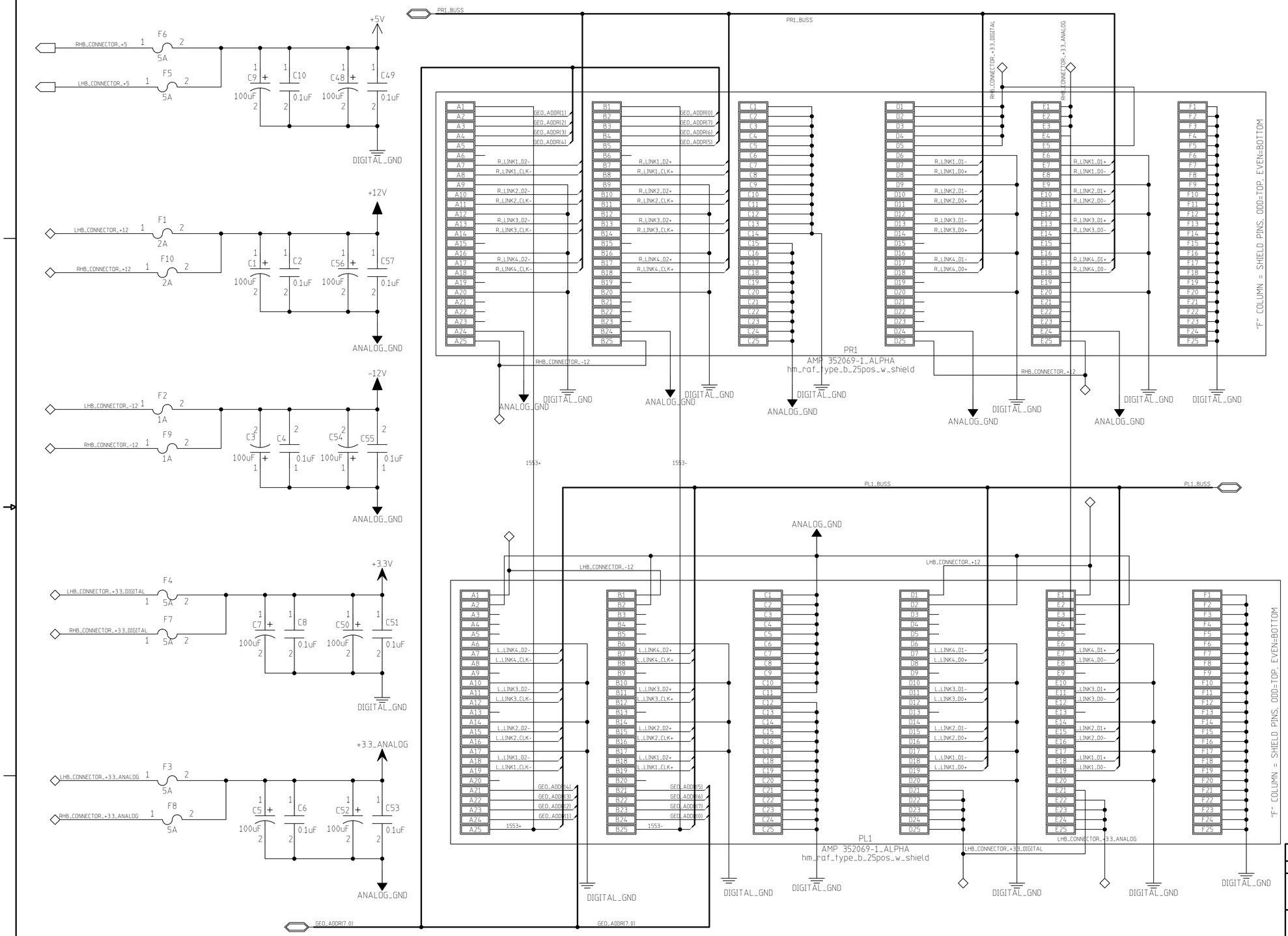
MODIFIED 3/15/2006 7:45:38 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H:8ND, V:4LA



MODIFIED 12/28/2005 2:59.22 PM

EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer	10

H=8ND; V=4LA

LEFT HAND INSERTION INTO BACKPLANE
PINOUT AS VIEWED FROM BOARD COMPONENT SIDE

CONNECTOR P1

	A	B	C	D	E	
			GND			25
			GND			24
			GND			22
			GND			21
			GND			20
			GND			19
			GND			18
			GND			18
	GND	GND	GND	GND	GND	17
			GND			16
			GND			15
	GND	GND	GND	GND	GND	14
			GND			13
			GND			12
			GND			11
	GND	GND	GND	GND	GND	10
			GND			9
			GND			8
			GND			7
	GND	GND	GND	GND	GND	6
			GND			5
			GND			4
			GND			3
	GND	GND	GND	GND	GND	2
	-12V	-12V	GND	+12V	+12V	1

RIGHT HAND INSERTION INTO BACKPLANE
PINOUT AS VIEWED FROM BOARD COMPONENT SIDE

CONNECTOR P1

	E	D	C	B	A
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					

CONNECTOR P2

	A	B	C	D	E	
25						25
24						24
22						22
21						21
20						20
19						19
18						18
17						17
16						16
15						15

	A	B	C	D	E	
11						11
10						10
9						9
8						8
7						7
6						6
5						5
4						4
3						3
2						2
1						1

CONNECTOR P2

	E	D	C	B	A
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					

	E	D	C	B	A
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					

MODFIED 12/28/2005 2:59:22 PM

EED Department			
	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

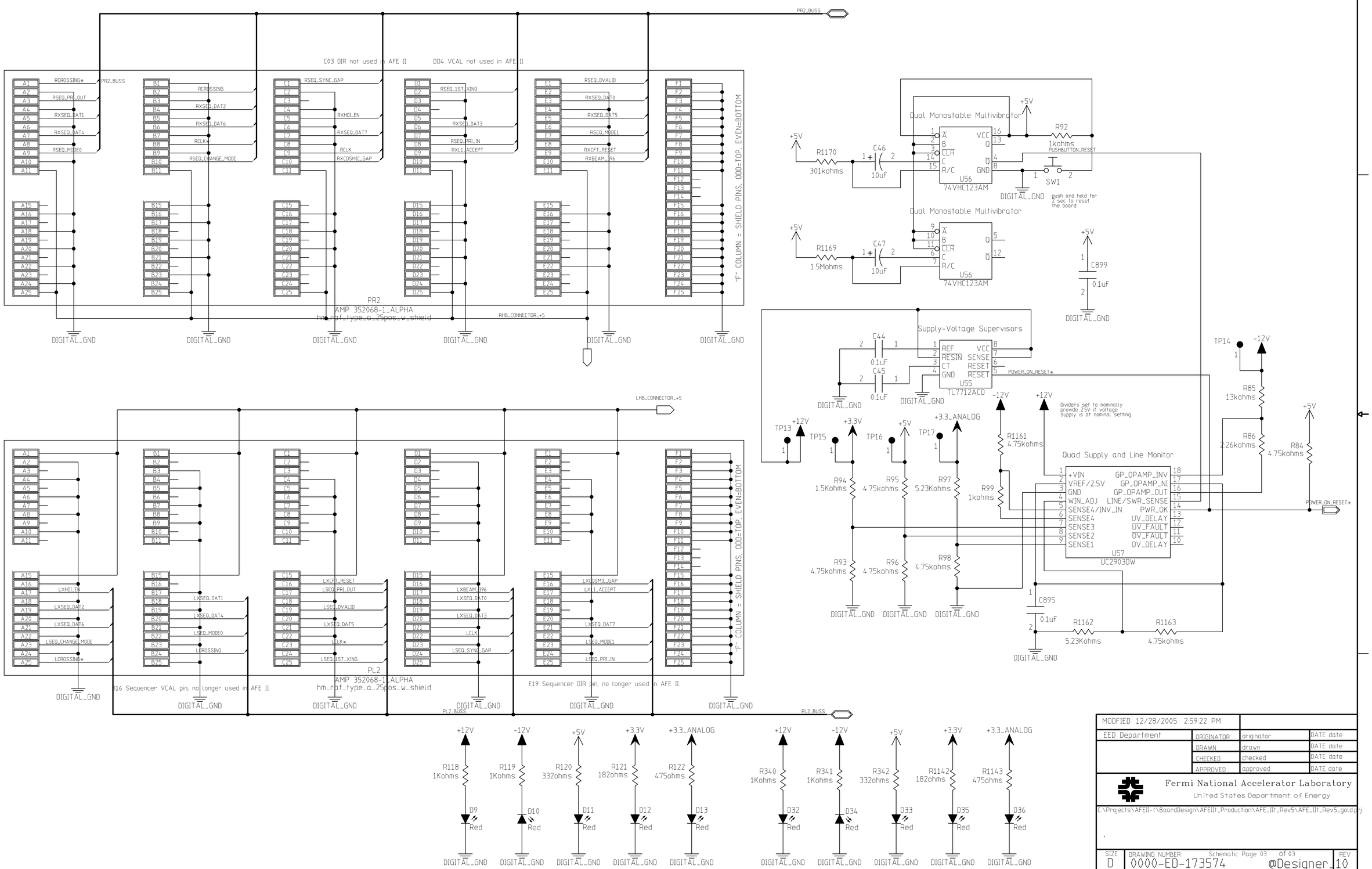
Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H:8ND, V:4LA



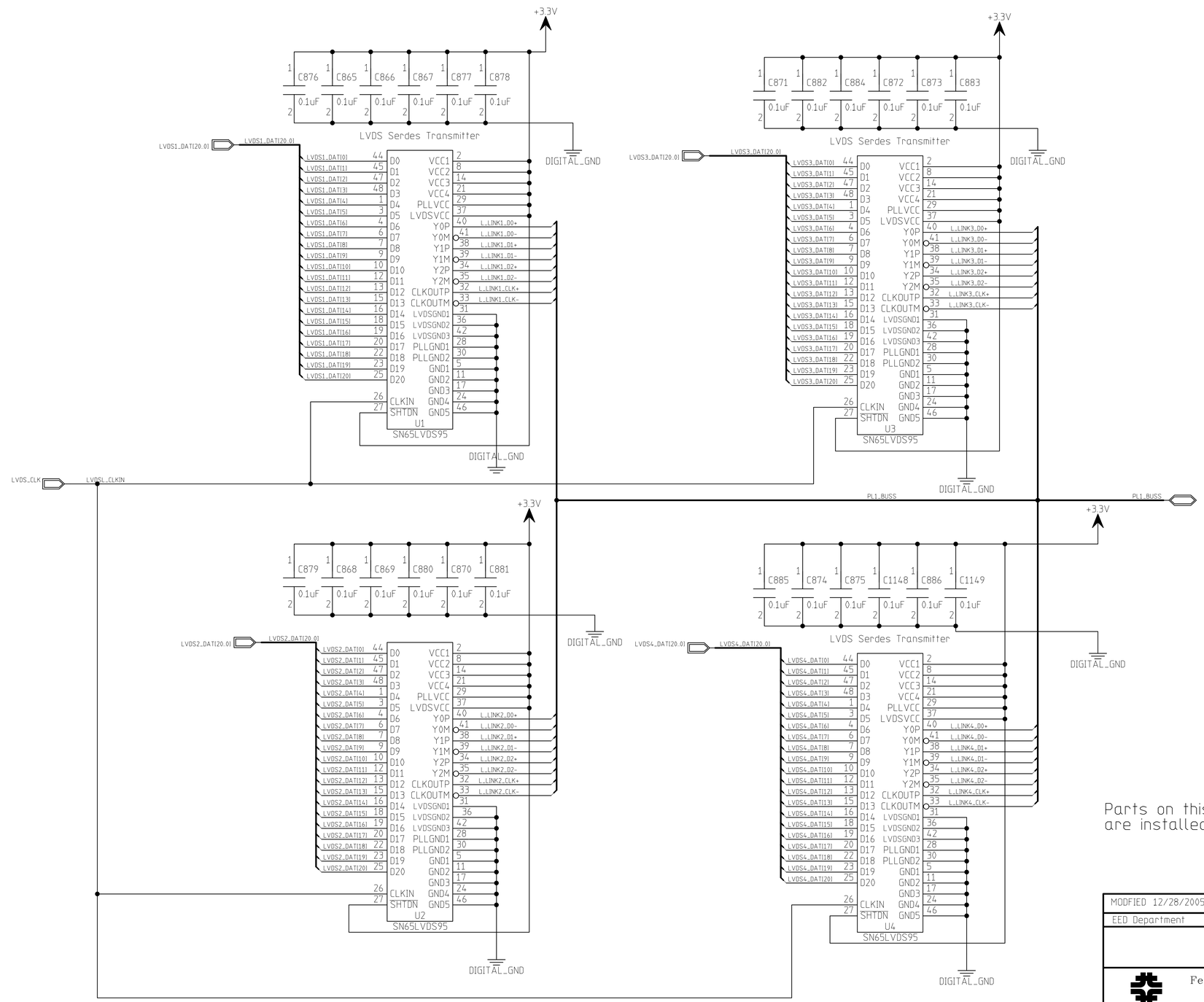
MODFIED 12/28/2005 2:59:22 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 03 of 03	@Designer_10

H=8ND, V=4LA



Parts on this page, if installed, are installed onto left-hand

MODFIED 12/28/2005 2:59:18 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

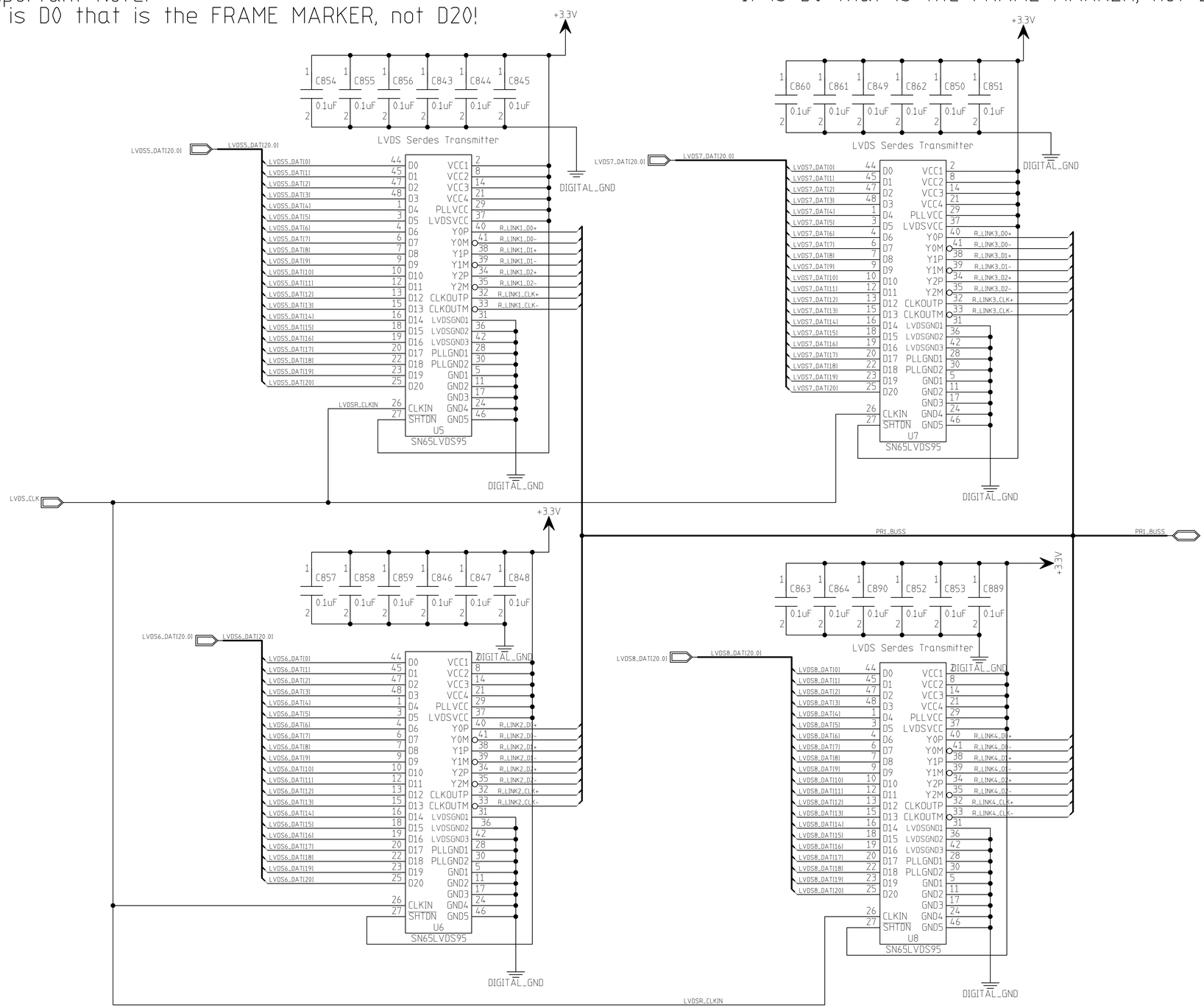
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	0

H=8ND, V=4LA

Important Note:
It is D0 that is the FRAME MARKER, not D20!

Important Note:
It is D0 that is the FRAME MARKER, not D20!



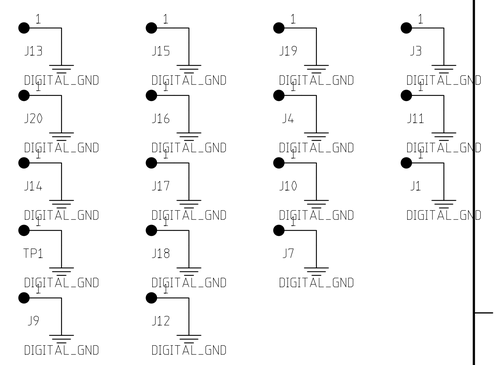
MODIFIED 12/28/2005 2:59:20 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer	10

H=8ND; V=4LA



MODFIED 3/15/2006 7:45:42 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

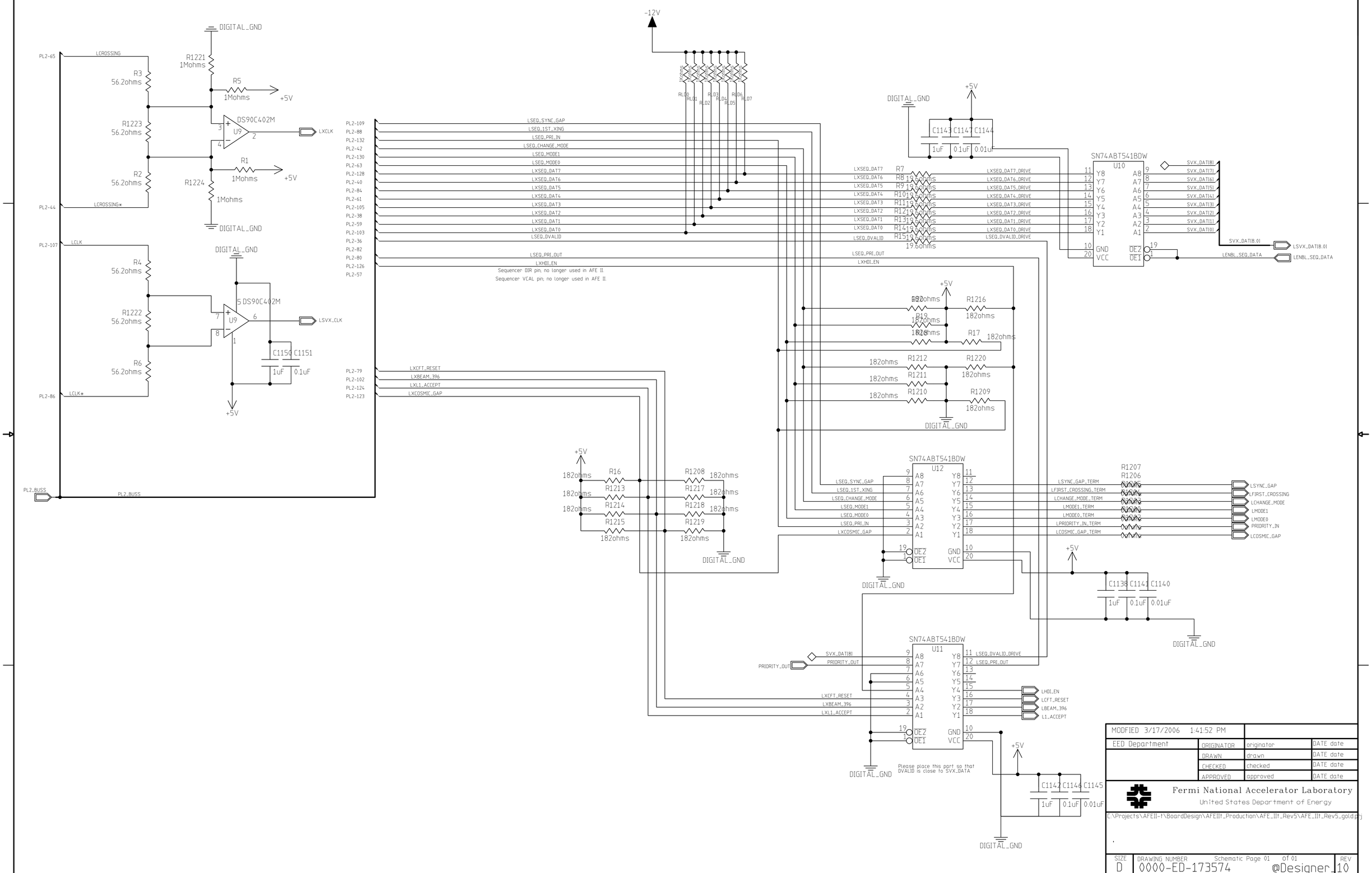
Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer	10

H:8ND, V:4LA



MODIFIED 3/17/2006 1:41:52 PM

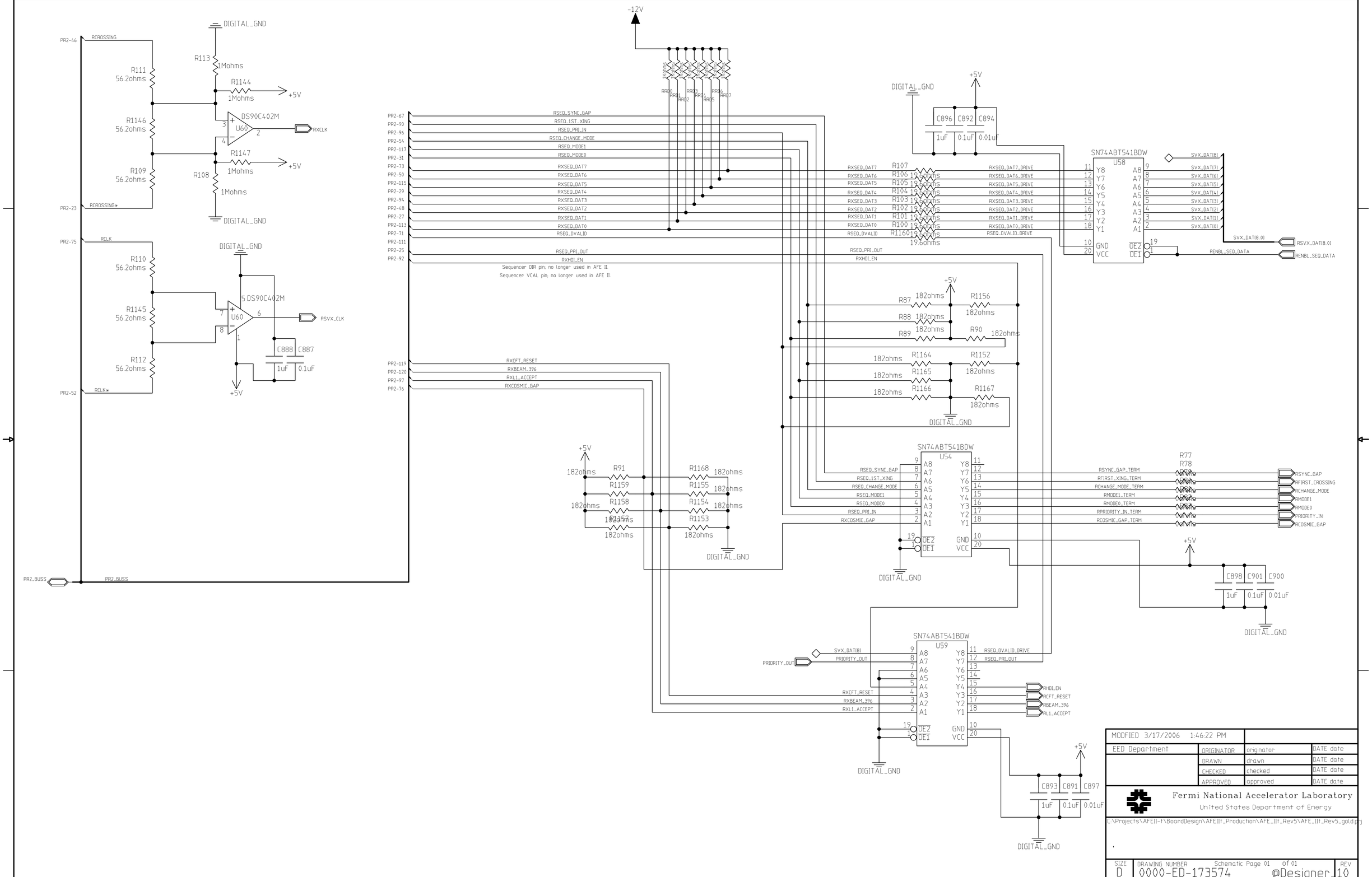
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

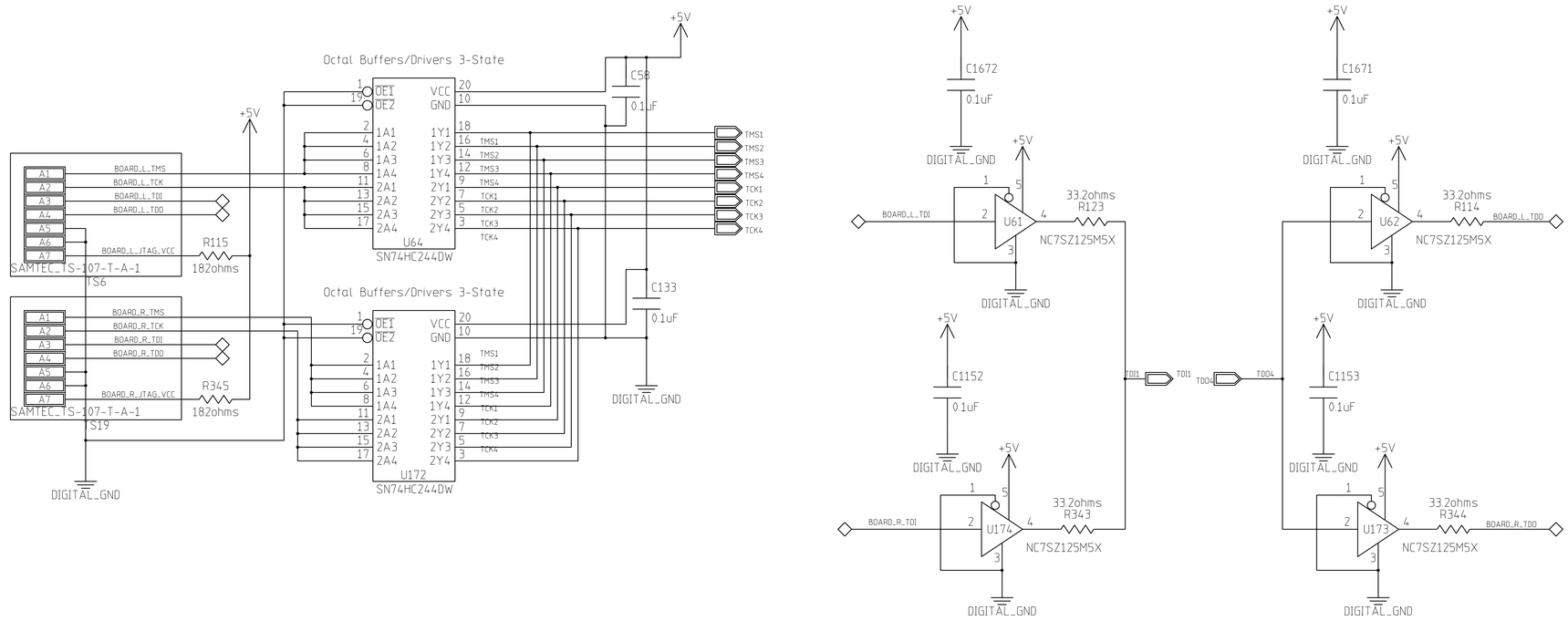
Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	0

H:8ND, V:4LA


DIGITAL_GND
PR2-46
RCROSSING
R111
56.2ohms
R113
1Mohms
R1144
1Mohms
+5V
R1146
56.2ohms
DS90C402M
U60
RXCLK
R1147
1Mohms
+5V
R109
56.2ohms
R108
1Mohms
PR2-23
RCROSSING*
DIGITAL_GND
PR2-75
RCLK
R110
56.2ohms
DIGITAL_GND
DS90C402M
U60
RSVX_CLK
R1145
56.2ohms
C888
C887
1uF
0.1uF
R112
56.2ohms
+5V
PR2-52
RCLK*
PR2_BUSS
PR2_BUSS
-12V
RR0
RR1
RR2
RR3
RR4
RR5
RR6
RR7
PR2-67
RSEQ_SYNC_GAP
PR2-90
RSEQ_1ST_XING
PR2-96
RSEQ_PRI_IN
PR2-54
RSEQ_CHANGE_MODE
PR2-117
RSEQ_MODE1
PR2-31
RSEQ_MODE0
PR2-73
RXSEQ_DAT7
PR2-50
RXSEQ_DAT6
PR2-115
RXSEQ_DAT5
PR2-29
RXSEQ_DAT4
PR2-94
RXSEQ_DAT3
PR2-48
RXSEQ_DAT2
PR2-27
RXSEQ_DAT1
PR2-113
RXSEQ_DAT0
PR2-71
RSEQ_DVALID
PR2-111
PR2-25
RSEQ_PRI_OUT
PR2-92
RXHDI_EN
Sequencer DIR pin; no longer used in AFE II.
Sequencer VCAL pin; no longer used in AFE II.
PR2-119
RXCFT_RESET
PR2-120
RXBEAM_396
PR2-97
RXL1_ACCEPT
PR2-76
RXCOSMIC_GAP
DIGITAL_GND
+5V
C896
C892
C894
1uF
0.1uF
0.01uF
RXSEQ_DAT7
R107
19.6ohms
RXSEQ_DAT6
R106
19.6ohms
RXSEQ_DAT5
R105
19.6ohms
RXSEQ_DAT4
R104
19.6ohms
RXSEQ_DAT3
R103
19.6ohms
RXSEQ_DAT2
R102
19.6ohms
RXSEQ_DAT1
R101
19.6ohms
RXSEQ_DAT0
R100
19.6ohms
RSEQ_DVALID
R116
19.6ohms
RXSEQ_DAT7_DRIVE
RXSEQ_DAT6_DRIVE
RXSEQ_DAT5_DRIVE
RXSEQ_DAT4_DRIVE
RXSEQ_DAT3_DRIVE
RXSEQ_DAT2_DRIVE
RXSEQ_DAT1_DRIVE
RXSEQ_DAT0_DRIVE
RSEQ_DVALID_DRIVE
RSEQ_PRI_OUT
RXHDI_EN
SN74ABT541BDW
U58
SVX_DAT(8)
SVX_DAT(7)
SVX_DAT(6)
SVX_DAT(5)
SVX_DAT(4)
SVX_DAT(3)
SVX_DAT(2)
SVX_DAT(1)
SVX_DAT(0)
SVX_DAT(8.0)
RSVX_DAT(8.0)
RENBL_SEQ_DATA
RENBL_SEQ_DATA
+5V
R87
182ohms
R1156
182ohms
R88
182ohms
R89
182ohms
R90
182ohms
182ohms
R1164
R1152
182ohms
182ohms
R1165
182ohms
R1166
R1167
182ohms
DIGITAL_GND
+5V
182ohms
R91
R1168
182ohms
R1159
R1155
182ohms
182ohms
R1158
R1154
182ohms
R1157
R1153
182ohms
182ohms
DIGITAL_GND
SN74ABT541BDW
U54
RSEQ_SYNC_GAP
RSEQ_1ST_XING
RSEQ_CHANGE_MODE
RSEQ_MODE1
RSEQ_MODE0
RSEQ_PRI_IN
RXCOSMIC_GAP
RSYNC_GAP_TERM
RFIRST_XING_TERM
RCHANGE_MODE_TERM
RMODE1_TERM
RMODE0_TERM
RPRIORITY_IN_TERM
RCOSMIC_GAP_TERM
R77
R78
RSYNC_GAP
RFIRST_CROSSING
RCHANGE_MODE
RMODE1
RMODE0
PRIORITY_IN
RCOSMIC_GAP
DIGITAL_GND
+5V
C898
C901
C900
1uF
0.1uF
0.01uF
DIGITAL_GND
SN74ABT541BDW
U59
SVX_DAT(8)
PRIORITY_OUT
PRIORITY_OUT
RSEQ_DVALID_DRIVE
RSEQ_PRI_OUT
RXCFT_RESET
RXBEAM_396
RXL1_ACCEPT
RHDI_EN
RCFT_RESET
RBEAM_396
RL1_ACCEPT
DIGITAL_GND
+5V
C893
C891
C897
1uF
0.1uF
0.01uF
DIGITAL_GND
MODFIED 3/17/2006 1:46:22 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 01
@Designer_10
REV
H=8ND, V=4LA



MODFIED 12/28/2005 2:50:32 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

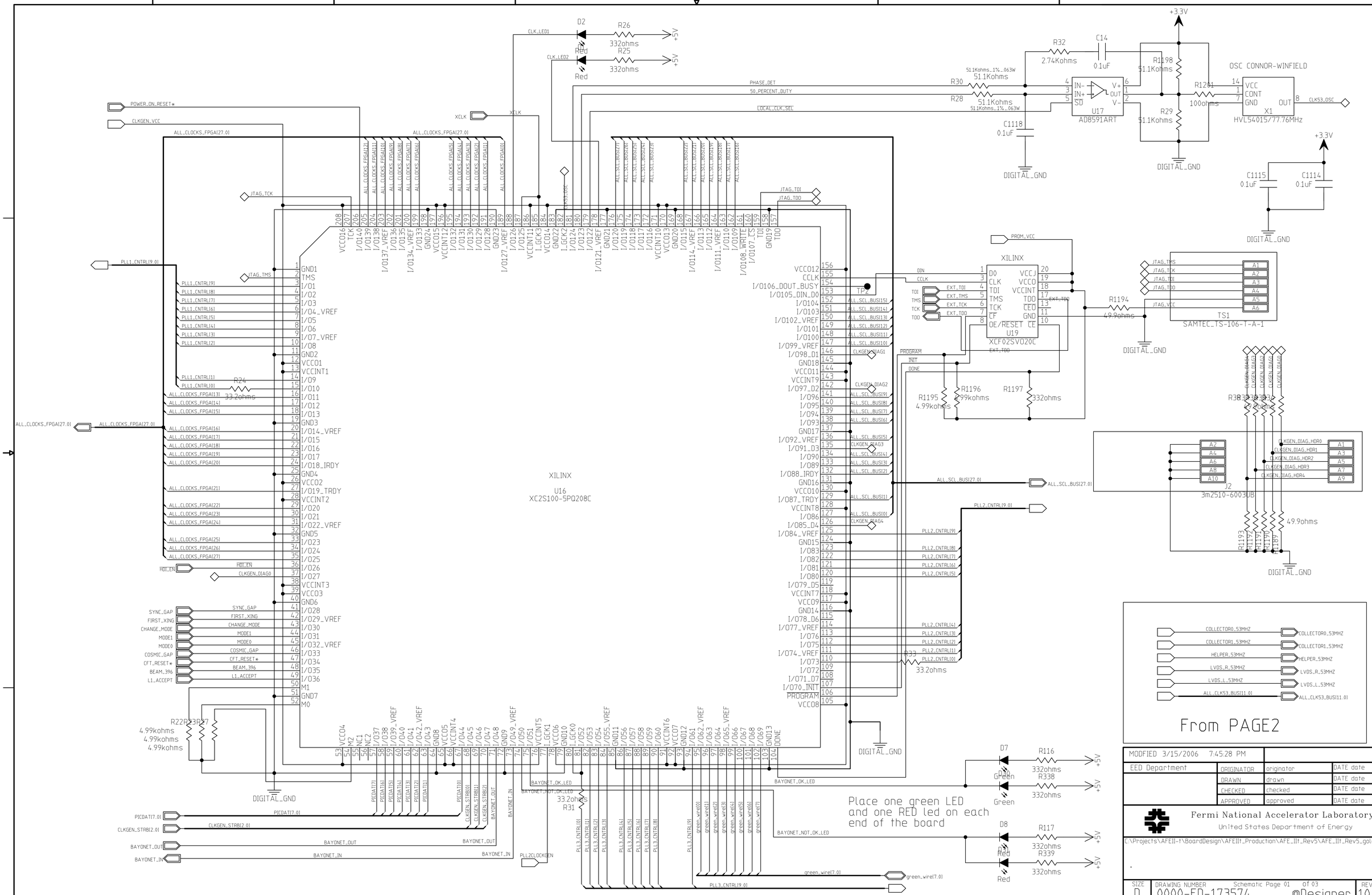
Fermi National Accelerator Laboratory
United States Department of Energy

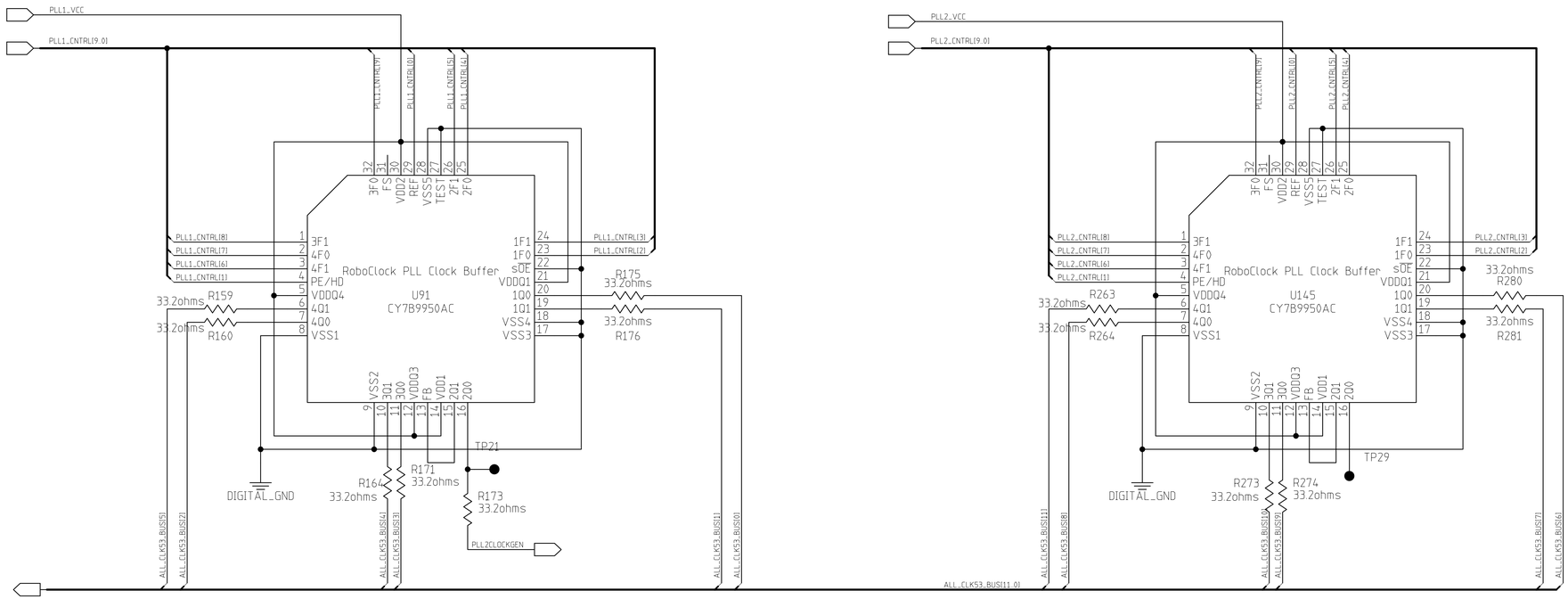
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

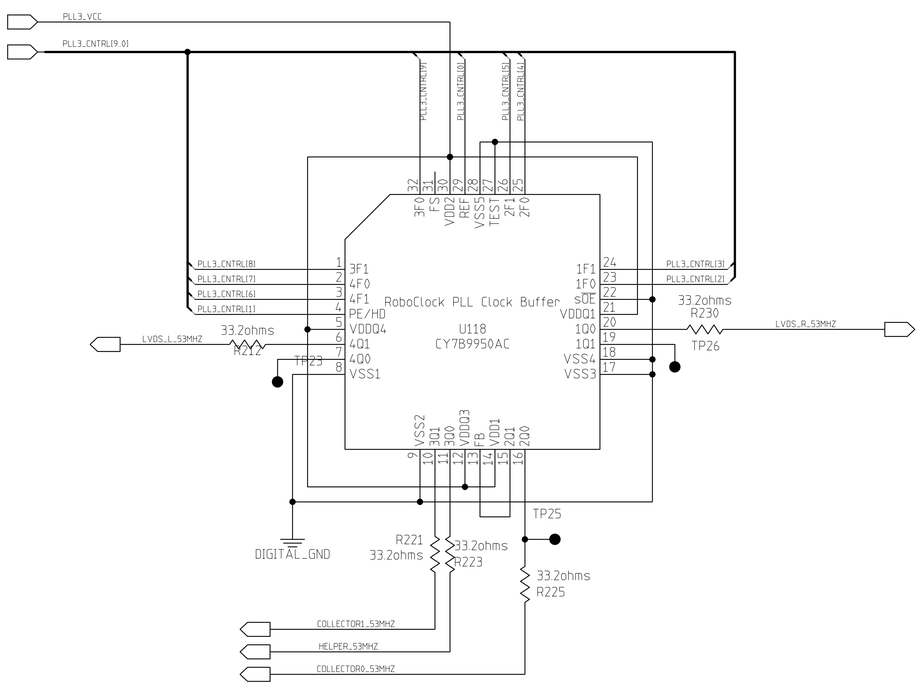
.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H:8ND, V:4LA


XILINX
U16
XC2S100-5PQ208C
XILINX
U19
XCF02SVO20C
AD8591ART
U17
OSC CONNOR-WINFIELD
X1
HVL54015/77.76MHz
SAMTEC_TS-106-1-A-1
TS1
3M2510-6003UB
J2
From PAGE2
Place one green LED and one RED led on each end of the board
DIGITAL_GND
+3.3V
+5V
MODIFIED 3/15/2006 7:45:28 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV





ALL_CLK53_BUS[11..0]

0 = AFPGA0 CLK53
1 = AFPGA1 CLK53
2 = DFPGA01 CLK53
3 = AFPGA2 CLK53
4 = AFPGA3 CLK53
5 = DFPGA23 CLK53
6 = AFPGA4 CLK53
7 = AFPGA5 CLK53
8 = DFPGA45 CLK53
9 = AFPGA6 CLK53
10 = AFPGA7 CLK53
11 = DFPGA67 CLK53

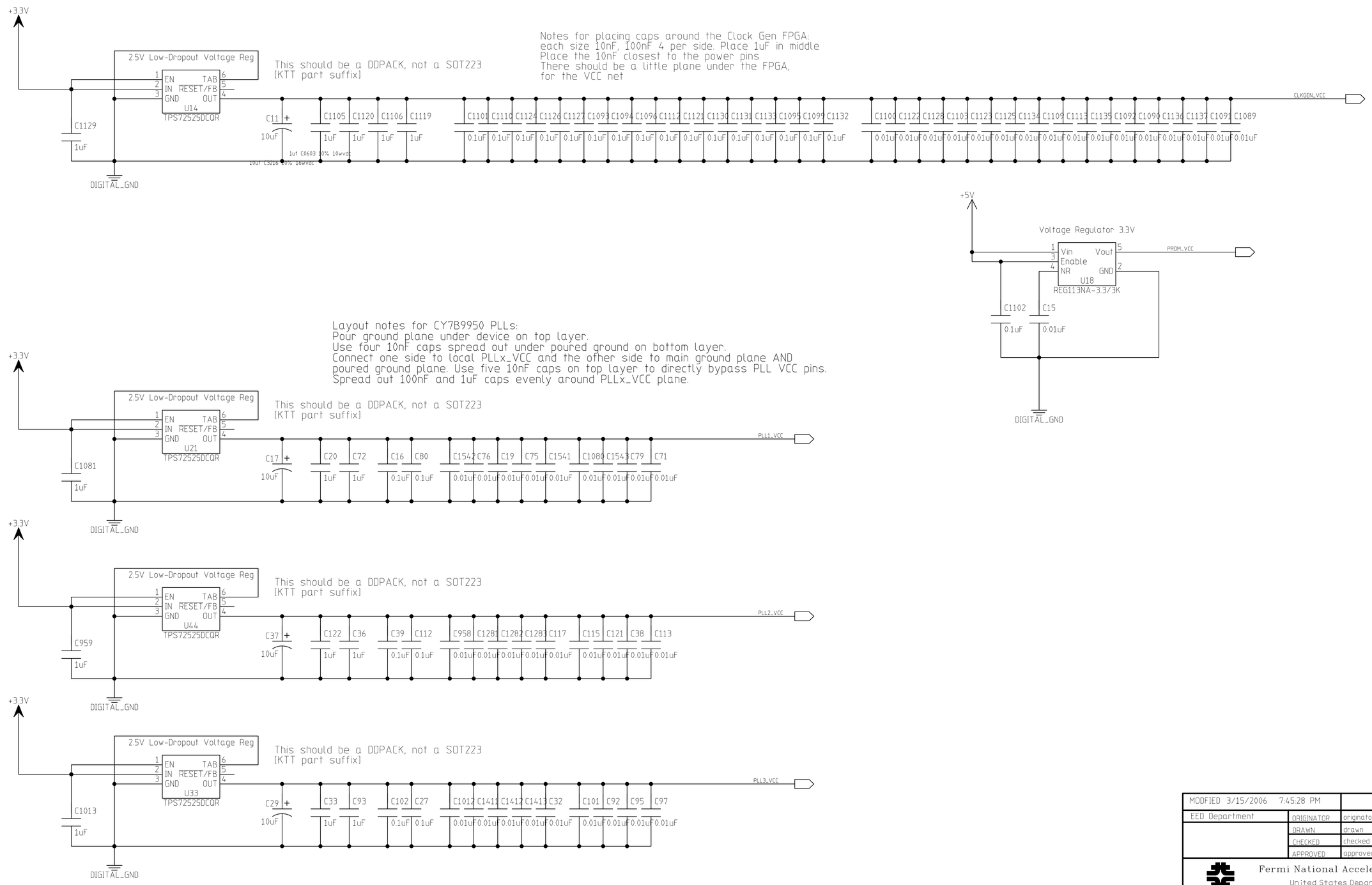
MODFIED 3/15/2006 7:45:28 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

SIZE D | DRAWING NUMBER 0000-ED-173574 | Schematic Page 02 of 03 | @Designer_10 | REV

H:8ND, V:4LA



MODFIED 3/15/2006 7:45:28 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

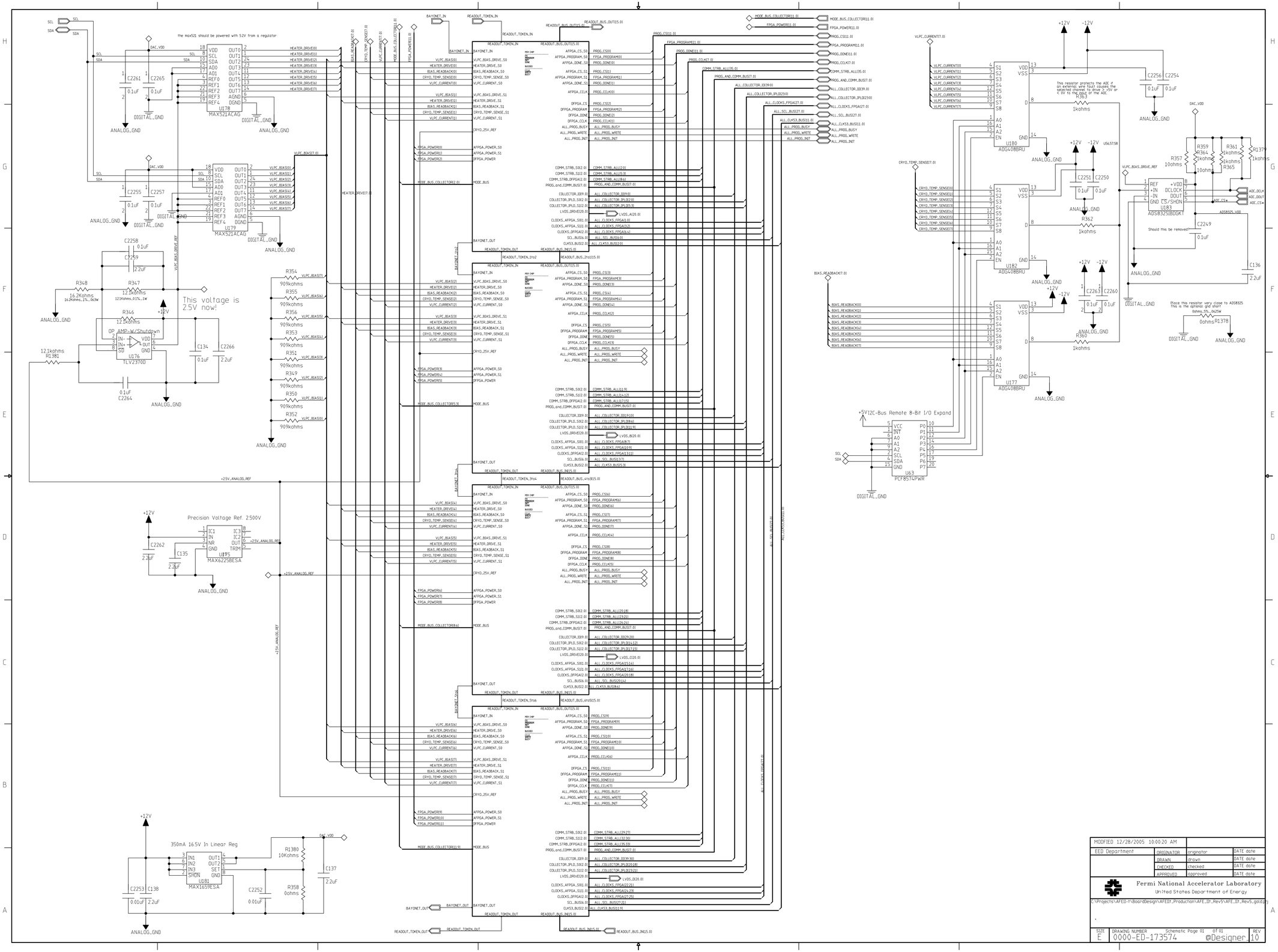
Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 03 of 03 @Designer_10	

H:8ND, V:4LA



MODIFIED 12/28/2005 10:00:20 AM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Projects\AFEII-I\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5.gpdprj

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
E	0000-ED-173574	@Designer_10	

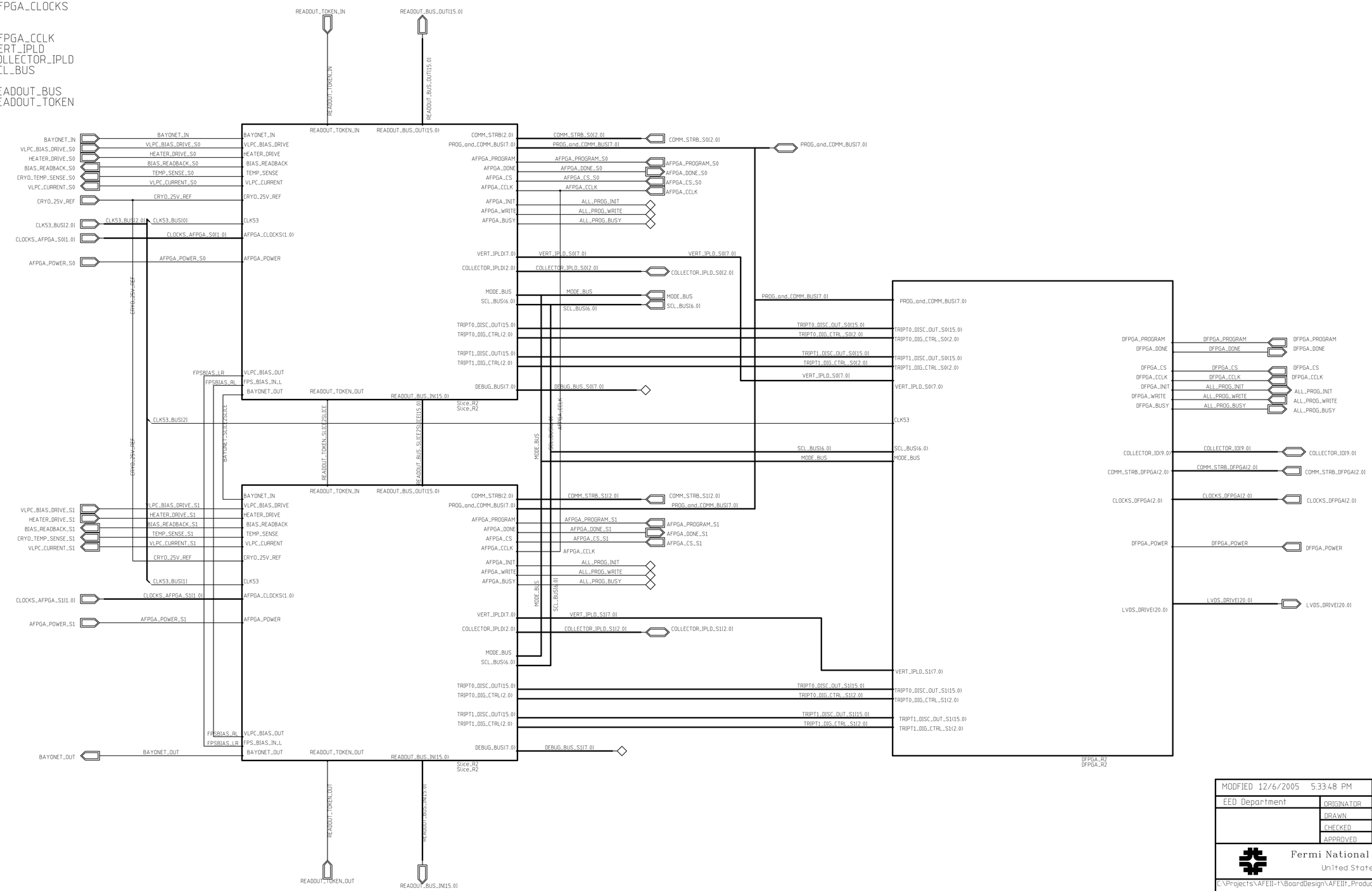
H:\BND. V:\BLA

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



MODFIED 12/6/2005 5:33:48 PM			
EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

E:\Projects\AFEII-t\BoardDesign\AFEIIt_Production\AFE_IIt_Rev5\AFE_IIt_Rev5_gold.prj

.

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	10

H=8ND, V=4LA