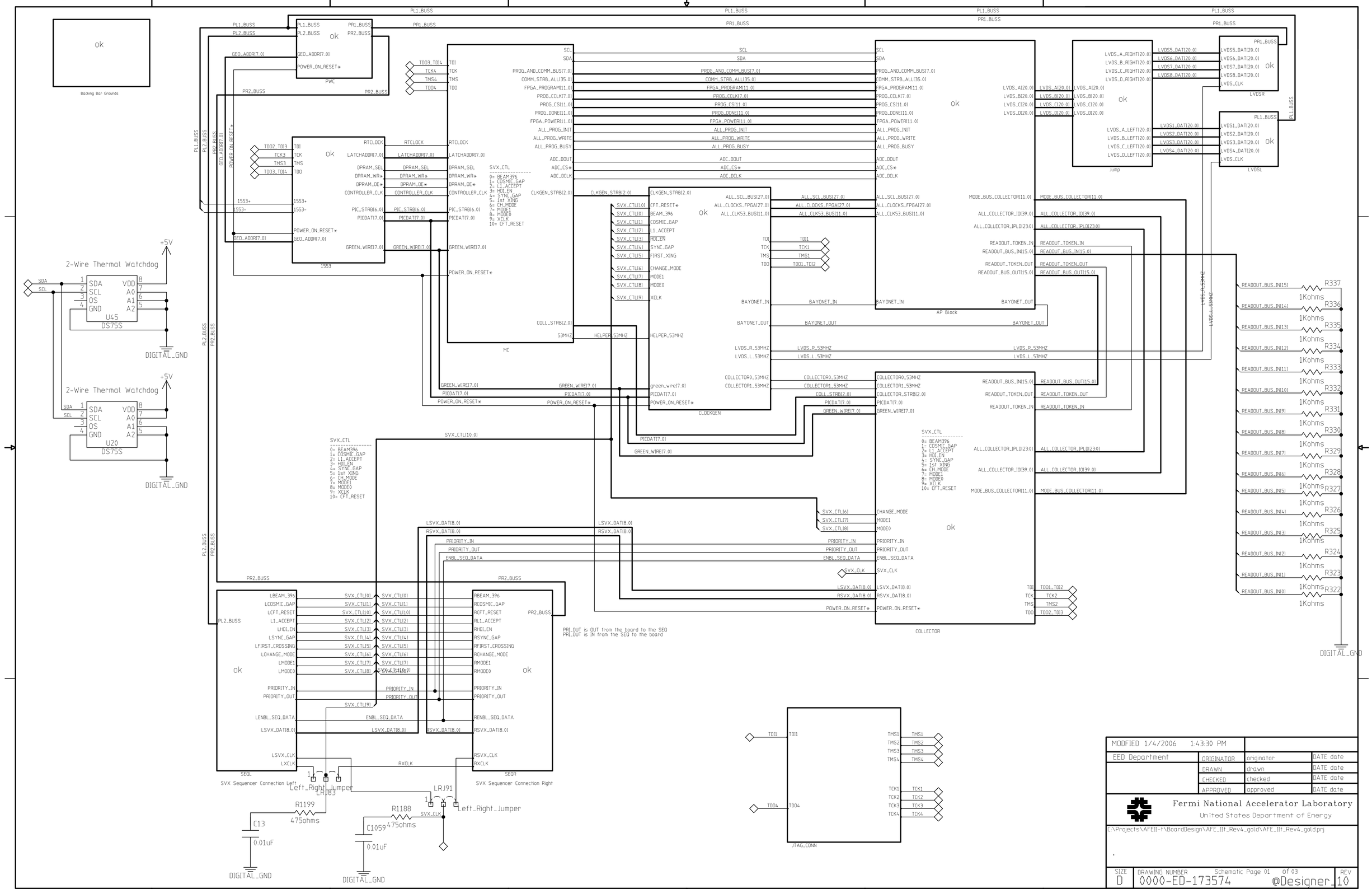

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EED Department	ORIGINATOR	originator	DATE date
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	APPROVED	approved	DATE date

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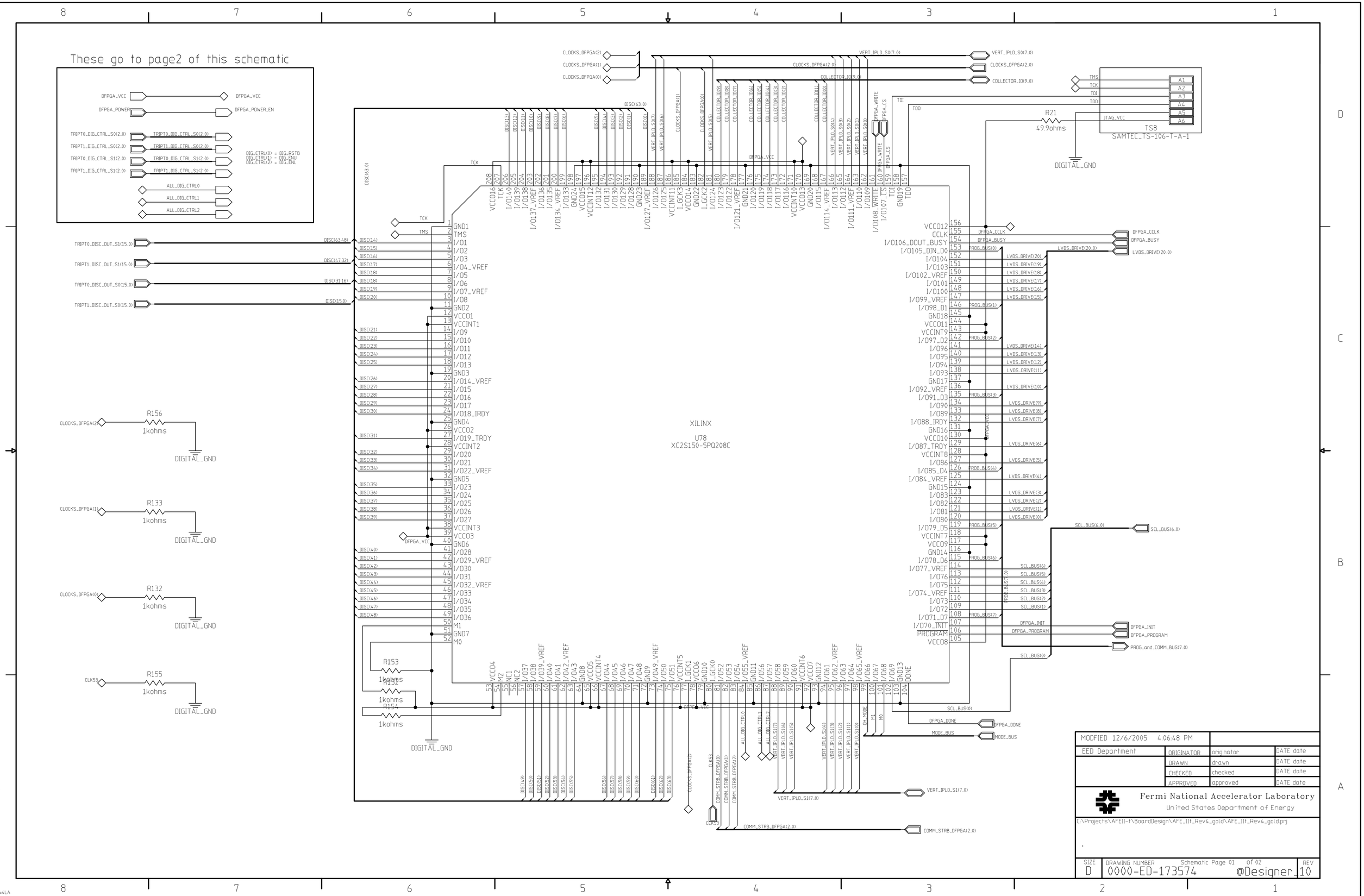
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer_10	

H=8ND; V=4LA



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SIZE	DRAWING NUMBER	Schematic Page 01 of 02	REV
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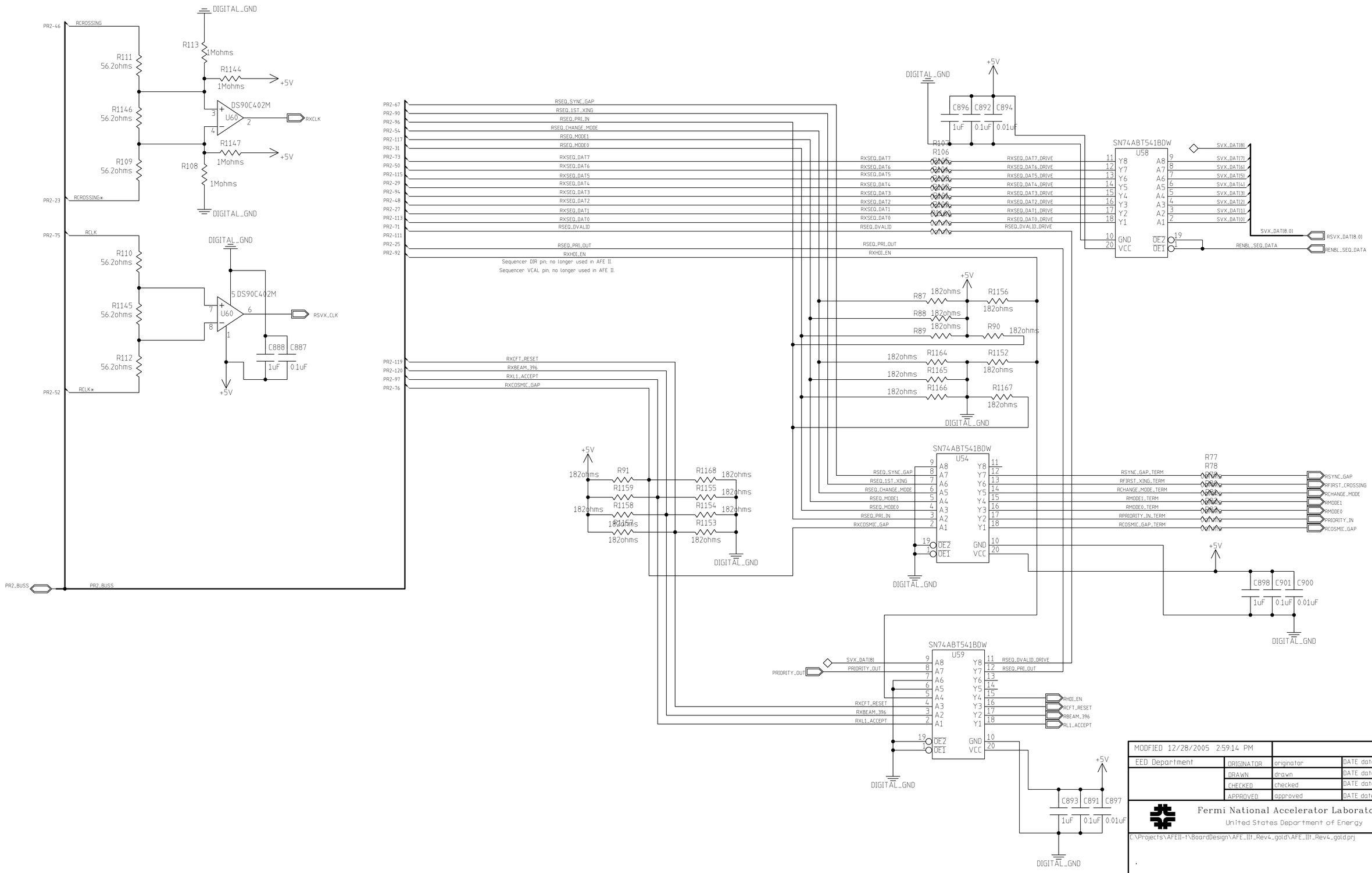
DIGITAL_GND
PR2-46
RCROSSING
R111
56.2ohms
R113
1Mohms
R1144
1Mohms
+5V
R1146
56.2ohms
DS90C402M
U60
RXCLK
R1147
1Mohms
+5V
R109
56.2ohms
R108
1Mohms
PR2-23
RCROSSING*
DIGITAL_GND
PR2-75
RCLK
R110
56.2ohms
DIGITAL_GND
DS90C402M
R1145
56.2ohms
U60
RSVX_CLK
C888
C887
1uF
0.1uF
R112
56.2ohms
+5V
PR2-52
RCLK*
PR2_BUSS
PR2_BUSS
PR2-67
PR2-90
PR2-96
PR2-54
PR2-117
PR2-31
PR2-73
PR2-50
PR2-115
PR2-29
PR2-94
PR2-48
PR2-27
PR2-113
PR2-71
PR2-111
PR2-25
PR2-92
RSEQ_SYNC_GAP
RSEQ_1ST_XING
RSEQ_PRI_IN
RSEQ_CHANGE_MODE
RSEQ_MODE1
RSEQ_MODE0
RXSEQ_DAT7
RXSEQ_DAT6
RXSEQ_DAT5
RXSEQ_DAT4
RXSEQ_DAT3
RXSEQ_DAT2
RXSEQ_DAT1
RXSEQ_DAT0
RSEQ_DVALID
RSEQ_PRI_OUT
RXHDI_EN
Sequencer DIR pin; no longer used in AFE II.
Sequencer VCAL pin; no longer used in AFE II.
PR2-119
PR2-120
PR2-97
PR2-76
RXCFT_RESET
RXBEAM_396
RXL1_ACCEPT
RXCOSMIC_GAP
+5V
182ohms
R91
R1168
182ohms
R1159
R1155
182ohms
182ohms
R1158
R1154
182ohms
R1157
R1153
182ohms
182ohms
DIGITAL_GND
DIGITAL_GND
+5V
C896
C892
C894
1uF
0.1uF
0.01uF
R107
R106
RXSEQ_DAT7
RXSEQ_DAT6
RXSEQ_DAT5
RXSEQ_DAT4
RXSEQ_DAT3
RXSEQ_DAT2
RXSEQ_DAT1
RXSEQ_DAT0
RSEQ_DVALID
RSEQ_PRI_OUT
RXHDI_EN
RXSEQ_DAT7_DRIVE
RXSEQ_DAT6_DRIVE
RXSEQ_DAT5_DRIVE
RXSEQ_DAT4_DRIVE
RXSEQ_DAT3_DRIVE
RXSEQ_DAT2_DRIVE
RXSEQ_DAT1_DRIVE
RXSEQ_DAT0_DRIVE
RSEQ_DVALID_DRIVE
SN74ABT541BDW
U58
SVX_DAT(8)
SVX_DAT(7)
SVX_DAT(6)
SVX_DAT(5)
SVX_DAT(4)
SVX_DAT(3)
SVX_DAT(2)
SVX_DAT(1)
SVX_DAT(0)
SVX_DAT(8.0)
RSVX_DAT(8.0)
RENBL_SEQ_DATA
RENBL_SEQ_DATA
+5V
R87
182ohms
R1156
182ohms
R88
182ohms
R89
182ohms
R90
182ohms
182ohms
R1164
R1152
182ohms
182ohms
R1165
182ohms
R1166
R1167
182ohms
DIGITAL_GND
SN74ABT541BDW
U54
RSEQ_SYNC_GAP
RSEQ_1ST_XING
RSEQ_CHANGE_MODE
RSEQ_MODE1
RSEQ_MODE0
RSEQ_PRI_IN
RXCOSMIC_GAP
RSYNC_GAP_TERM
RFIRST_XING_TERM
RCHANGE_MODE_TERM
RMODE1_TERM
RMODE0_TERM
RPRIORITY_IN_TERM
RCOSMIC_GAP_TERM
R77
R78
RSYNC_GAP
RFIRST_CROSSING
RCHANGE_MODE
RMODE1
RMODE0
PRIORITY_IN
RCOSMIC_GAP
DIGITAL_GND
+5V
C898
C901
C900
1uF
0.1uF
0.01uF
DIGITAL_GND
SN74ABT541BDW
U59
SVX_DAT(8)
PRIORITY_OUT
PRIORITY_OUT
RSEQ_DVALID_DRIVE
RSEQ_PRI_OUT
RXCFT_RESET
RXBEAM_396
RXL1_ACCEPT
RHDI_EN
RCFT_RESET
RBEAM_396
RL1_ACCEPT
DIGITAL_GND
+5V
C893
C891
C897
1uF
0.1uF
0.01uF
DIGITAL_GND
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DATE date
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DATE date
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DRAWING NUMBER
0000-ED-173574
Schematic Page 01 of 01
@Designer_10
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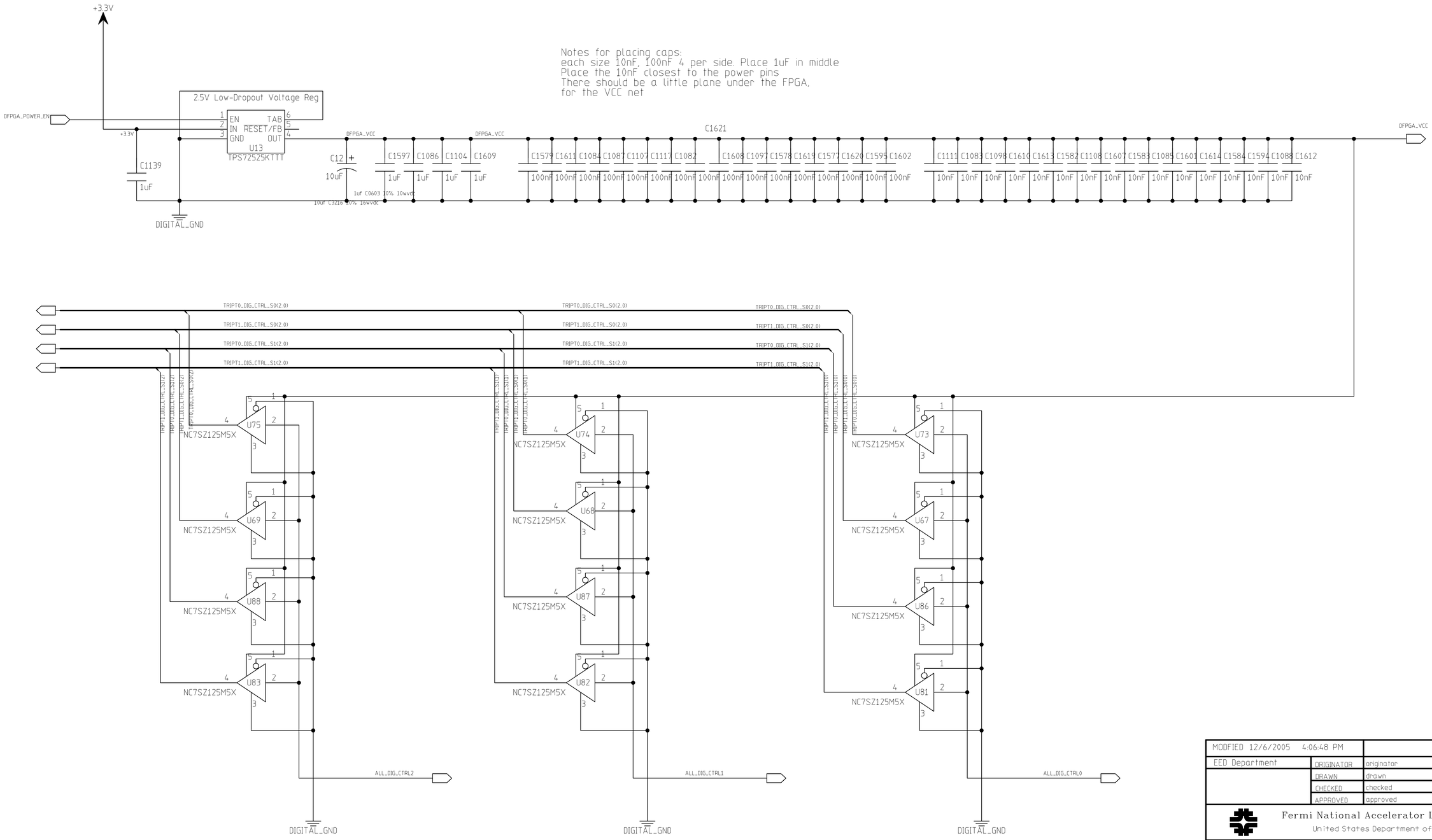

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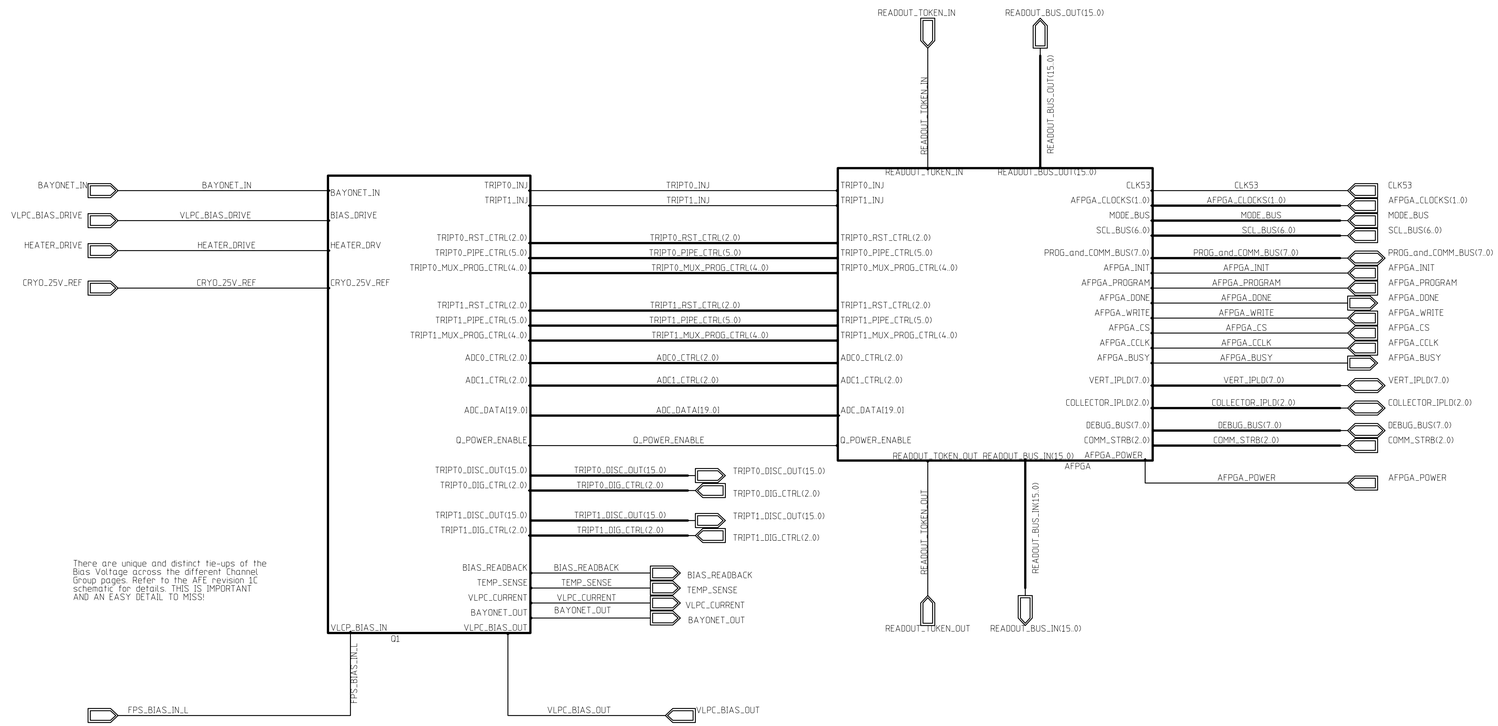
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer	10

H:8ND, V:4LA



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SIZE	DRAWING NUMBER		REV
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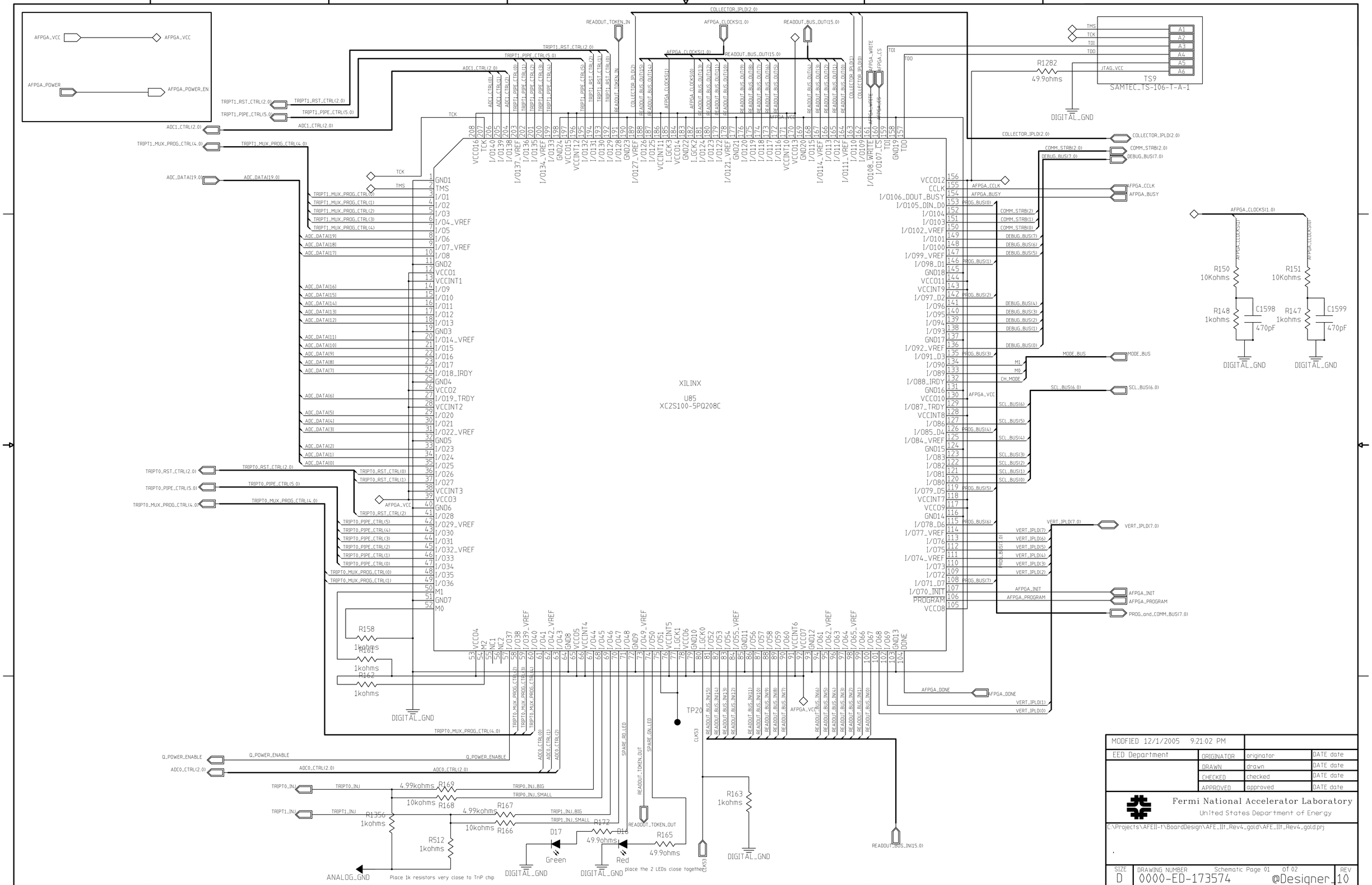

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SIZE	DRAWING NUMBER		REV
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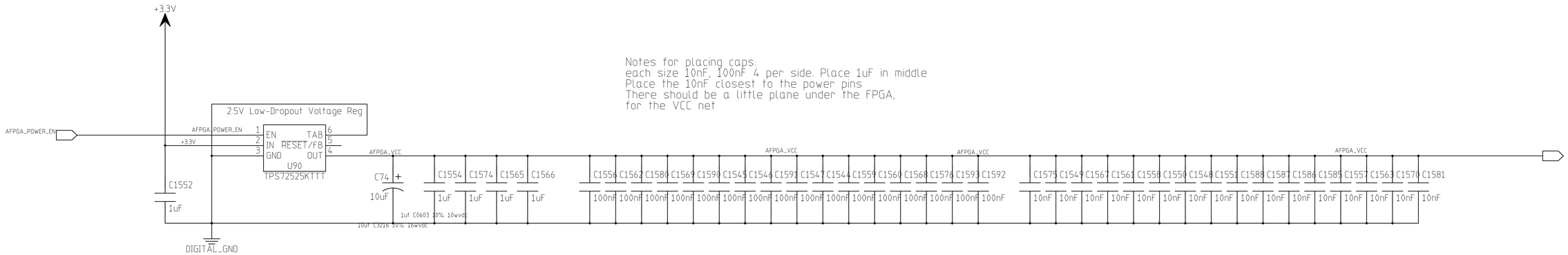

Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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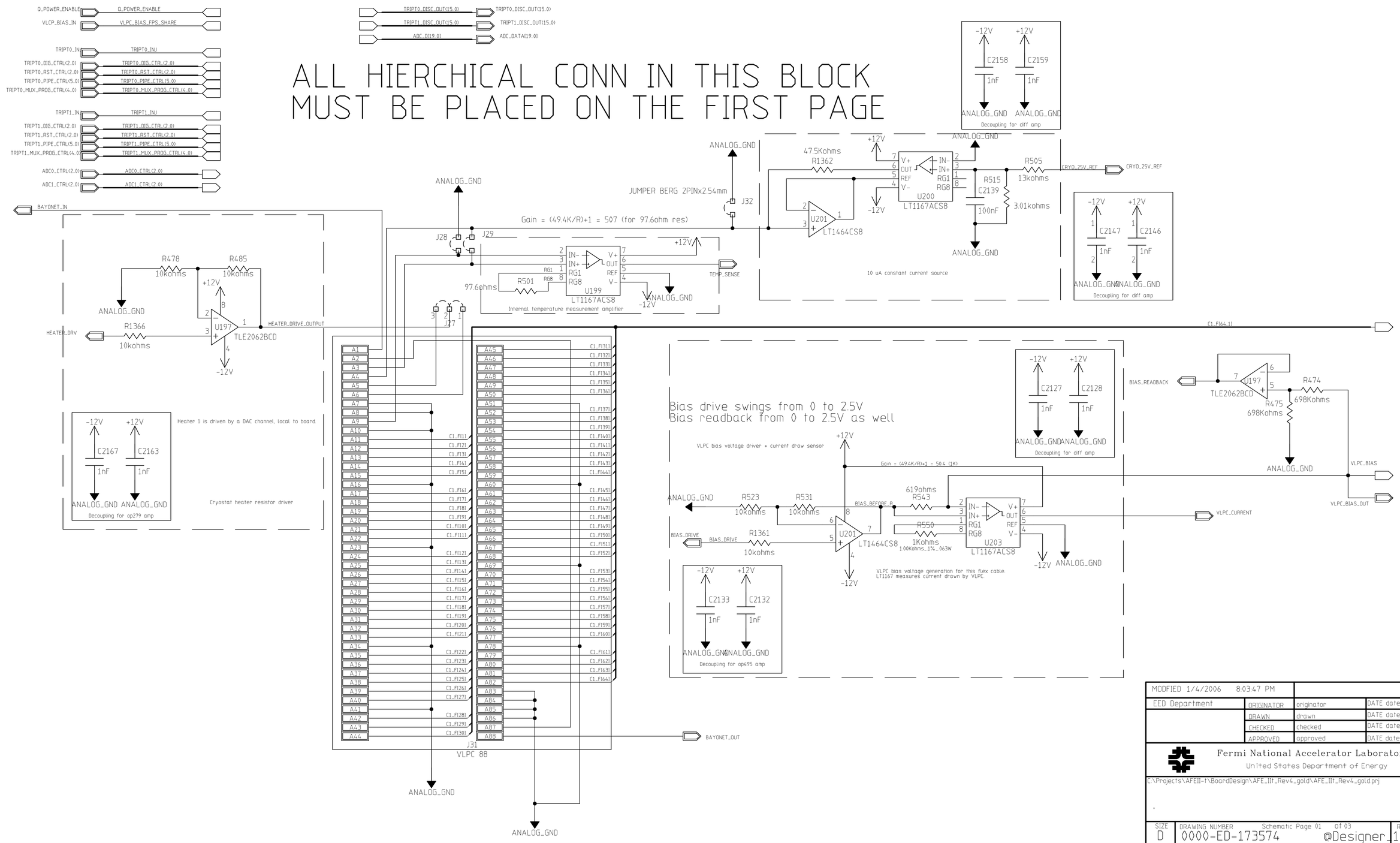
ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
BAYONET_IN
ANALOG_GND
R478
10kohms
R485
10kohms
+12V
U197
TLE2062BCD
HEATER_DRIVE_OUTPUT
HEATER_DRV
R1366
10kohms
-12V
C2167
C2163
1nF
ANALOG_GND ANALOG_GND
Decoupling for op279 amp
Heater 1 is driven by a DAC channel, local to board.
Cryostat heater resistor driver
J28
J29
J27
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
97.6ohms
R501
U199
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
JUMPER BERG 2PINx2.54mm
J32
47.5Kohms
R1362
U201
LT1464CS8
U200
LT1167ACS8
R505
13kohms
CRYO_25V_REF
R515
3.01kohms
C2139
100nF
10 uA constant current source
C2158
C2159
Decoupling for diff amp
C2147
C2146
Decoupling for diff amp
C1_FI64.1
J31
VLPC 88
BAYONET_OUT
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R523
10kohms
R531
10kohms
BIAS_BEFORE_R
619ohms
R543
R550
1Kohms
1.00Kohms_1%_.063W
BIAS_DRIVE
R1361
10kohms
U203
LT1167ACS8
VLPC_CURRENT
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
C2133
C2132
Decoupling for op495 amp
C2127
C2128
Decoupling for diff amp
BIAS_READBACK
R474
698Kohms
R475
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
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ORIGINATOR originator DATE date
DRAWN drawn DATE date
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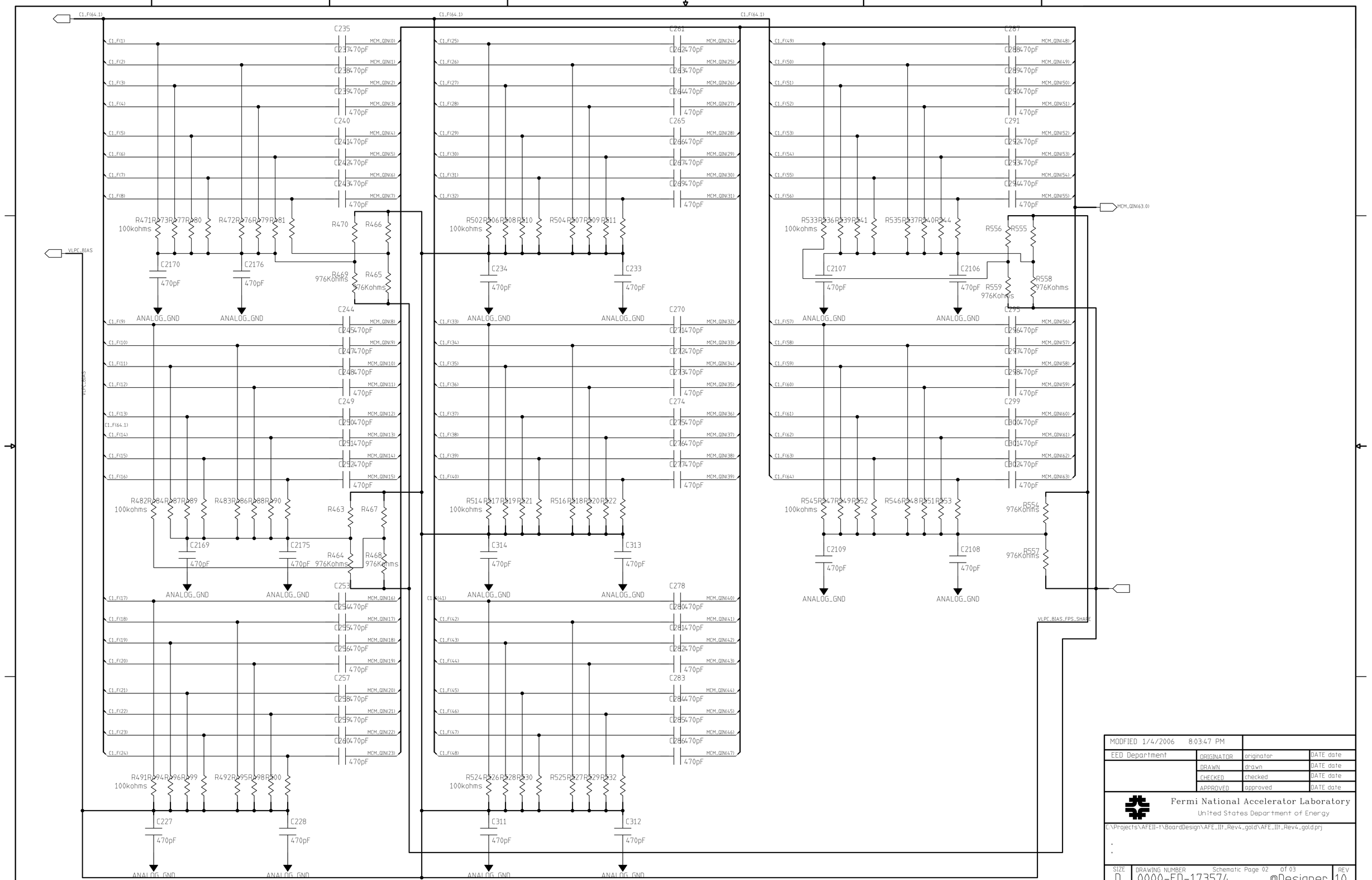
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV
H=8ND, V=4LA


C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
R471 R473 R477 R480
R472 R476 R479 R481
100kohms
R470 R466
R469 R465
976Kohms
C2170 C2176
470pF
R482 R484 R487 R489
R483 R486 R488 R490
R463 R467
R464 R468
C2169 C2175
R491 R494 R496 R499
R492 R495 R498 R500
C227 C228
R502 R506 R508 R510
R504 R507 R509 R511
C234 C233
R514 R517 R519 R521
R516 R518 R520 R522
C314 C313
R524 R526 R528 R530
R525 R527 R529 R532
C311 C312
R533 R536 R539 R541
R535 R537 R540 R544
C2107 C2106
R556 R555
R558
R559
R545 R547 R549 R552
R546 R548 R551 R553
C2109 C2108
R554
R557
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@Designer_10
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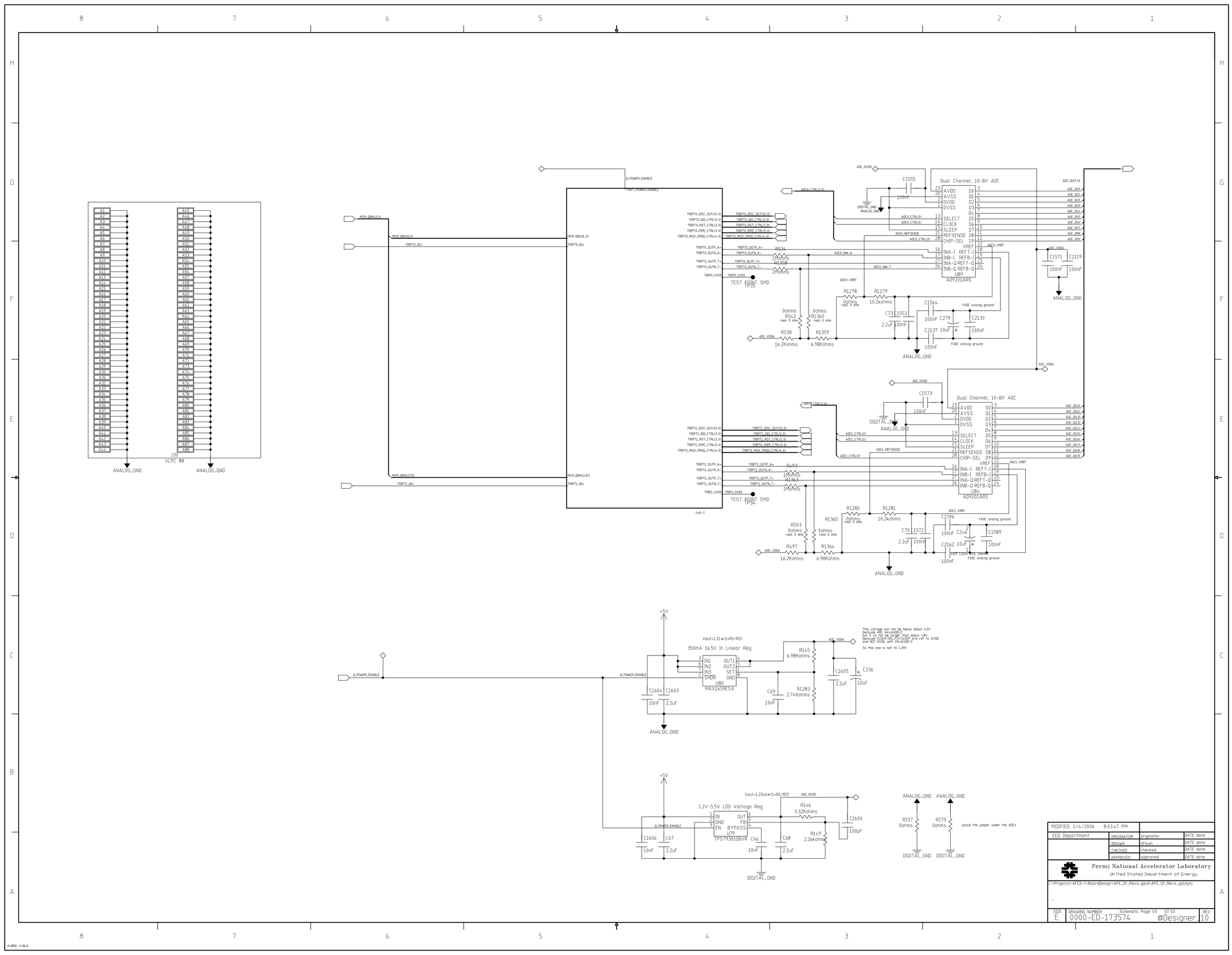

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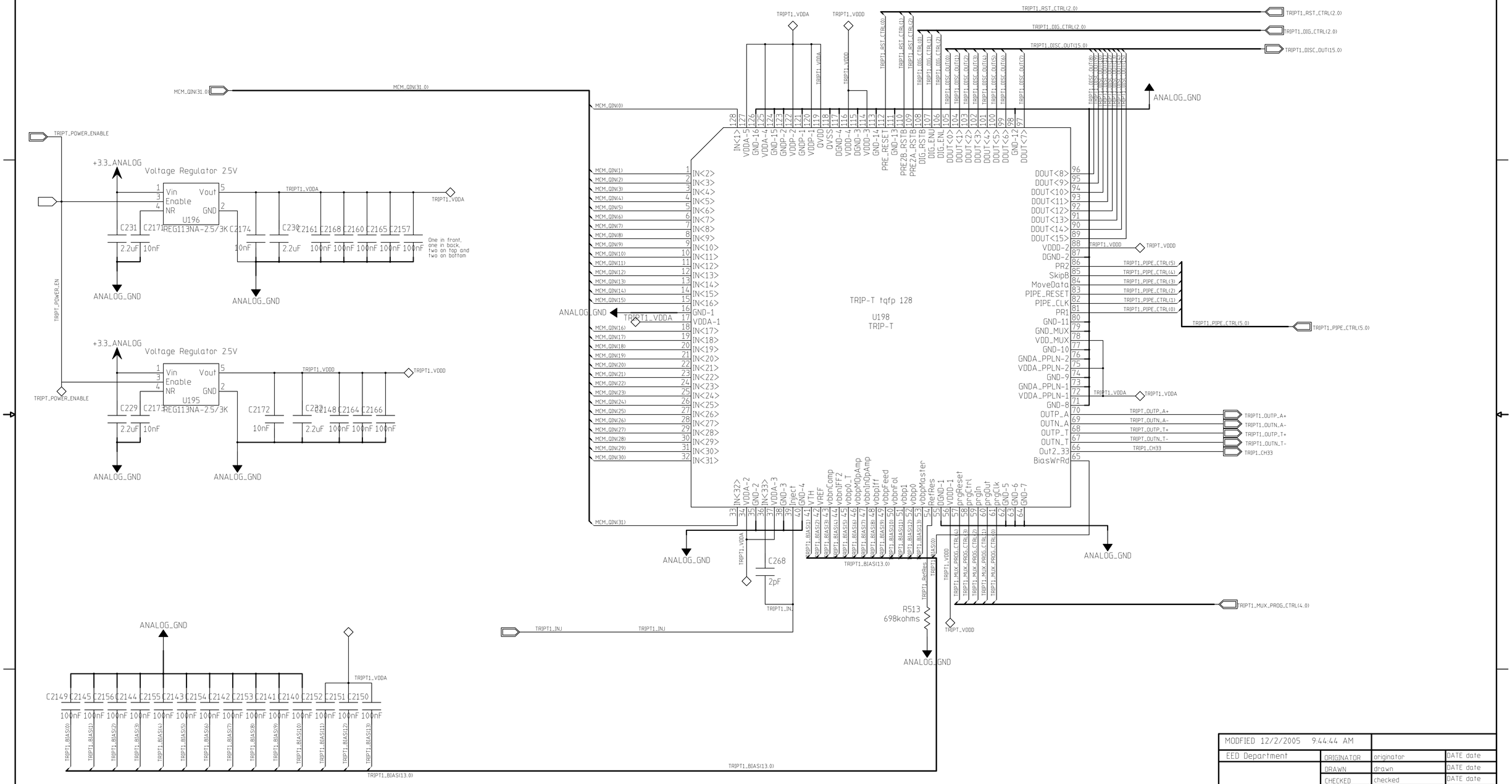

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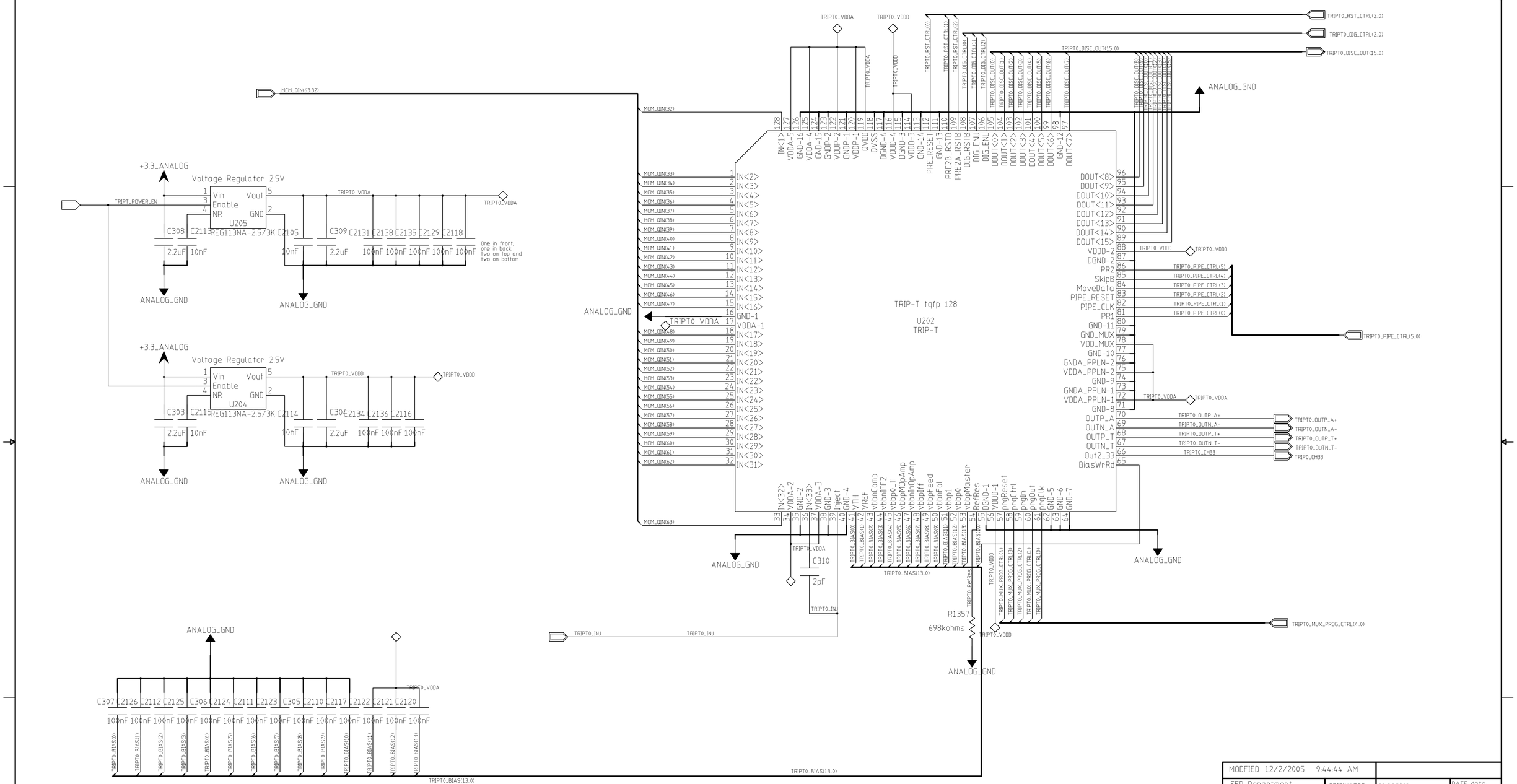
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H:8ND, V:4LA



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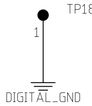
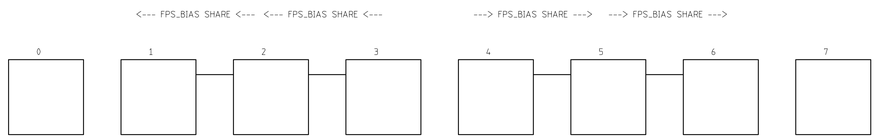
H=8ND, V=4LA

Comments go here





Left to right:
CLOCKGEN
COLLECTOR
1553
HELPER

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SIZE	DRAWING NUMBER		REV
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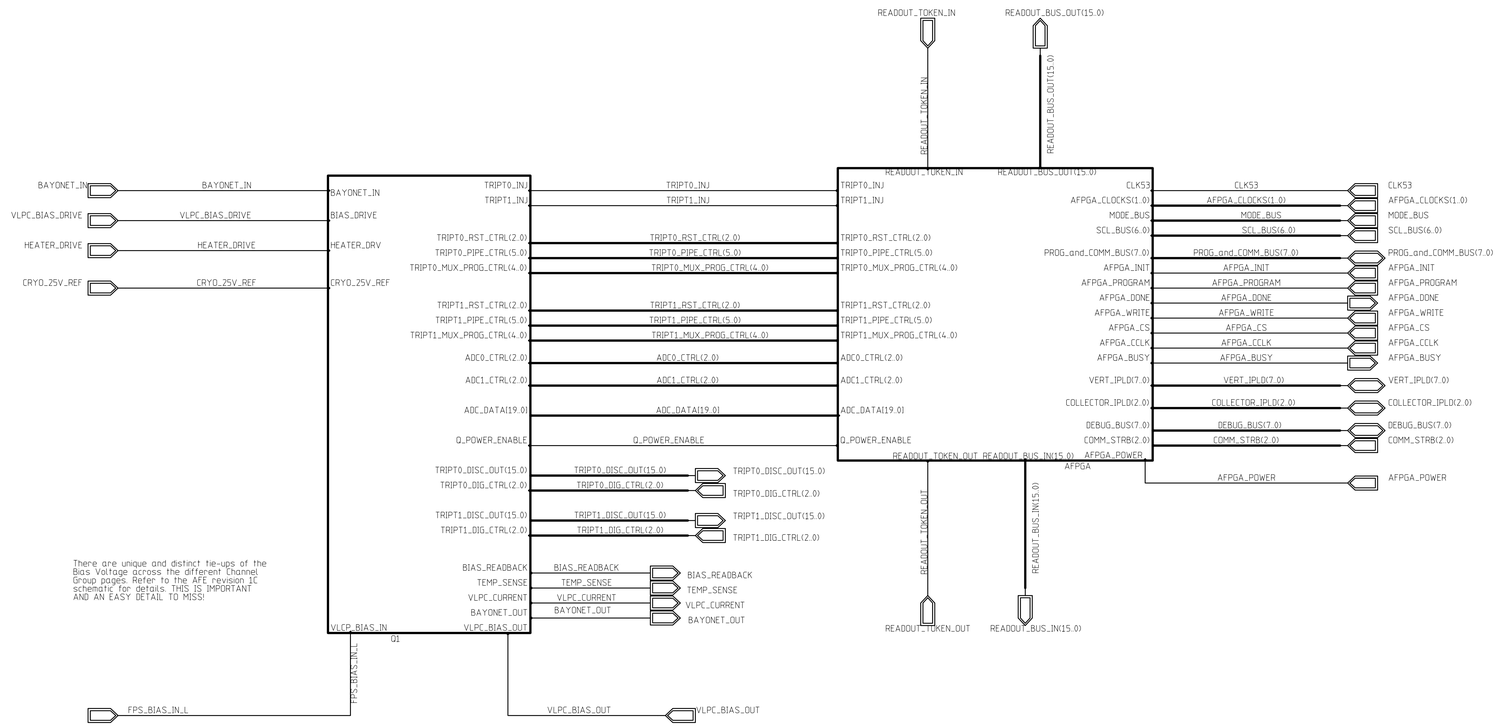

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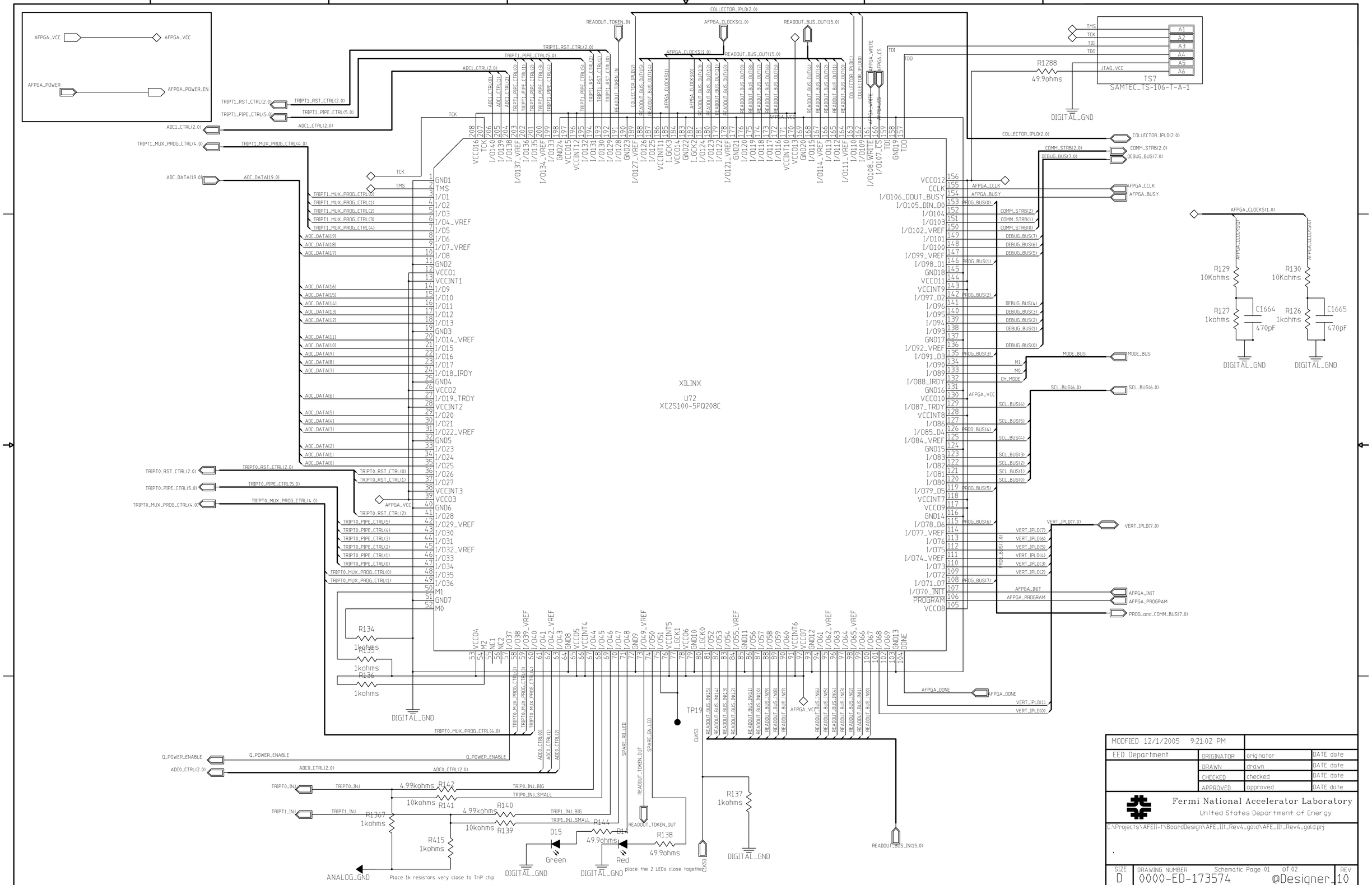
XILINX
U72
XC2S100-5PQ208C
TS7
SAMTEC_TS-106-T-A-1
R1288
49.9ohms
R129
10Kohms
R130
10Kohms
R127
1kohms
R126
1kohms
C1664
470pF
C1665
470pF
R134
1kohms
R135
1kohms
R136
1kohms
R142
4.99kohms
R141
10kohms
R140
4.99kohms
R139
10kohms
R1367
1kohms
R415
1kohms
R144
49.9ohms
R138
49.9ohms
R137
1kohms
D15
Green
D14
Red
TP19
DIGITAL_GND
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
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REV 10
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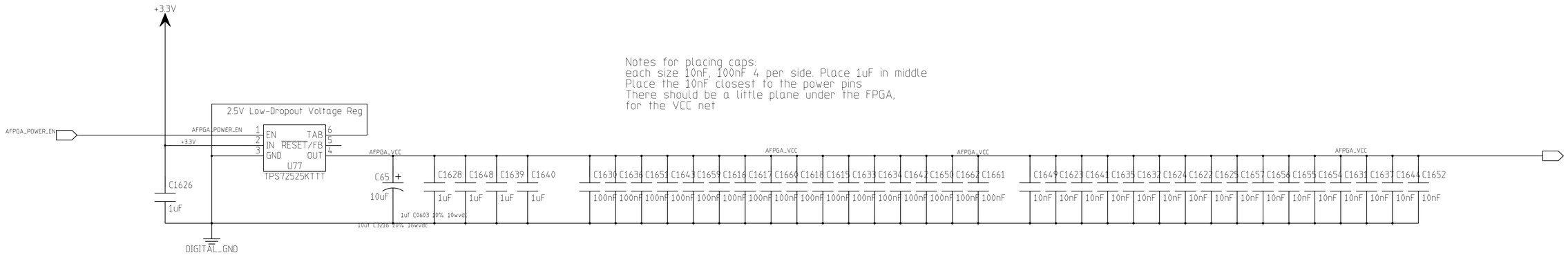

Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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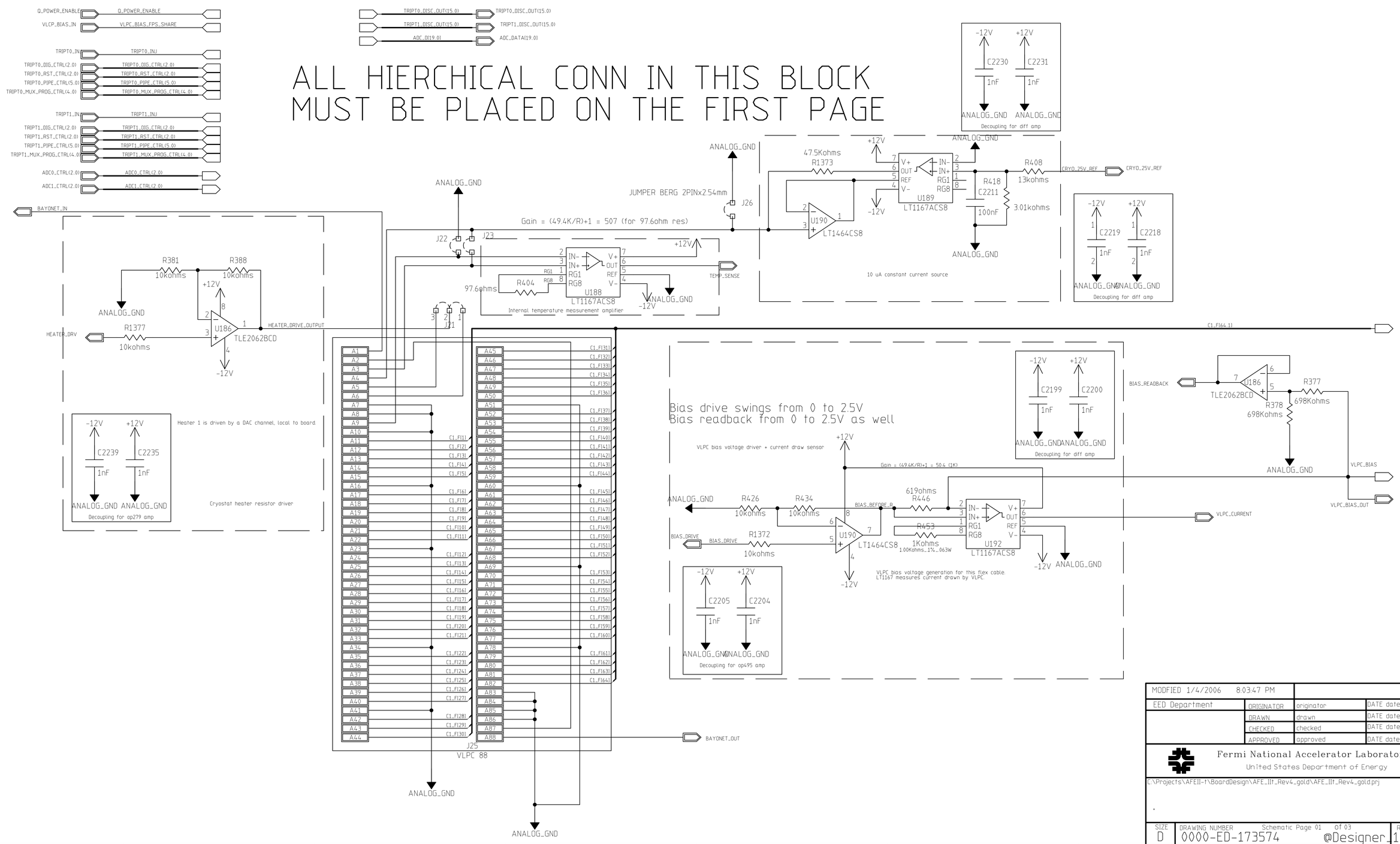
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA



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	APPROVED	approved	DATE date

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SIZE	DRAWING NUMBER		REV
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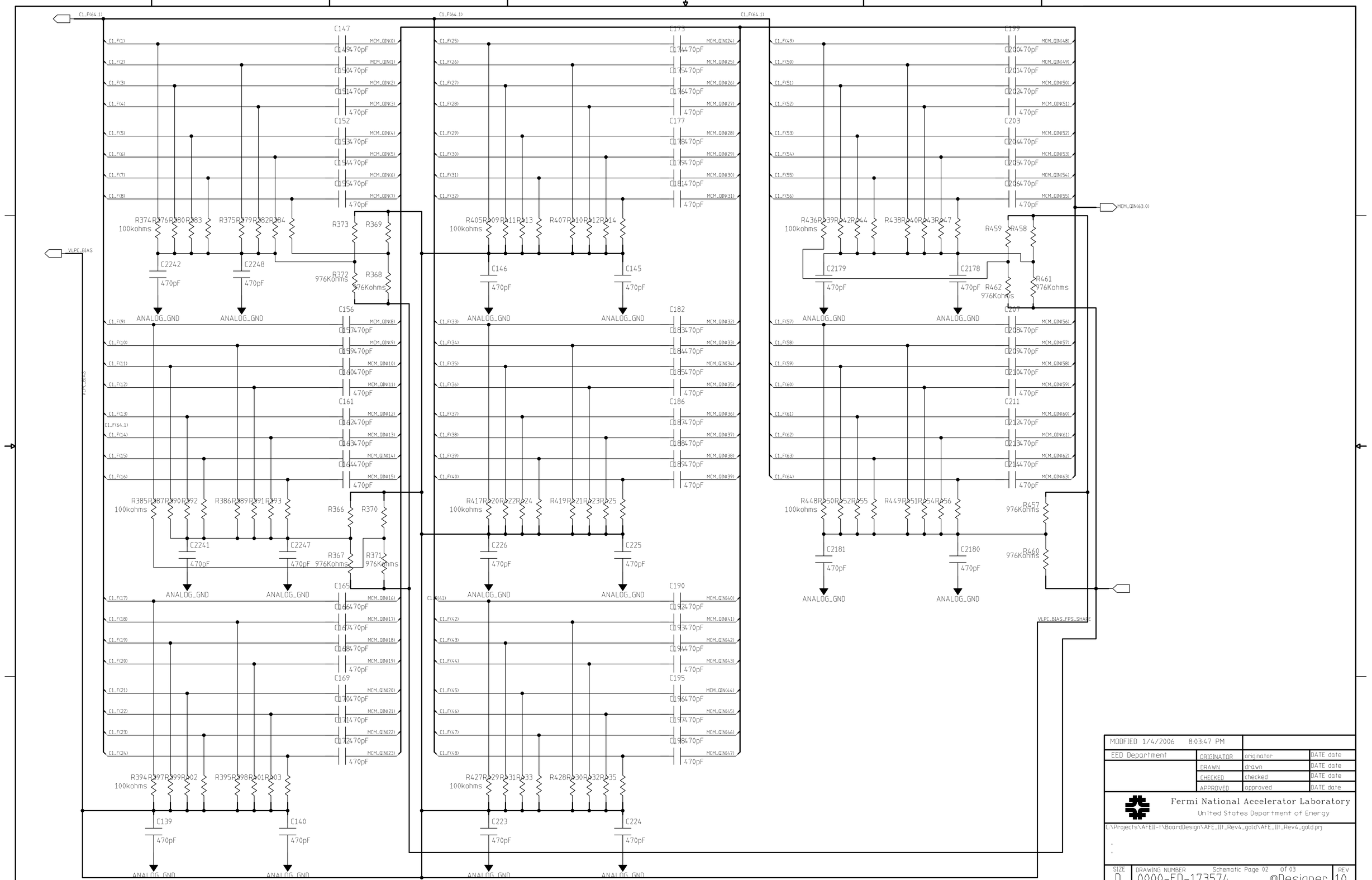

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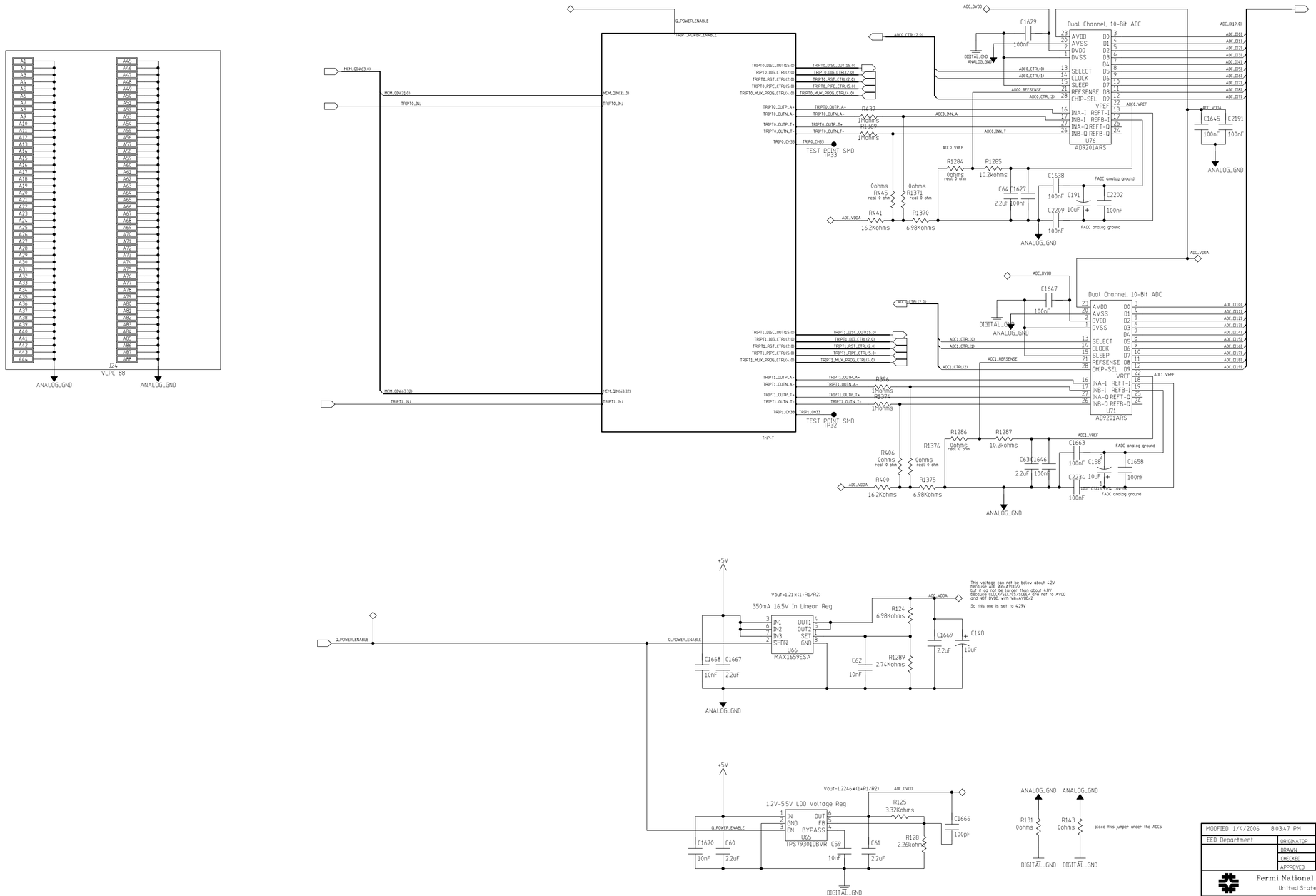

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SIZE	DRAWING NUMBER	REV
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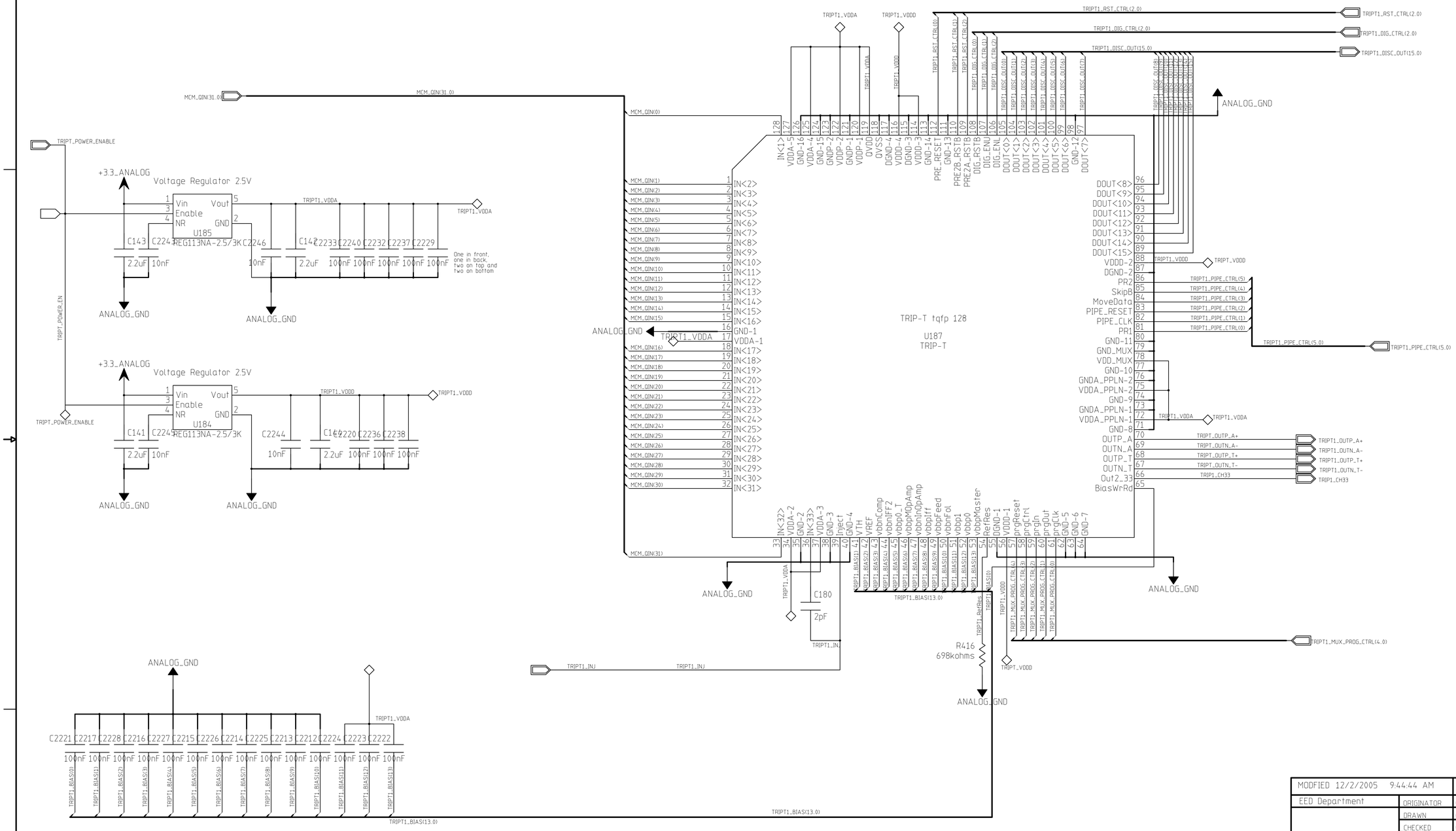
H:\BND V:\BLA



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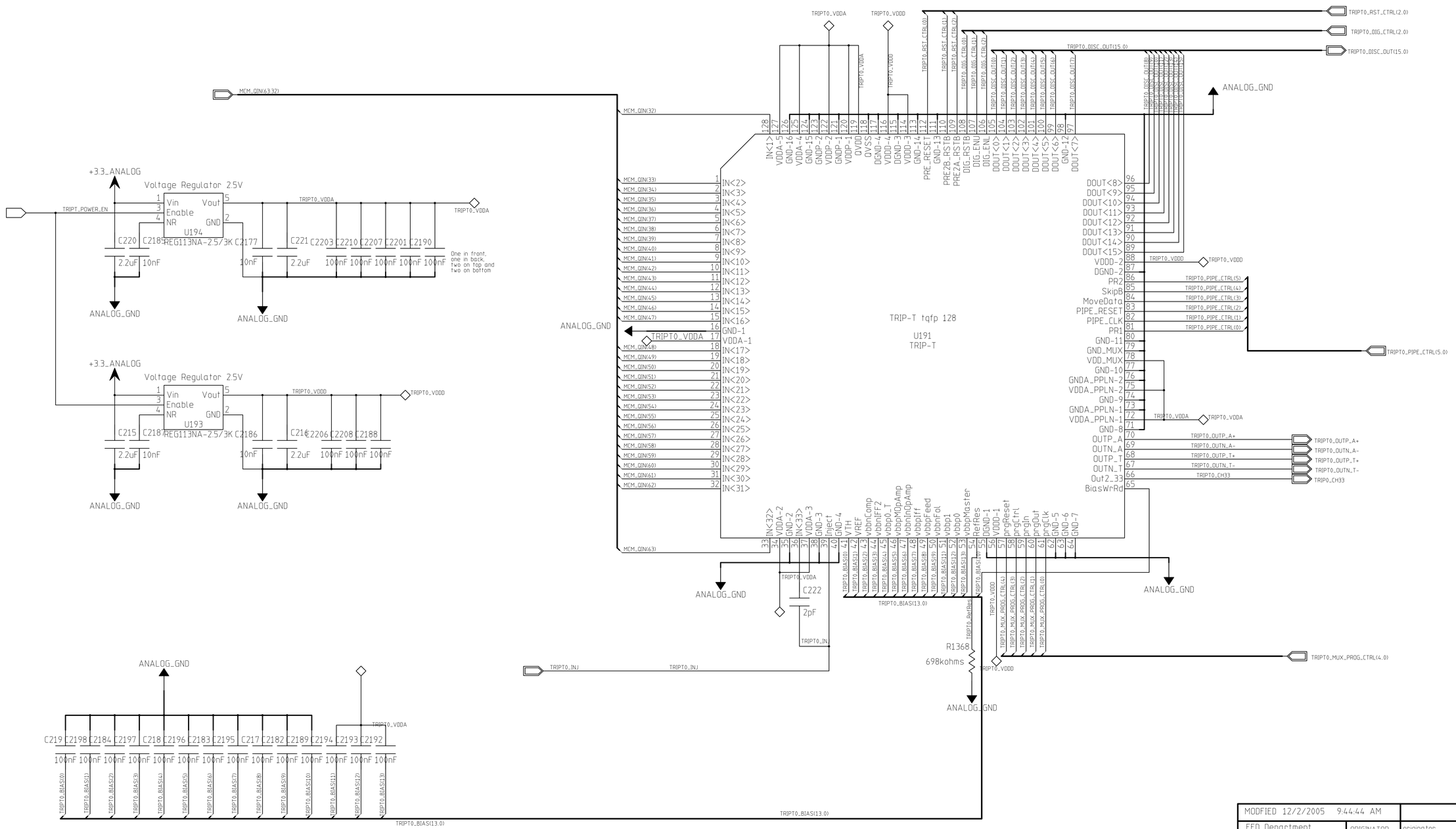

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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

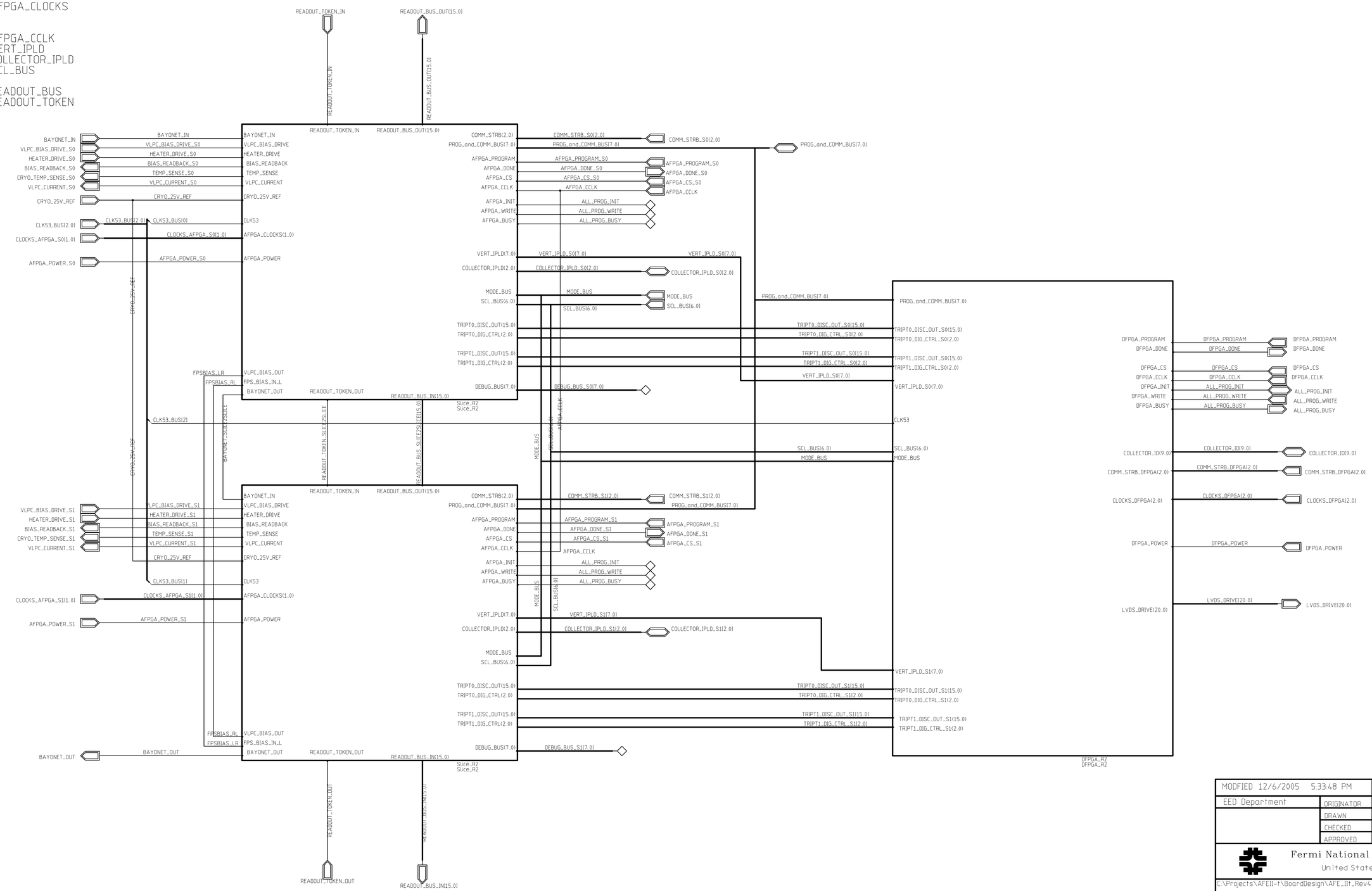
H=8ND, V=4LA

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



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SIZE	DRAWING NUMBER		REV
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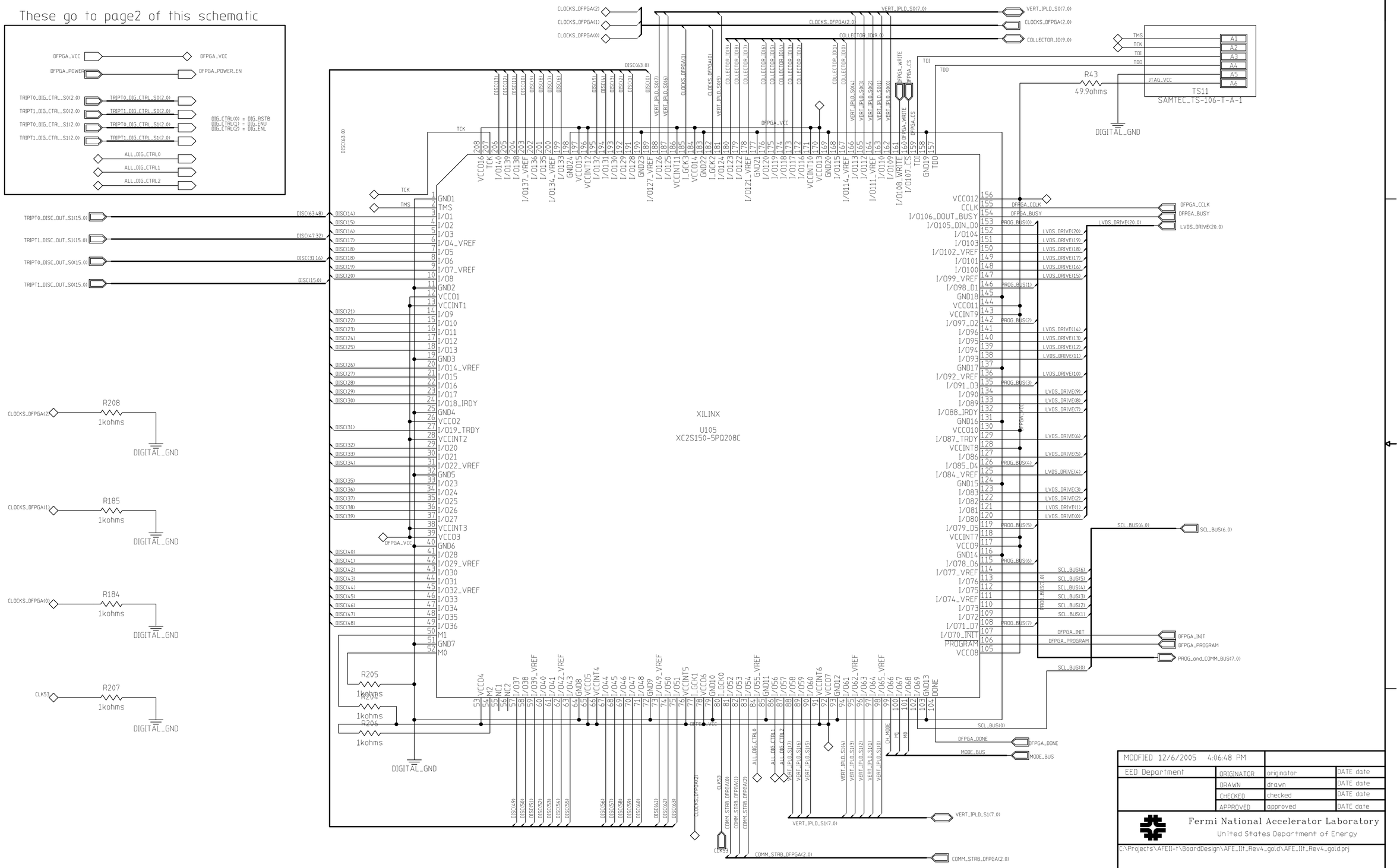
H=8ND, V=4LA



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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer	10

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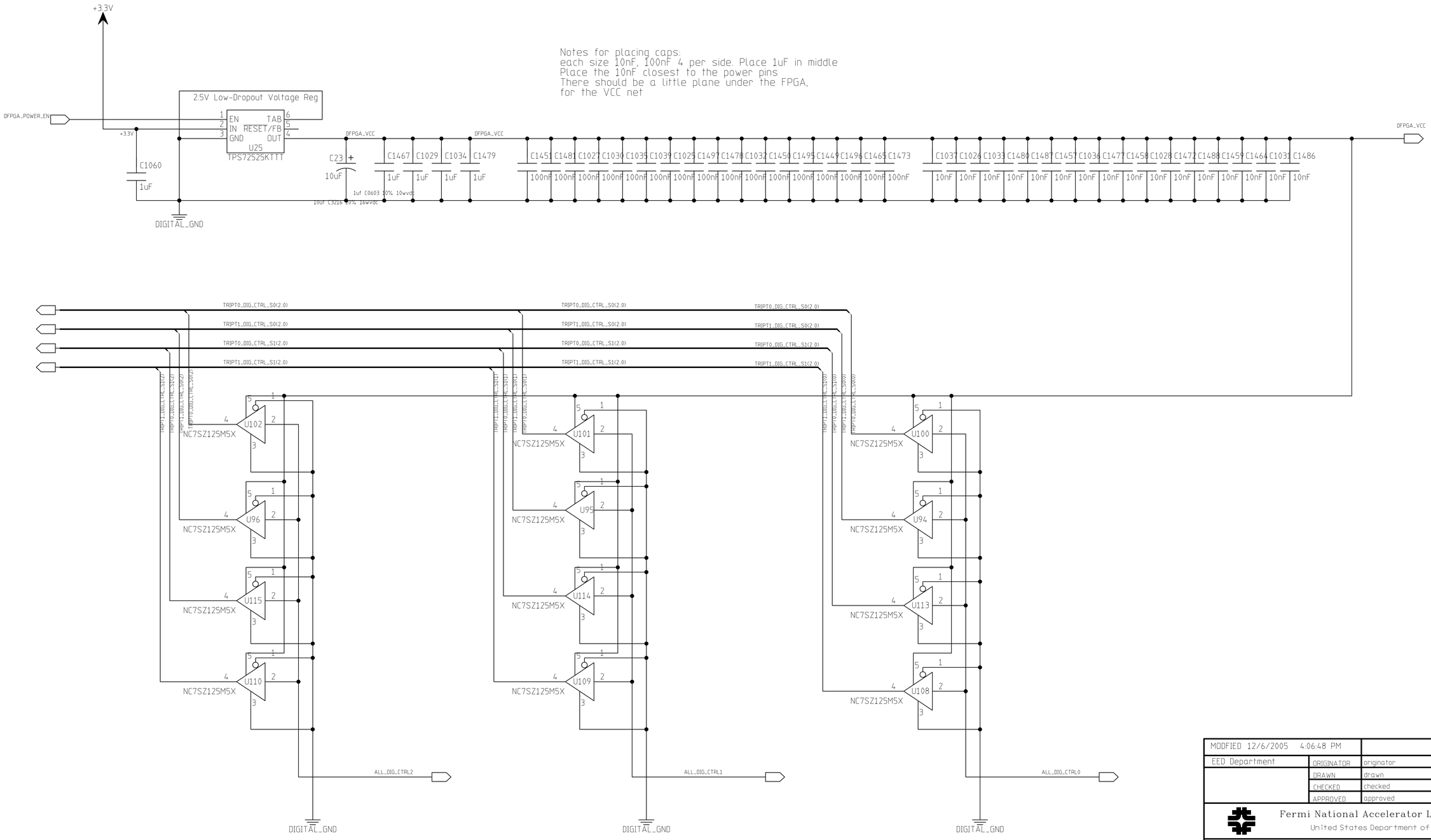

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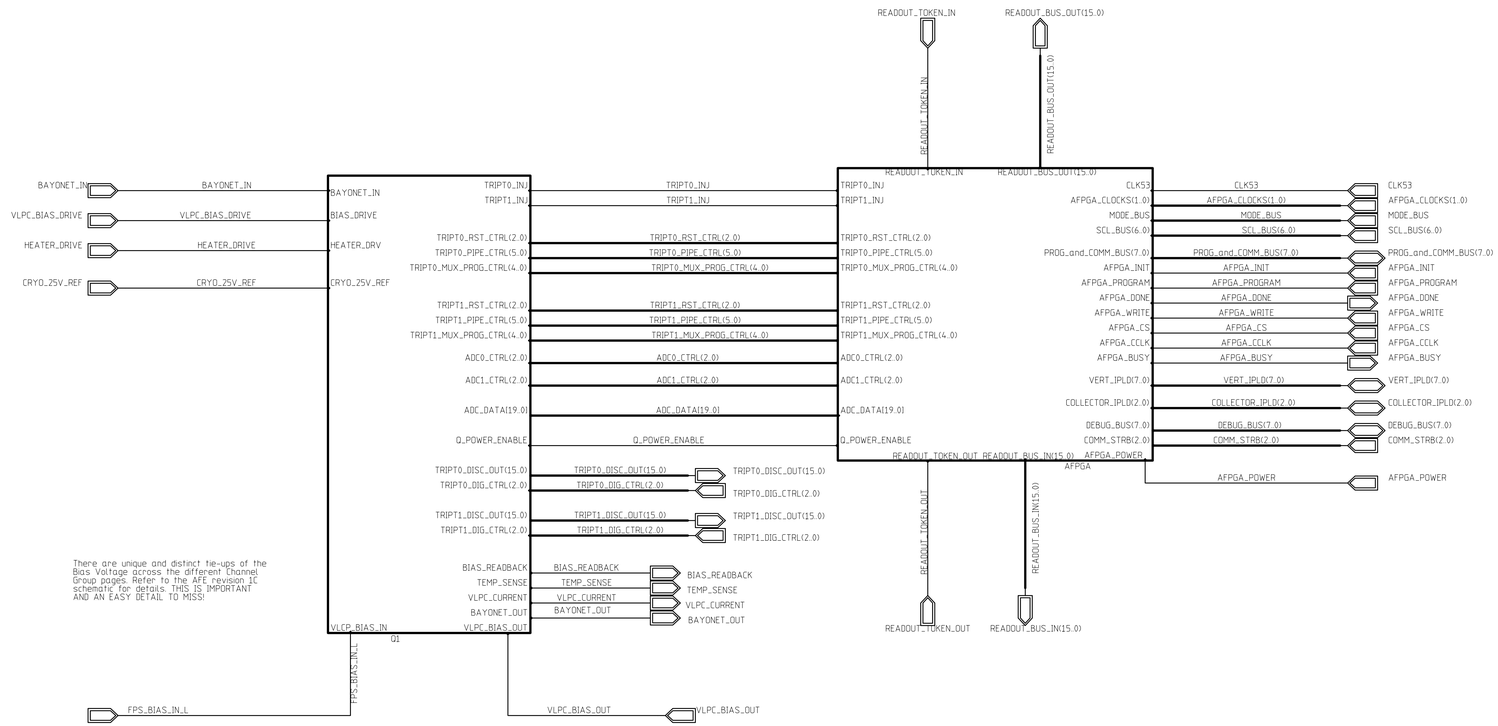

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SIZE	DRAWING NUMBER		REV
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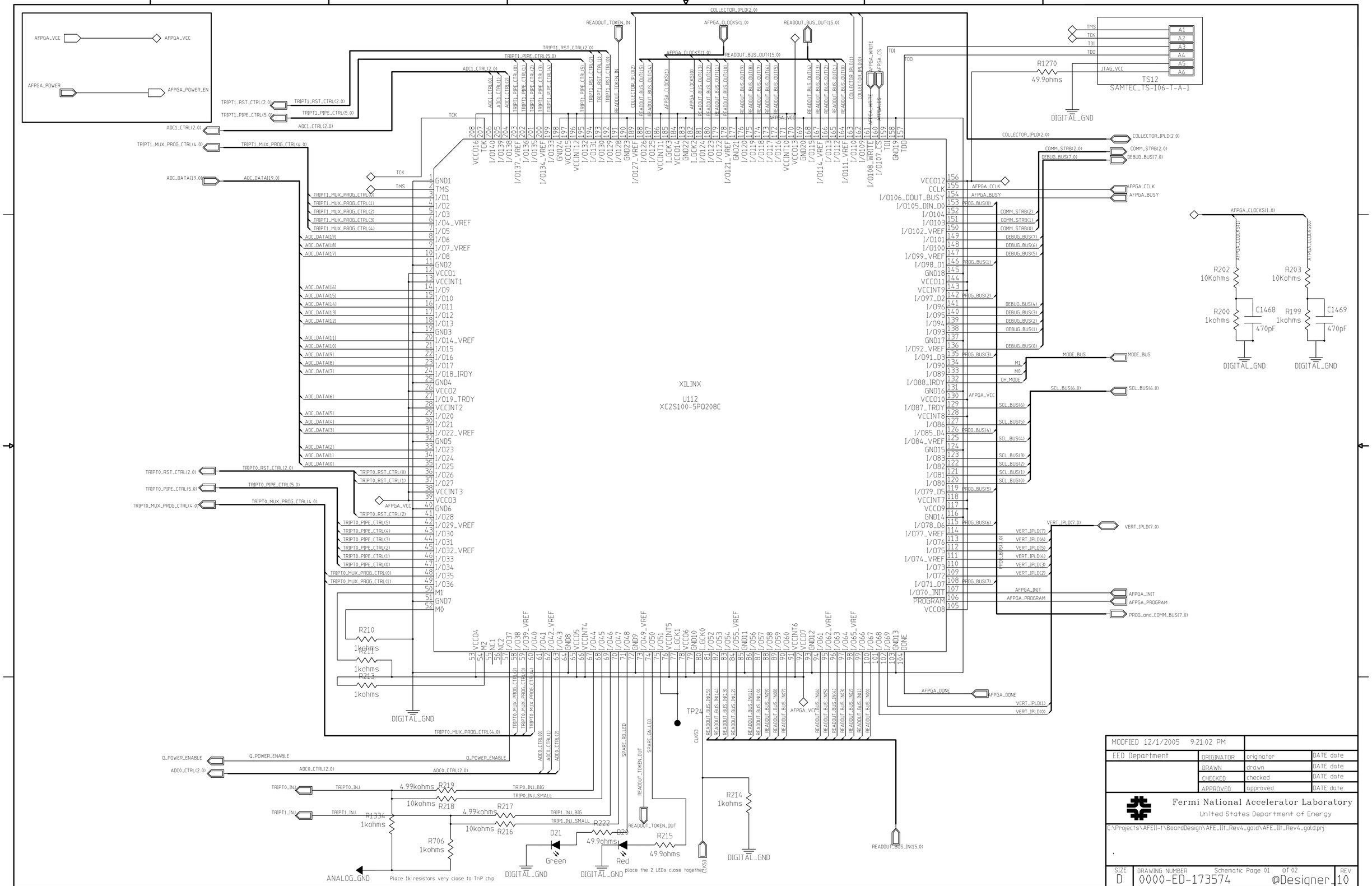
H:8ND, V:4LA


XILINX
U112
XC2S100-5PQ208C
SAMTEC_TS-106-T-A-1
TS12
R1270
49.9ohms
DIGITAL_GND
R202
10Kohms
R203
10Kohms
R200
1kohms
R199
1kohms
C1468
470pF
C1469
470pF
R210
1kohms
R211
1kohms
R213
1kohms
R219
4.99kohms
R218
10kohms
R217
4.99kohms
R216
10kohms
R1334
1kohms
R706
1kohms
R222
49.9ohms
R215
49.9ohms
R214
1kohms
D21
Green
D20
Red
TP24
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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C:\Projects\AFEII-T\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj
SIZE D
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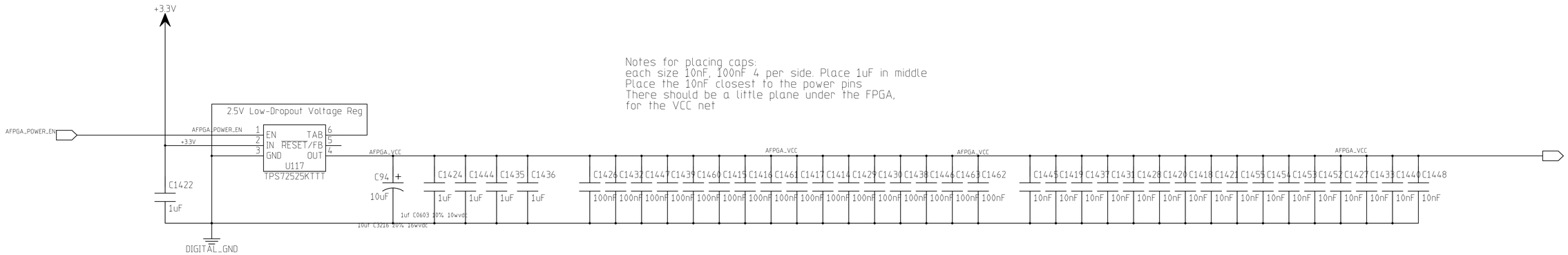
Schematic Page 01 of 02
@Designer
REV 10
H=8ND, V=4LA



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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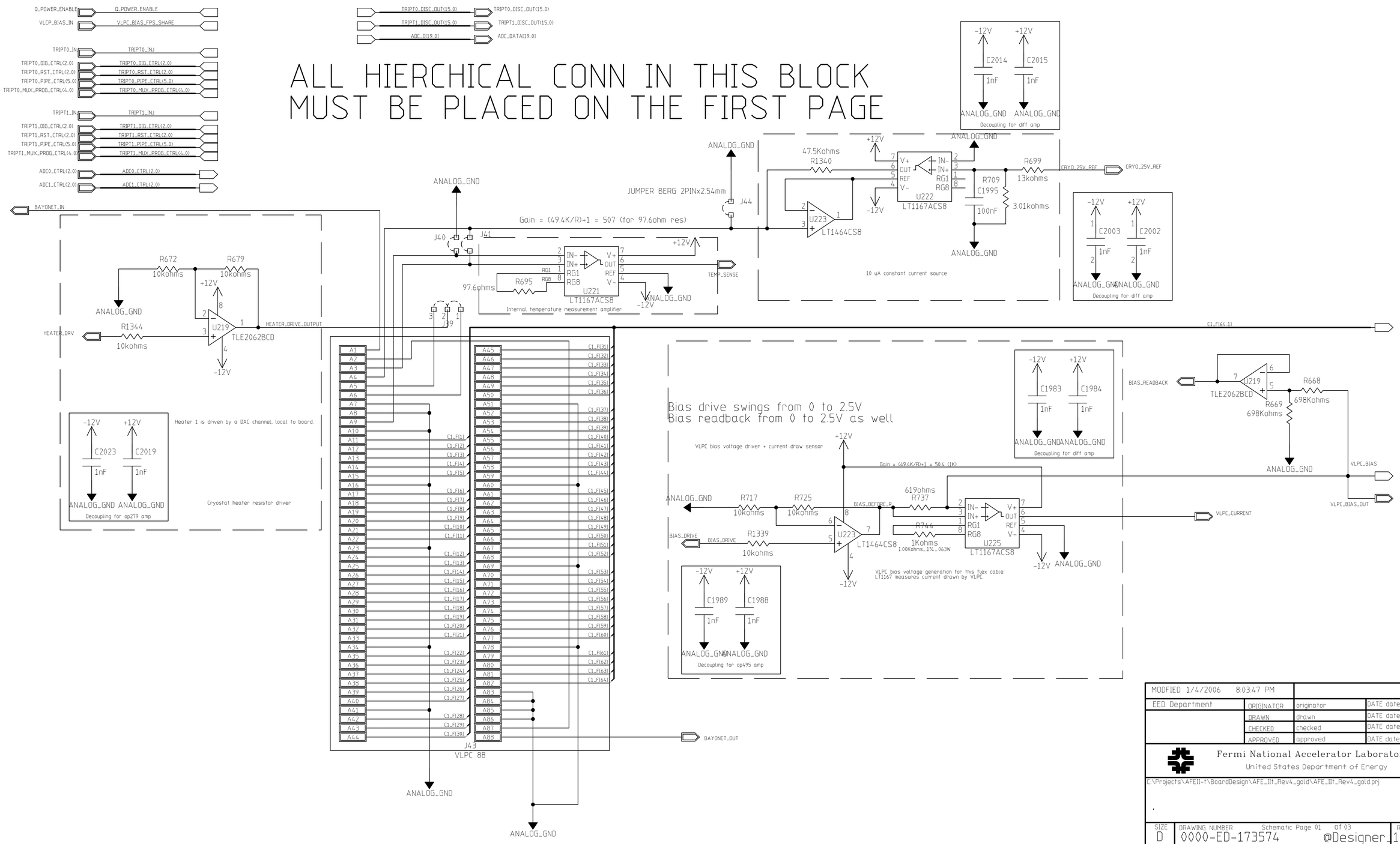
ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
BAYONET_IN
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
ANALOG_GND
JUMPER BERG 2PINx2.54mm
J44
J40
J41
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
R672
10kohms
R679
10kohms
+12V
U219
TLE2062BCD
HEATER_DRIVE_OUTPUT
HEATER_DRV
R1344
10kohms
-12V
C2023
C2019
1nF
Heater 1 is driven by a DAC channel, local to board.
Cryostat heater resistor driver
Decoupling for op279 amp
R695
97.6ohms
U221
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
J39
J43
VLPC 88
BAYONET_OUT
C1_FI64.1
R1340
47.5Kohms
U223
LT1464CS8
U222
LT1167ACS8
R699
13kohms
CRYO_25V_REF
R709
3.01kohms
C1995
100nF
10 uA constant current source
C2014
C2015
C2003
C2002
Decoupling for diff amp
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R717
10kohms
R725
10kohms
BIAS_BEFORE_R
619ohms
R737
R744
1Kohms
1.00Kohms_1%_.063W
R1339
10kohms
BIAS_DRIVE
U225
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
VLPC_CURRENT
C1989
C1988
Decoupling for op495 amp
C1983
C1984
BIAS_READBACK
R668
698Kohms
R669
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
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drawn
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approved
DATE date
Fermi National Accelerator Laboratory
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SIZE D
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Schematic Page 01 of 03
@Designer_10
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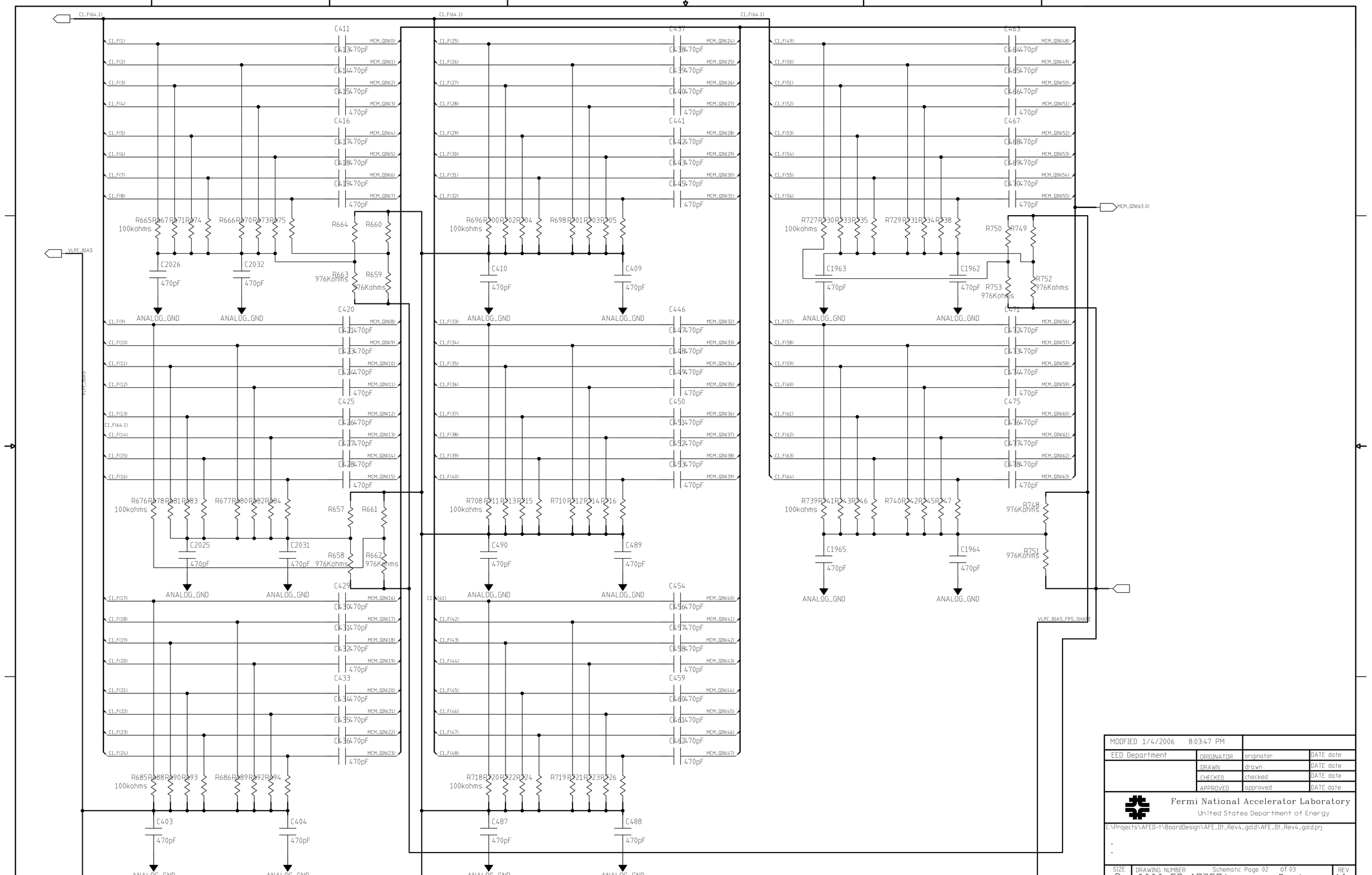
C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
R665 R667 R671 R674
R666 R670 R673 R675
100kohms
R664 R660
R663 R659
976Kohms
C2026 C2032
470pF
R696 R700 R702 R704
R698 R701 R703 R705
C410 C409
R727 R730 R733 R735
R729 R731 R734 R738
R750 R749
R752
R753
C1963 C1962
R676 R678 R681 R683
R677 R680 R682 R684
R657 R661
R658 R662
C2025 C2031
R708 R711 R713 R715
R710 R712 R714 R716
C490 C489
R739 R741 R743 R746
R740 R742 R745 R747
R748
R751
C1965 C1964
R685 R688 R690 R693
R686 R689 R692 R694
C403 C404
R718 R720 R722 R724
R719 R721 R723 R726
C487 C488
C411 C437 C463
C412 C438 C464
C413 C439 C465
C414 C440 C466
C416 C441 C467
C417 C442 C468
C418 C443 C469
C419 C445 C470
C420 C446 C471
C421 C447 C472
C423 C448 C473
C424 C449 C474
C425 C450 C475
C426 C451 C476
C427 C452 C477
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C429 C454
C430 C456
C431 C457
C432 C458
C433 C459
C434 C460
C435 C461
C436 C462
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SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
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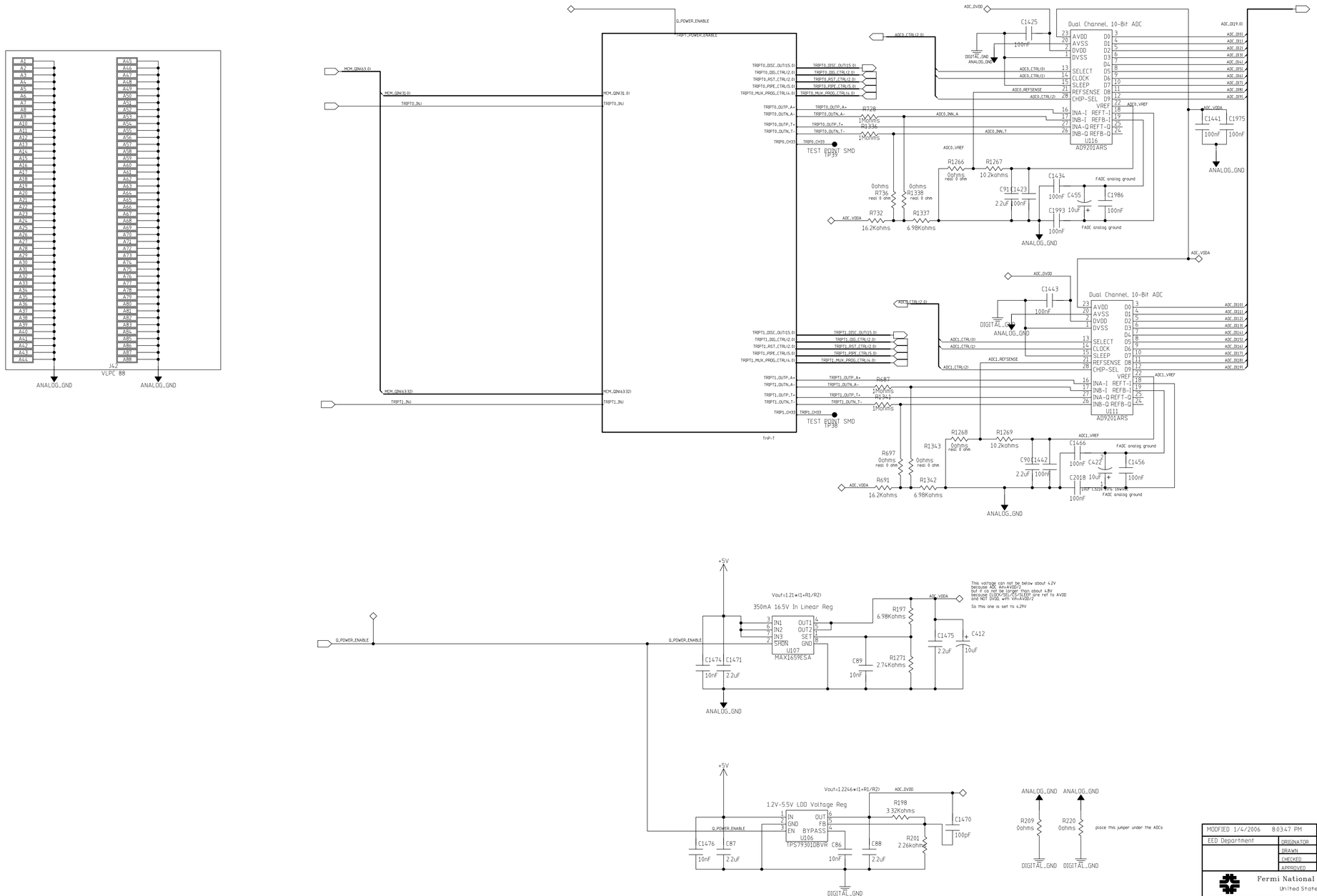

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SIZE	DRAWING NUMBER	REV
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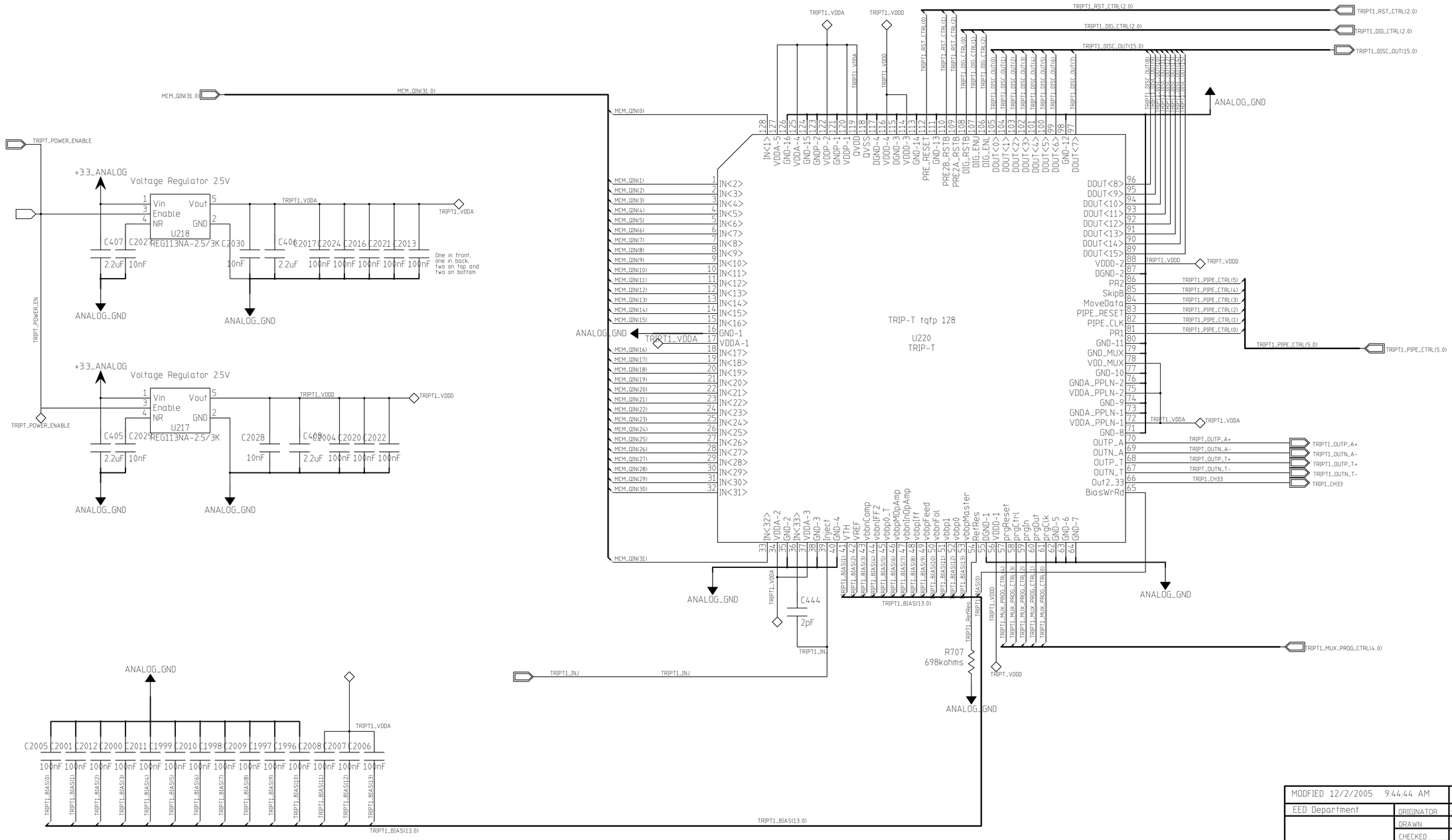
H:\BND V:\BLA



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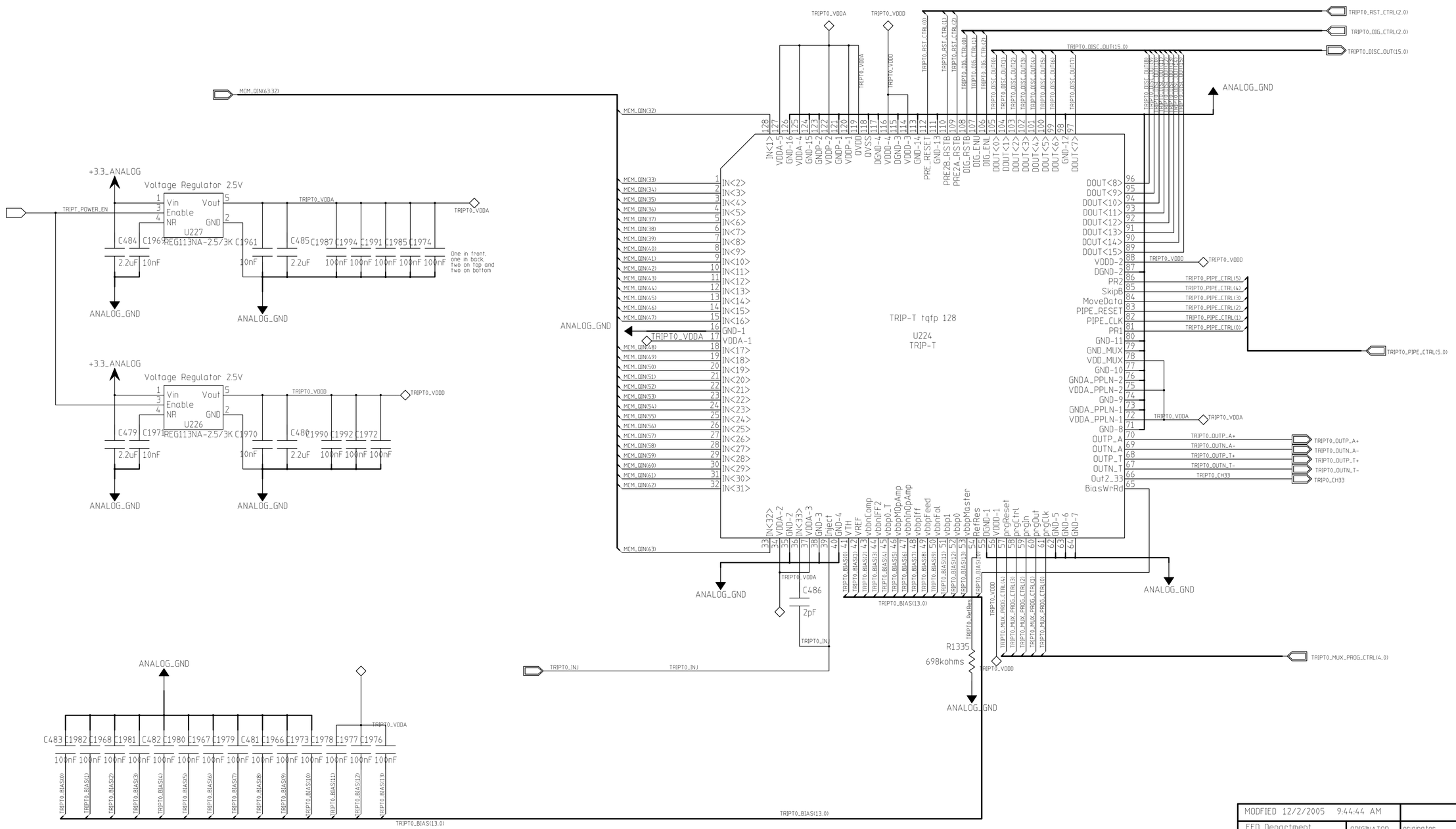

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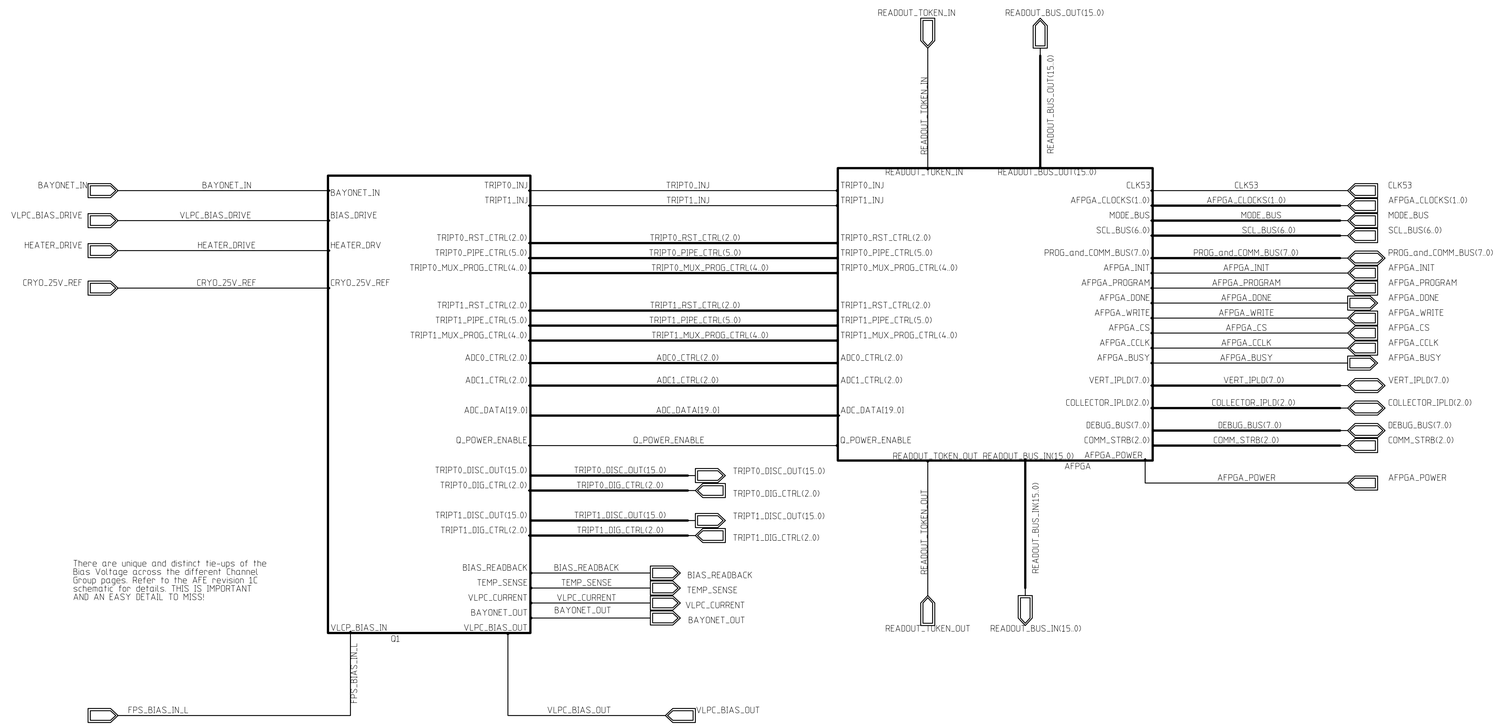

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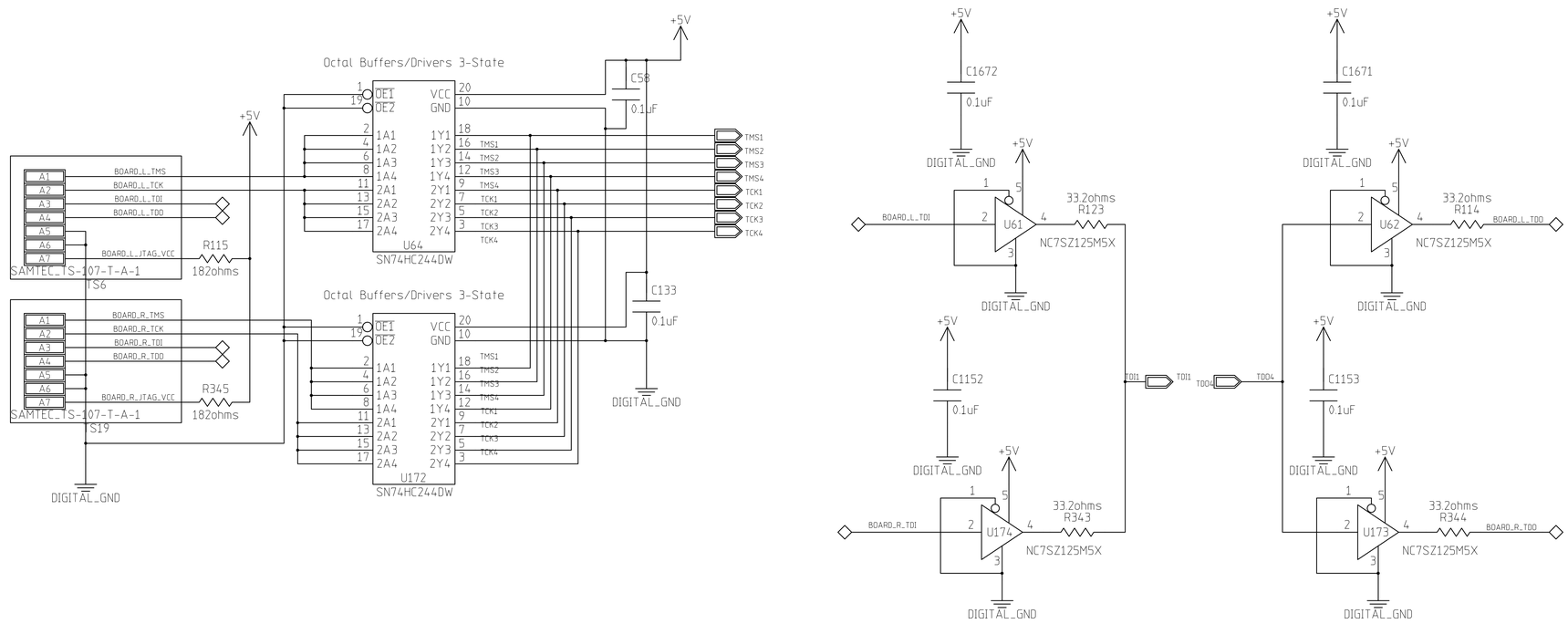

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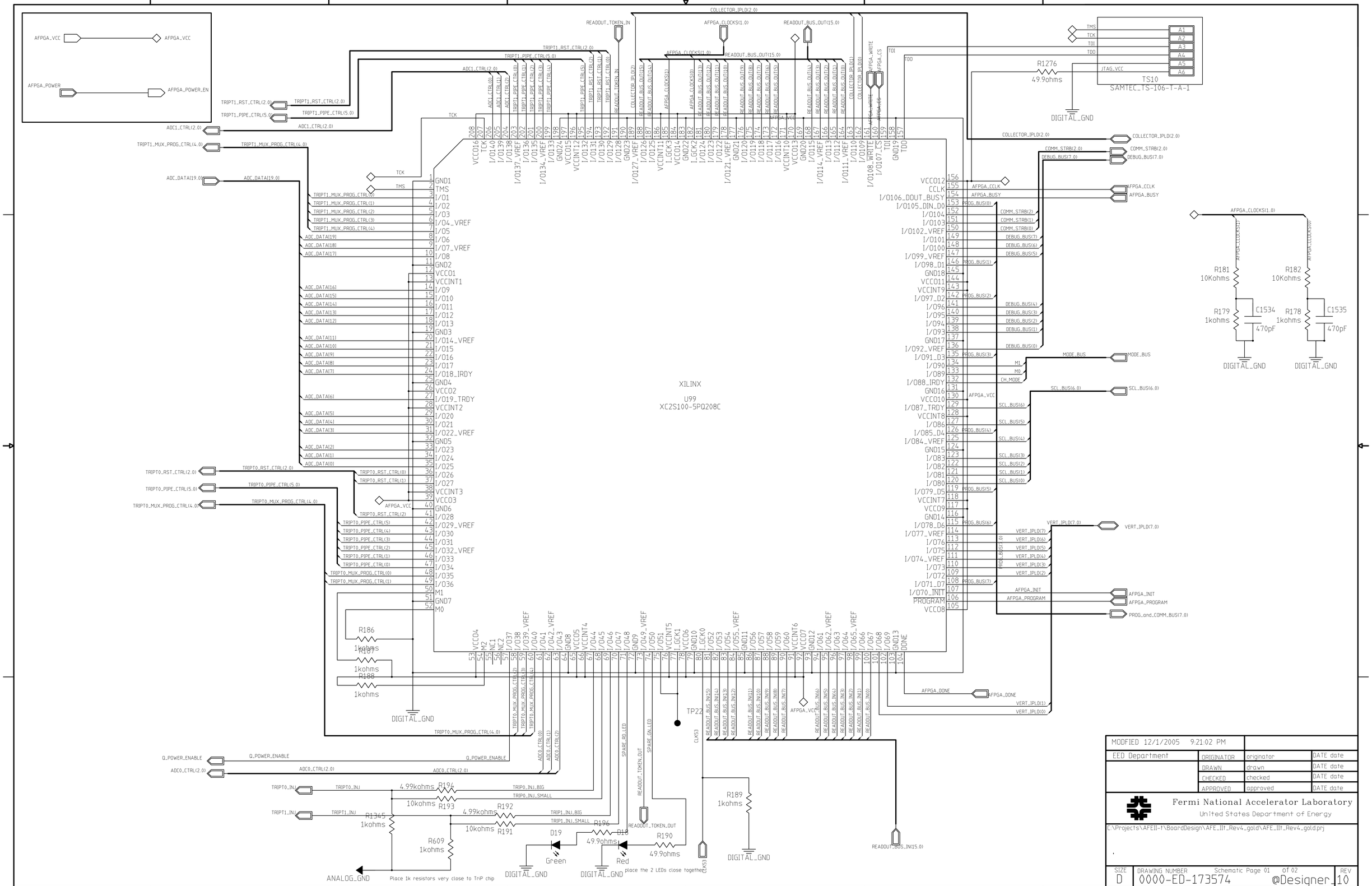

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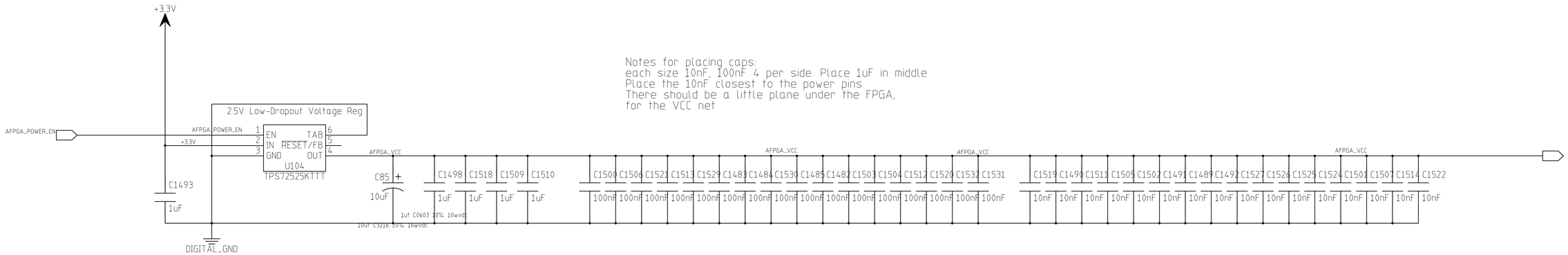

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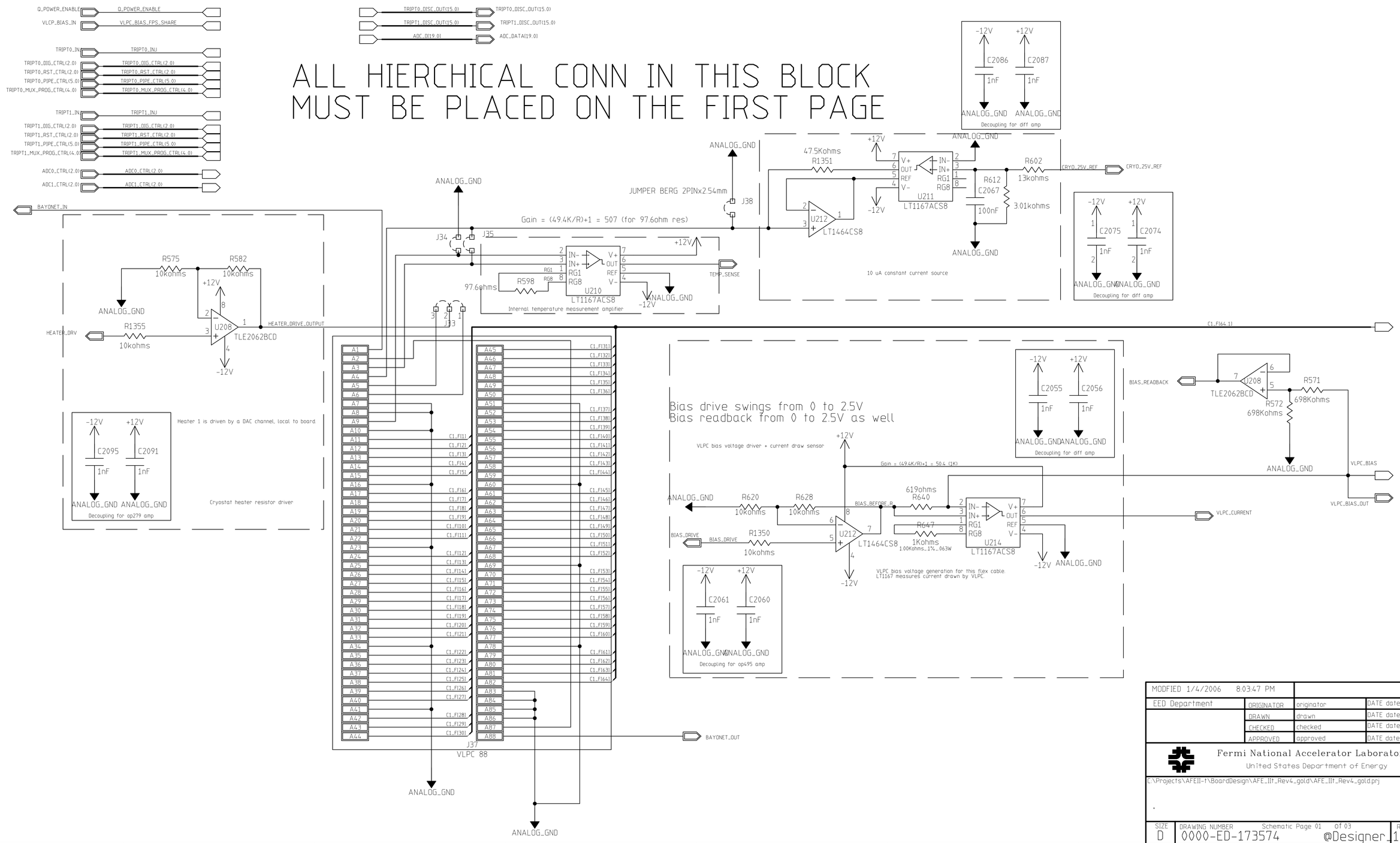
ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
BAYONET_IN
ANALOG_GND
R575
10kohms
R582
10kohms
+12V
U208
TLE2062BCD
HEATER_DRIVE_OUTPUT
HEATER_DRV
R1355
10kohms
-12V
C2095
C2091
1nF
ANALOG_GND ANALOG_GND
Decoupling for op279 amp
Heater 1 is driven by a DAC channel, local to board.
Cryostat heater resistor driver
J34
J35
J33
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
97.6ohms
R598
U210
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
JUMPER BERG 2PINx2.54mm
J38
47.5Kohms
R1351
U212
LT1464CS8
U211
LT1167ACS8
R612
C2067
100nF
R602
13kohms
3.01kohms
CRYO_25V_REF
10 uA constant current source
C2086
C2087
C2075
C2074
Decoupling for diff amp
C1_FI64.1
J37
VLPC 88
BAYONET_OUT
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R620
10kohms
R628
10kohms
BIAS_BEFORE_R
619ohms
R640
R647
1Kohms
1.00Kohms_1%_.063W
BIAS_DRIVE
R1350
10kohms
U214
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
VLPC_CURRENT
C2055
C2056
C2061
C2060
Decoupling for op495 amp
BIAS_READBACK
R571
698Kohms
R572
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
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DATE date
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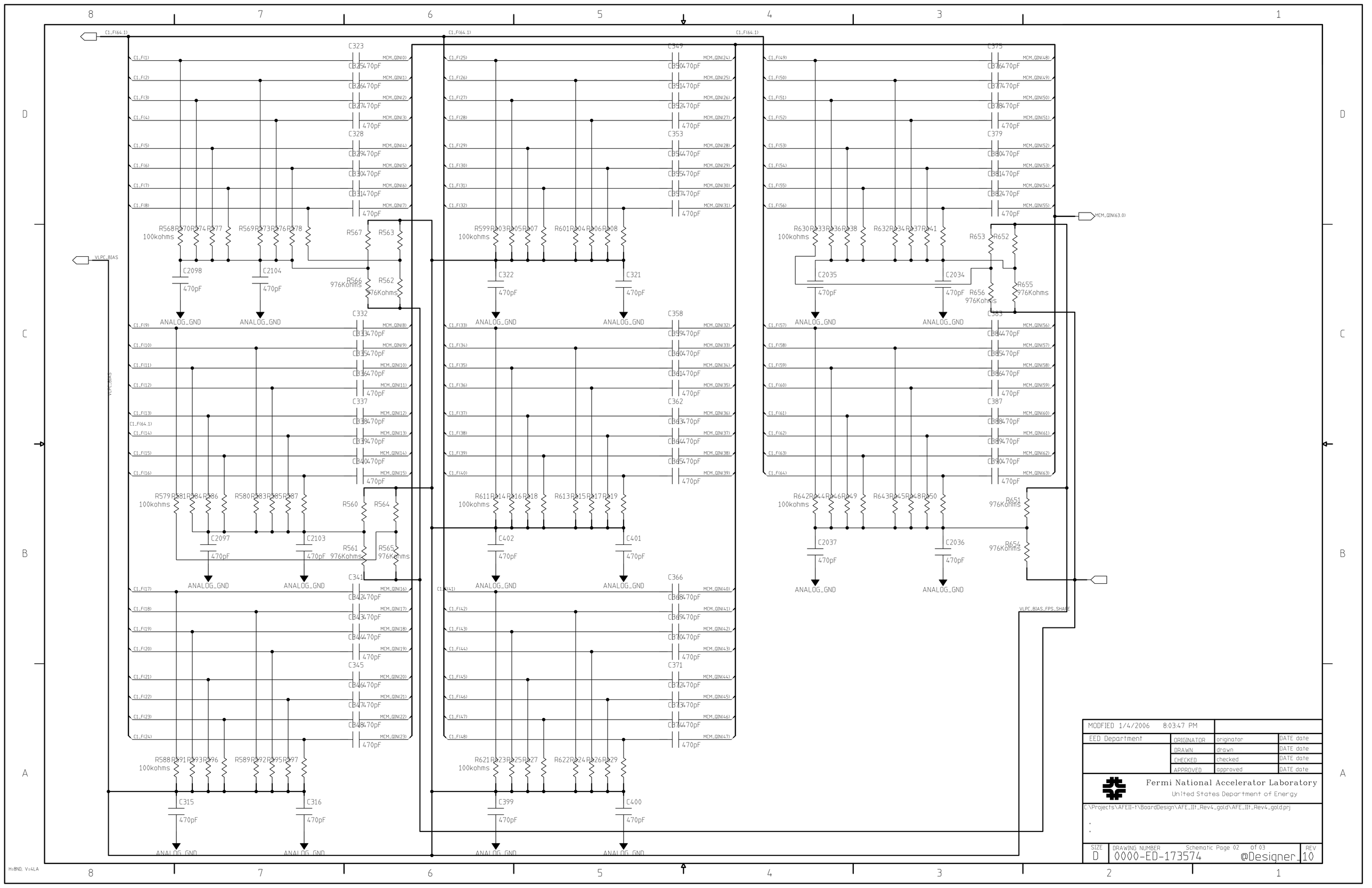
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV
H=8ND, V=4LA



C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHAPE
ANALOG_GND
100kohms
470pF
976Kohms
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ORIGINATOR originator DATE date
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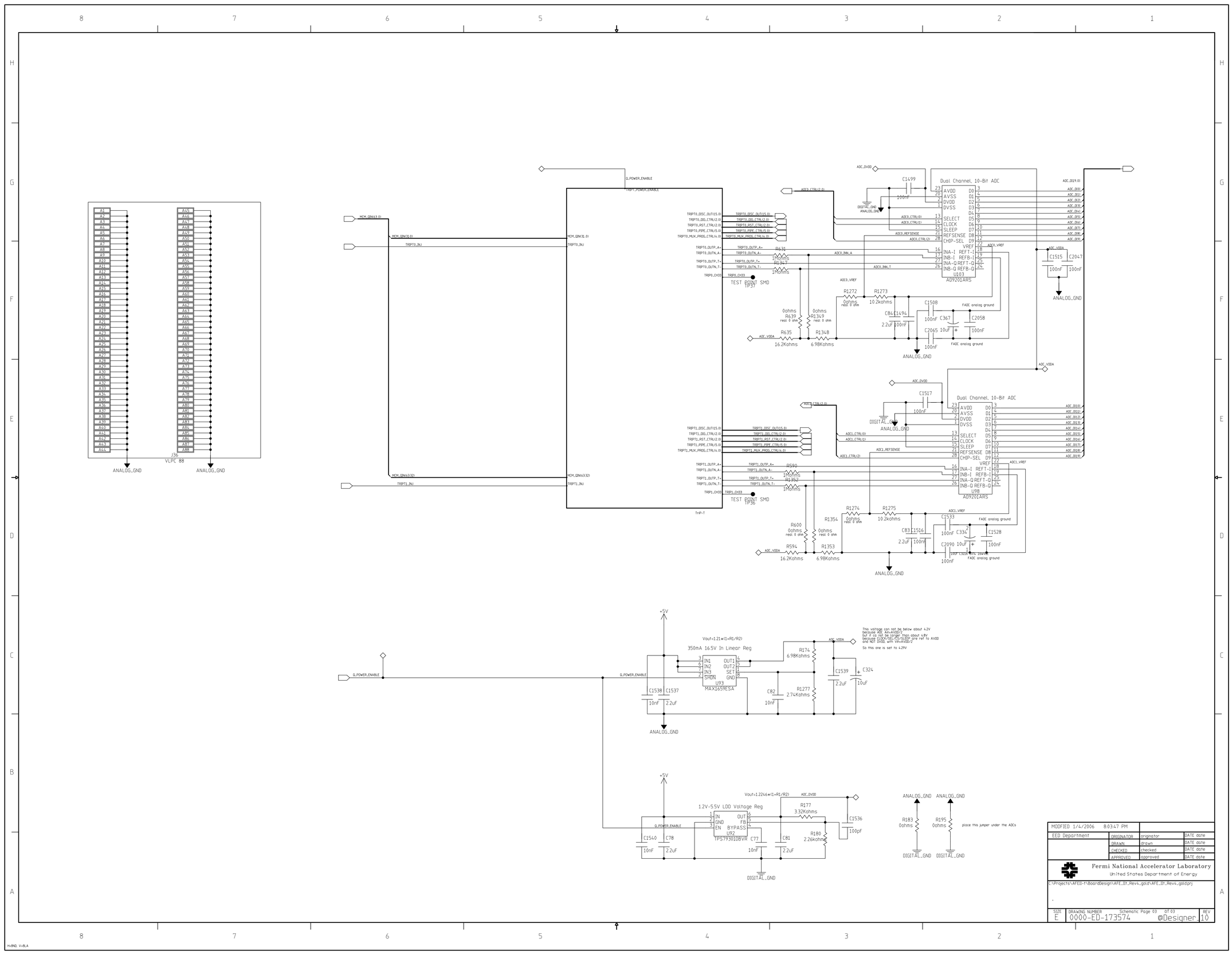
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H=8ND, V=4LA



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SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
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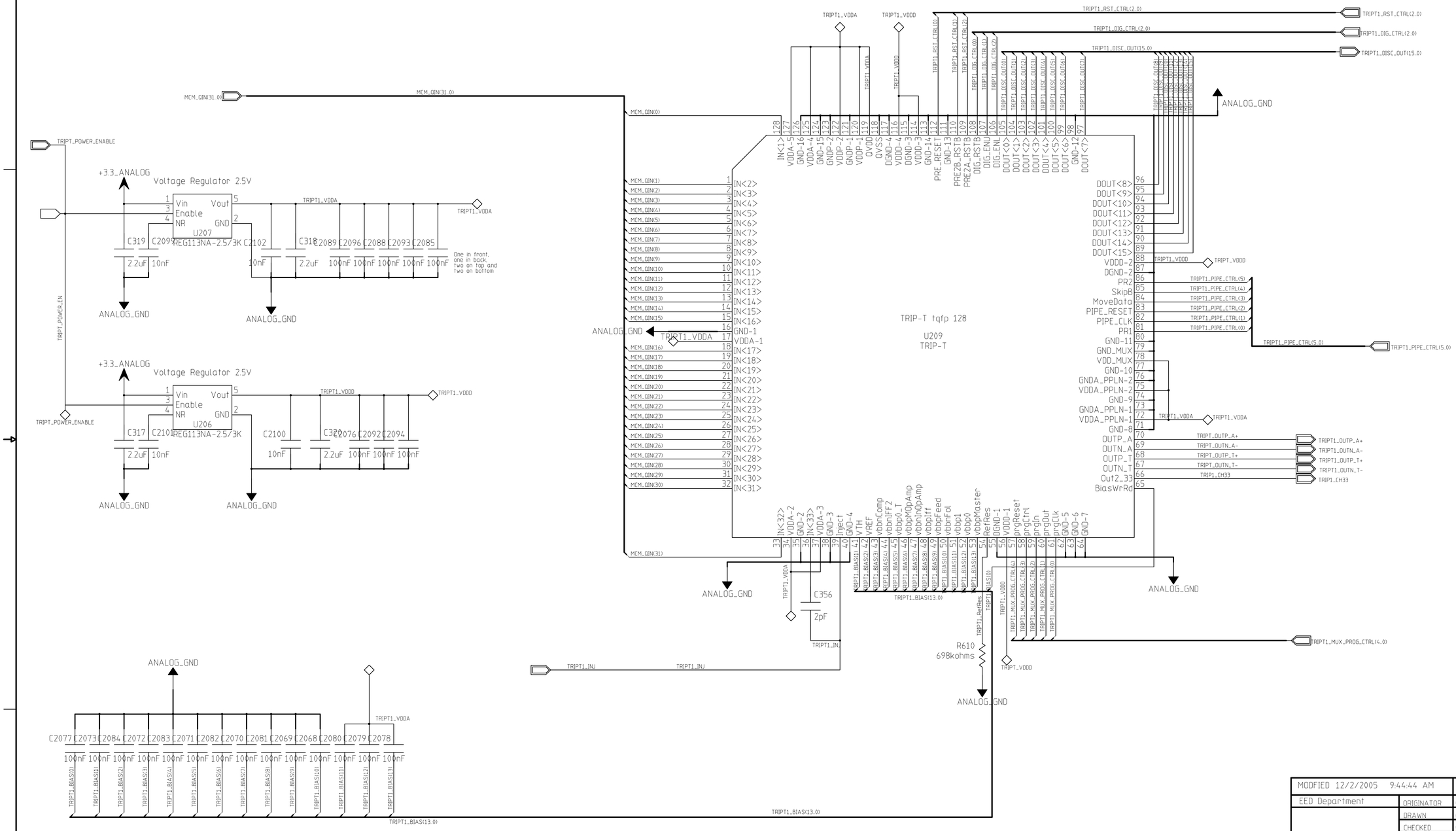

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SIZE	DRAWING NUMBER		REV
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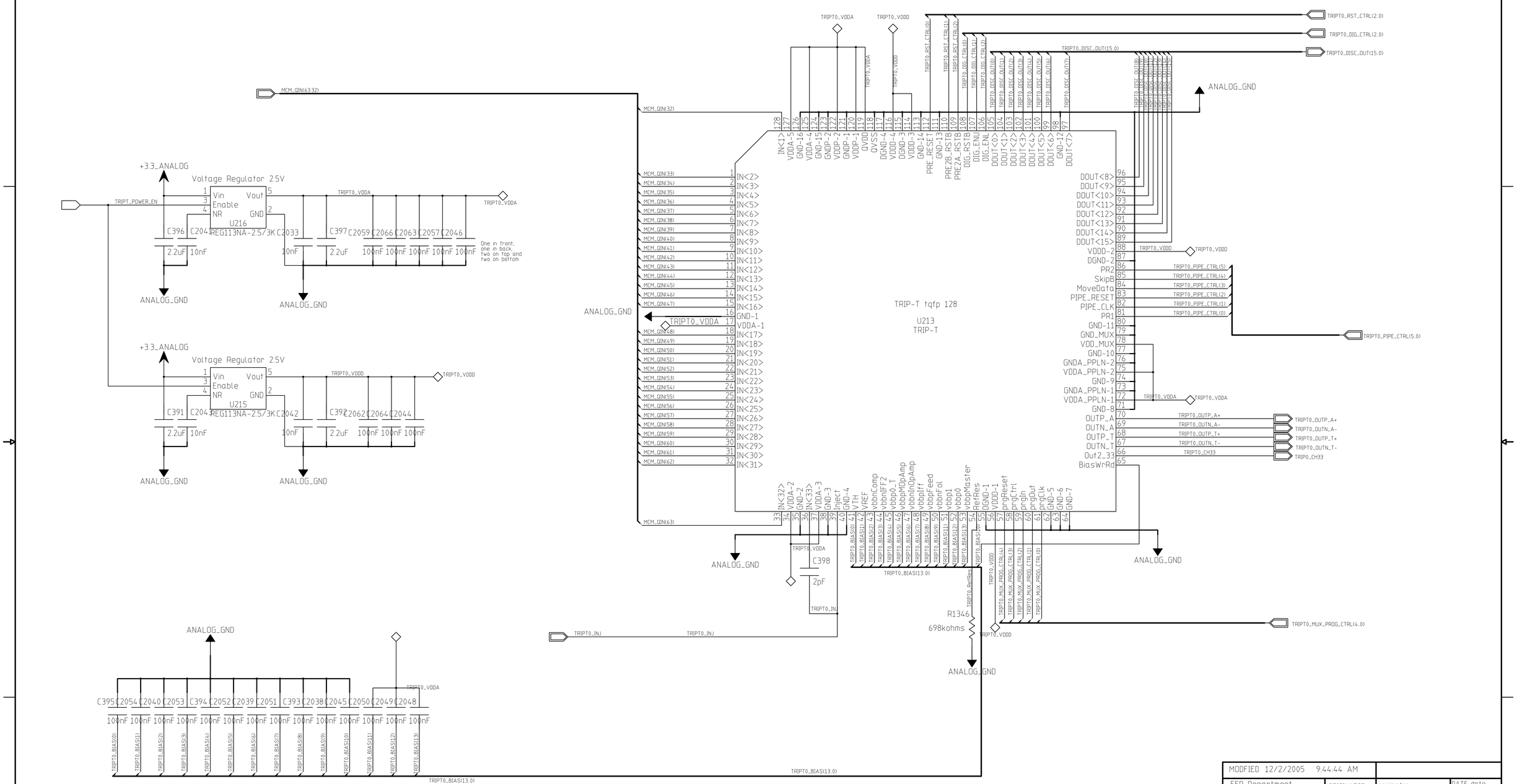

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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

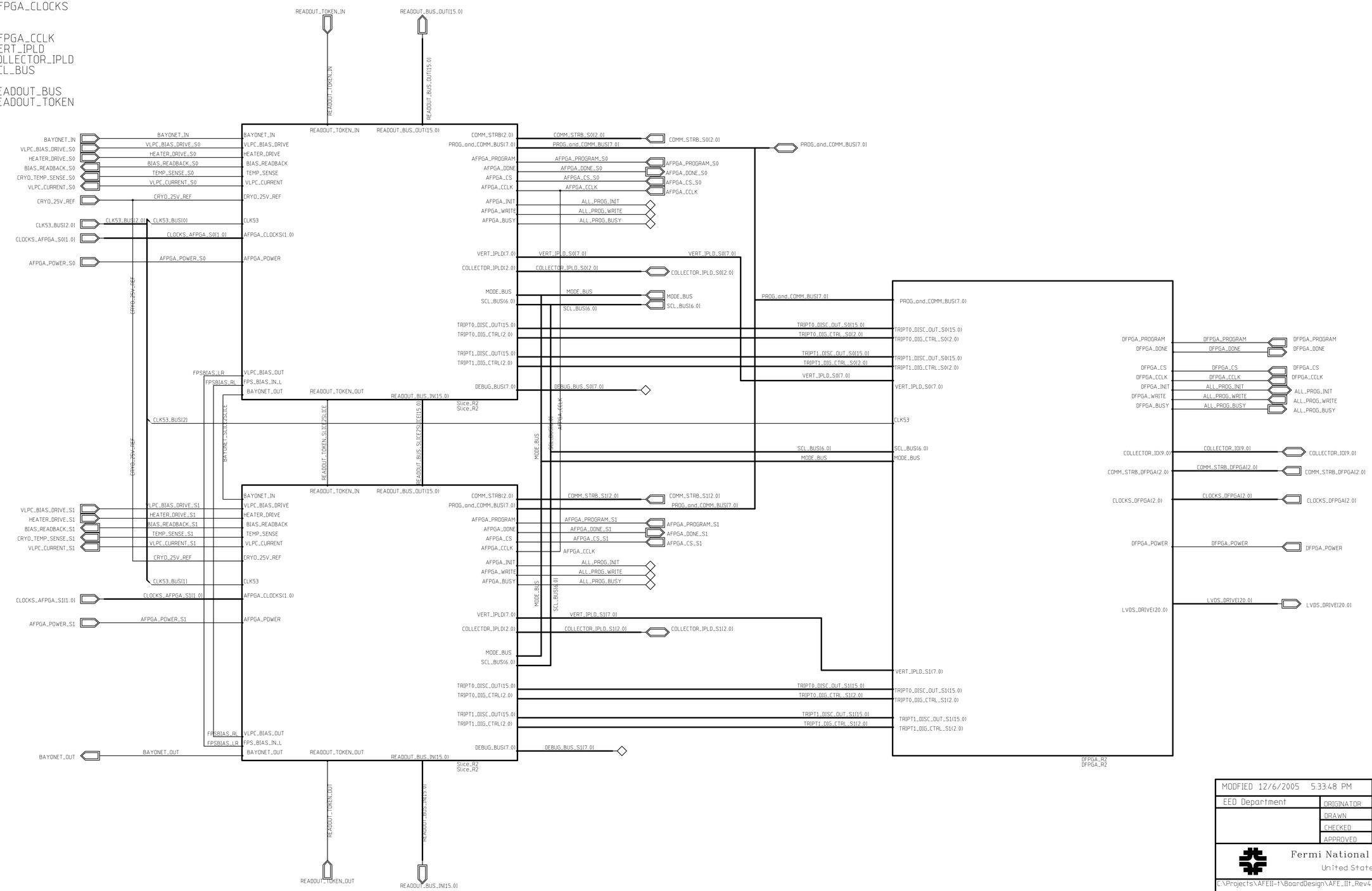
H:8ND, V:4LA

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



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SIZE	DRAWING NUMBER		REV
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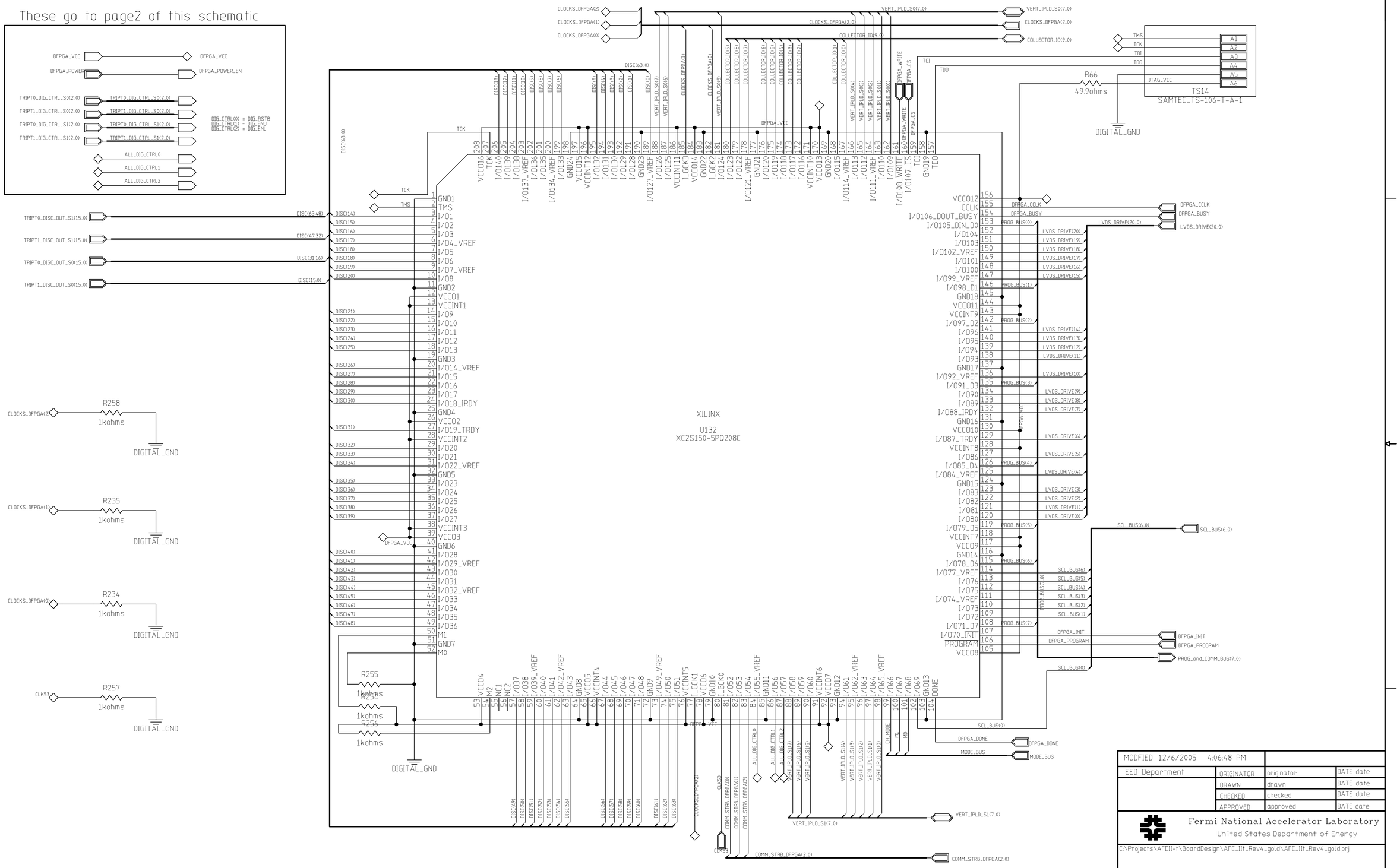

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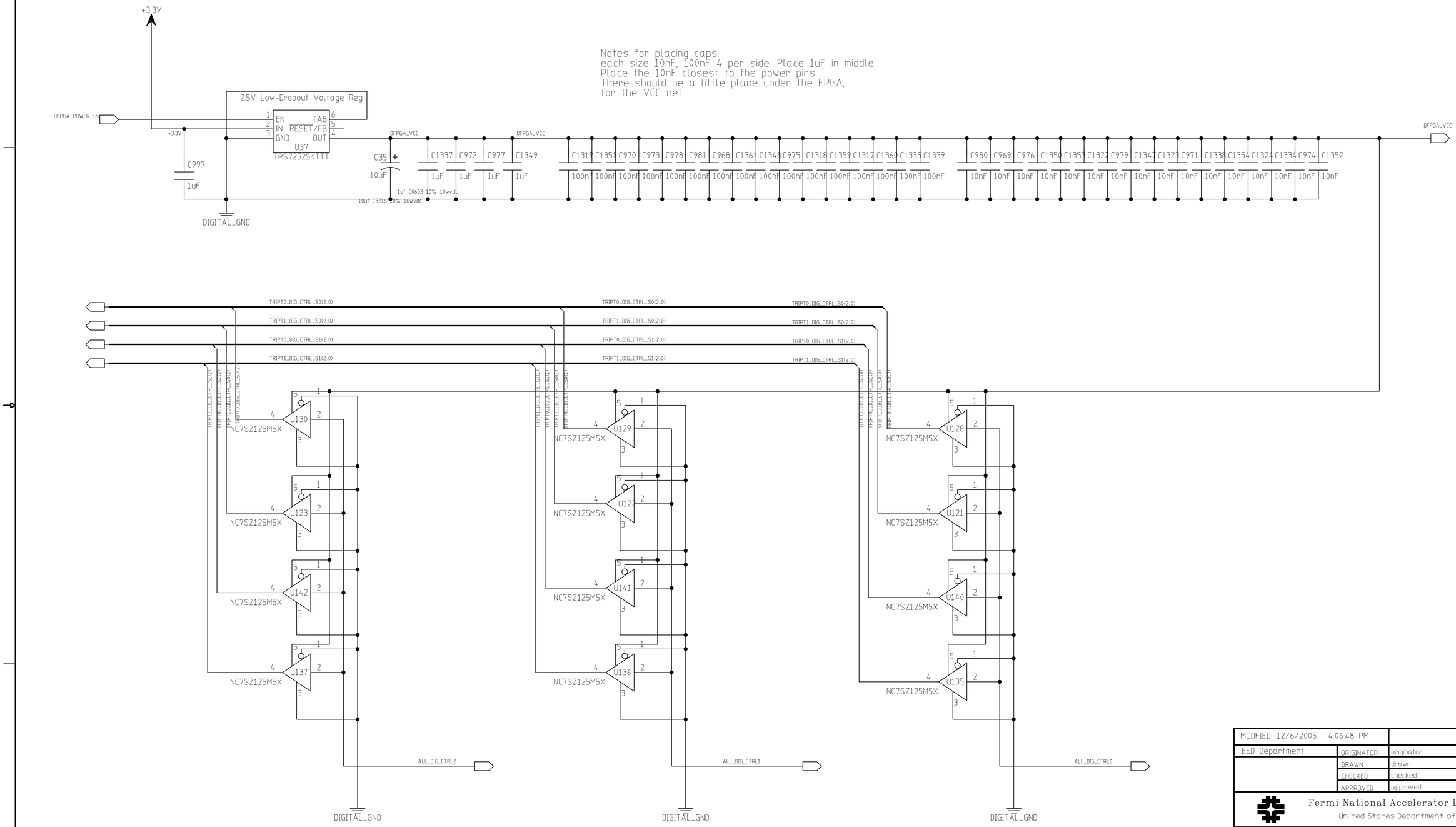
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer	10

H:8ND, V:4LA



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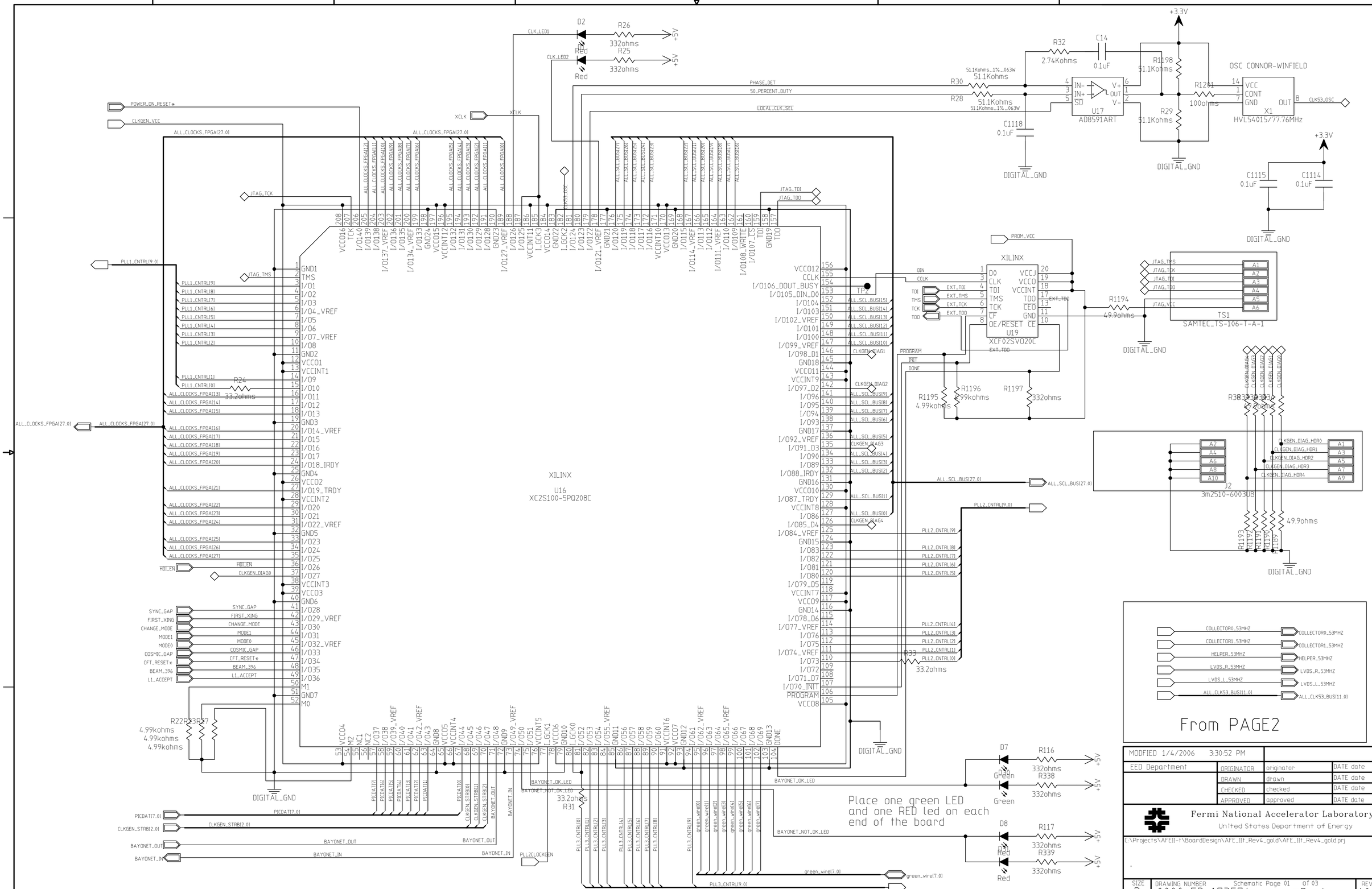
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA


XILINX
U16
XC2S100-5PQ208C
XILINX
U19
XCF02SVO20C
OSC CONNOR-WINFIELD
X1
HVL54015/77.76MHz
U17
AD8591ART
TS1
SAMTEC_TS-106-1-A-1
J2
3M2510-6003UB
From PAGE2
Place one green LED and one RED led on each end of the board
DIGITAL_GND
+3.3V
+5V
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EED Department
ORIGINATOR originator DATE date
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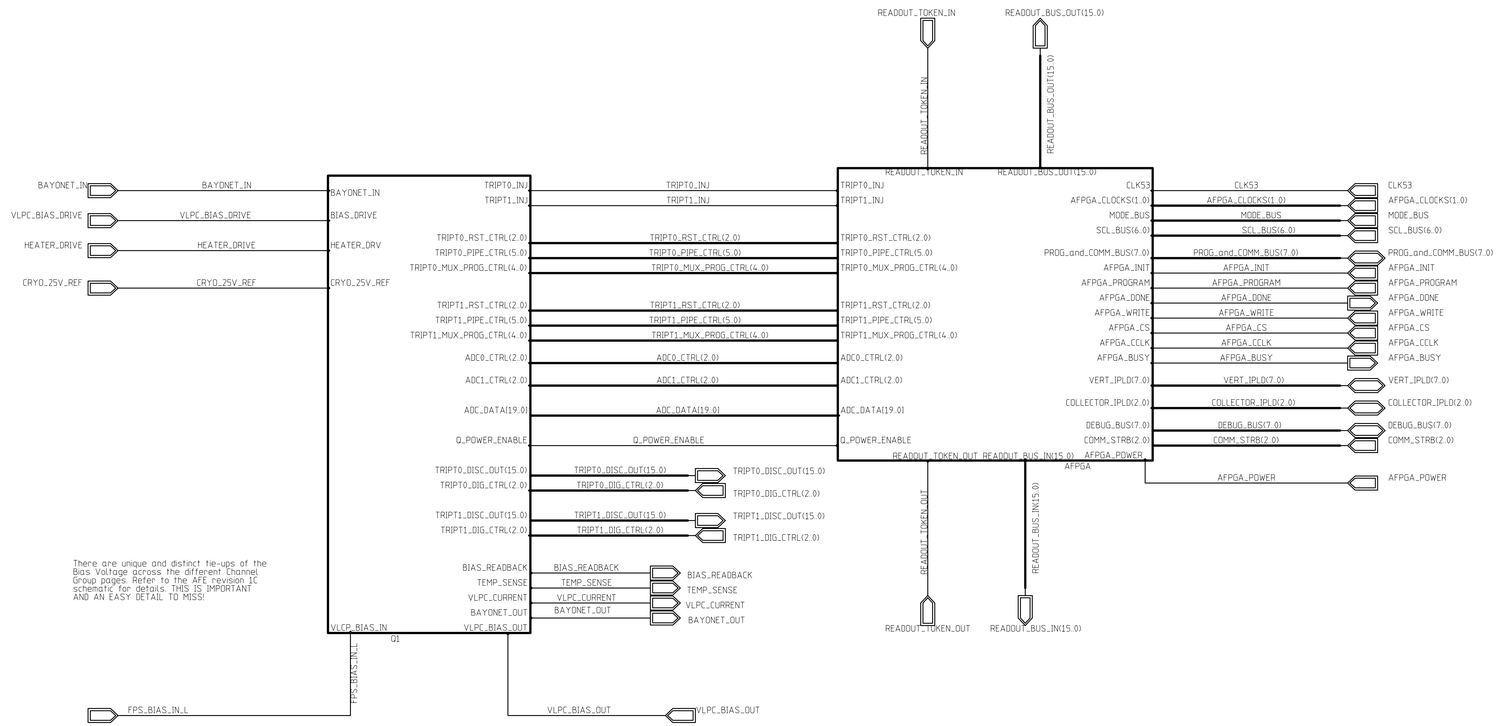
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV



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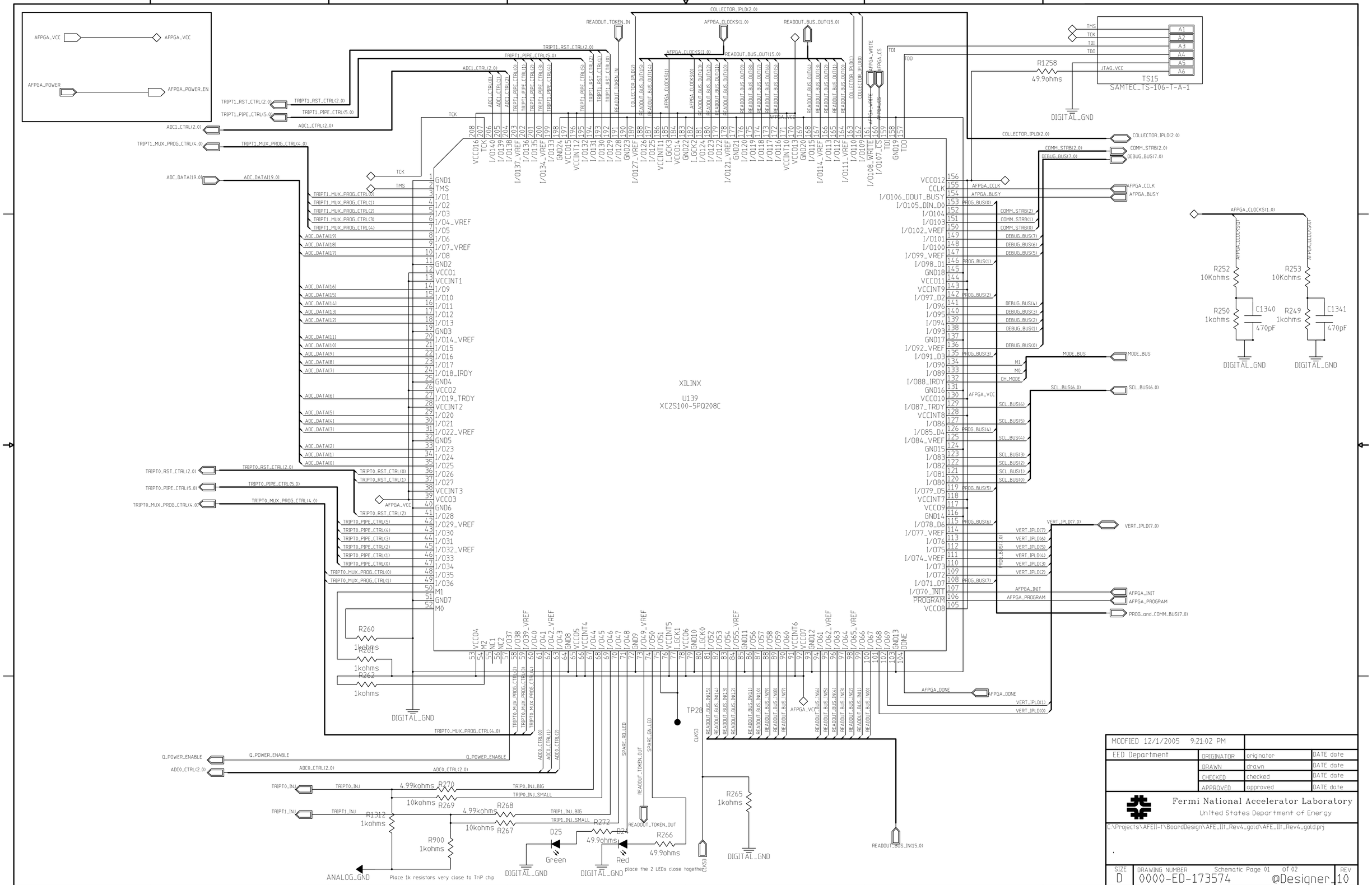
H:8ND, V:4LA


XILINX
U139
XC2S100-5PQ208C
SAMTEC_TS-106-T-A-1
TS15
R1258
49.9ohms
DIGITAL_GND
R252
10Kohms
R253
10Kohms
R250
1kohms
R249
1kohms
C1340
470pF
C1341
470pF
R260
1kohms
R261
1kohms
R262
1kohms
R270
4.99kohms
R269
10kohms
R268
4.99kohms
R267
10kohms
R1312
1kohms
R900
1kohms
R272
49.9ohms
R266
49.9ohms
R265
1kohms
D25
Green
D24
Red
TP28
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
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ORIGINATOR originator DATE date
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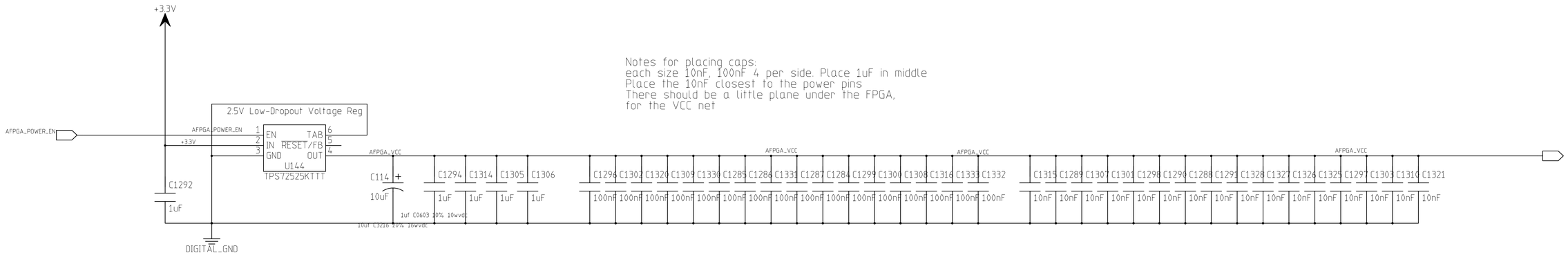
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 02
@Designer
REV 10



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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SIZE	DRAWING NUMBER		REV
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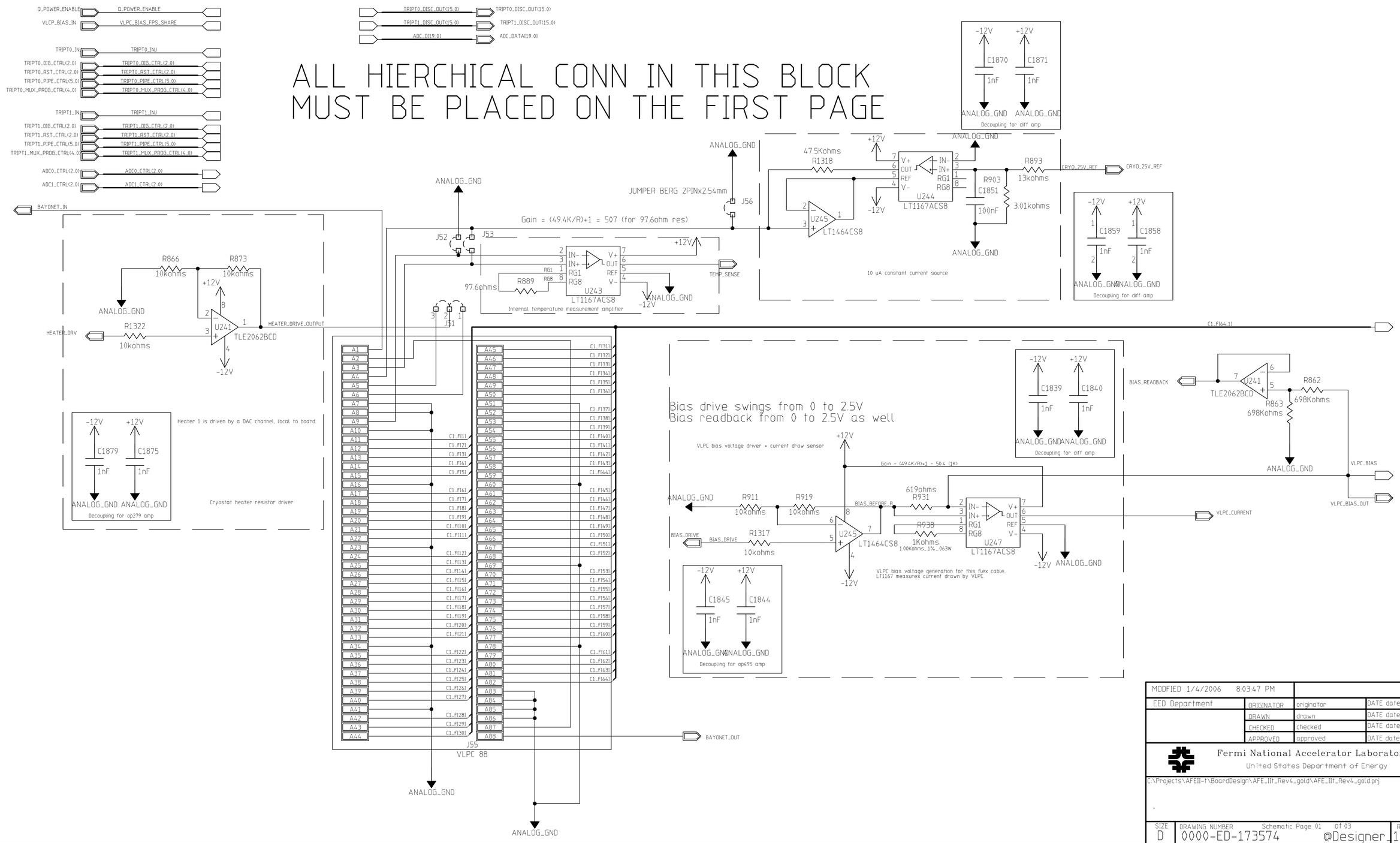
ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
BAYONET_IN
ANALOG_GND
HEATER_DRV
R1322
10kohms
R866
R873
U241
TLE2062BCD
HEATER_DRIVE_OUTPUT
-12V
+12V
C1879
C1875
1nF
Heater 1 is driven by a DAC channel, local to board.
Cryostat heater resistor driver
Decoupling for op279 amp
J52
J53
J51
J55
VLPC 88
JUMPER BERG 2PINx2.54mm
J56
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
R889
97.6ohms
U243
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
47.5Kohms
R1318
U245
LT1464CS8
U244
R893
13kohms
CRYO_25V_REF
R903
3.01kohms
C1851
100nF
10 uA constant current source
C1870
C1871
Decoupling for diff amp
C1859
C1858
C1_FI64_1
BAYONET_OUT
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R911
R919
BIAS_BEFORE_R
619ohms
R931
R938
1Kohms
1.00Kohms_1%_.063W
U247
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
BIAS_DRIVE
R1317
C1845
C1844
Decoupling for op495 amp
C1839
C1840
BIAS_READBACK
R862
698Kohms
R863
VLPC_BIAS
VLPC_BIAS_OUT
VLPC_CURRENT
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DATE date
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Schematic Page 01 of 03
@Designer_10
REV
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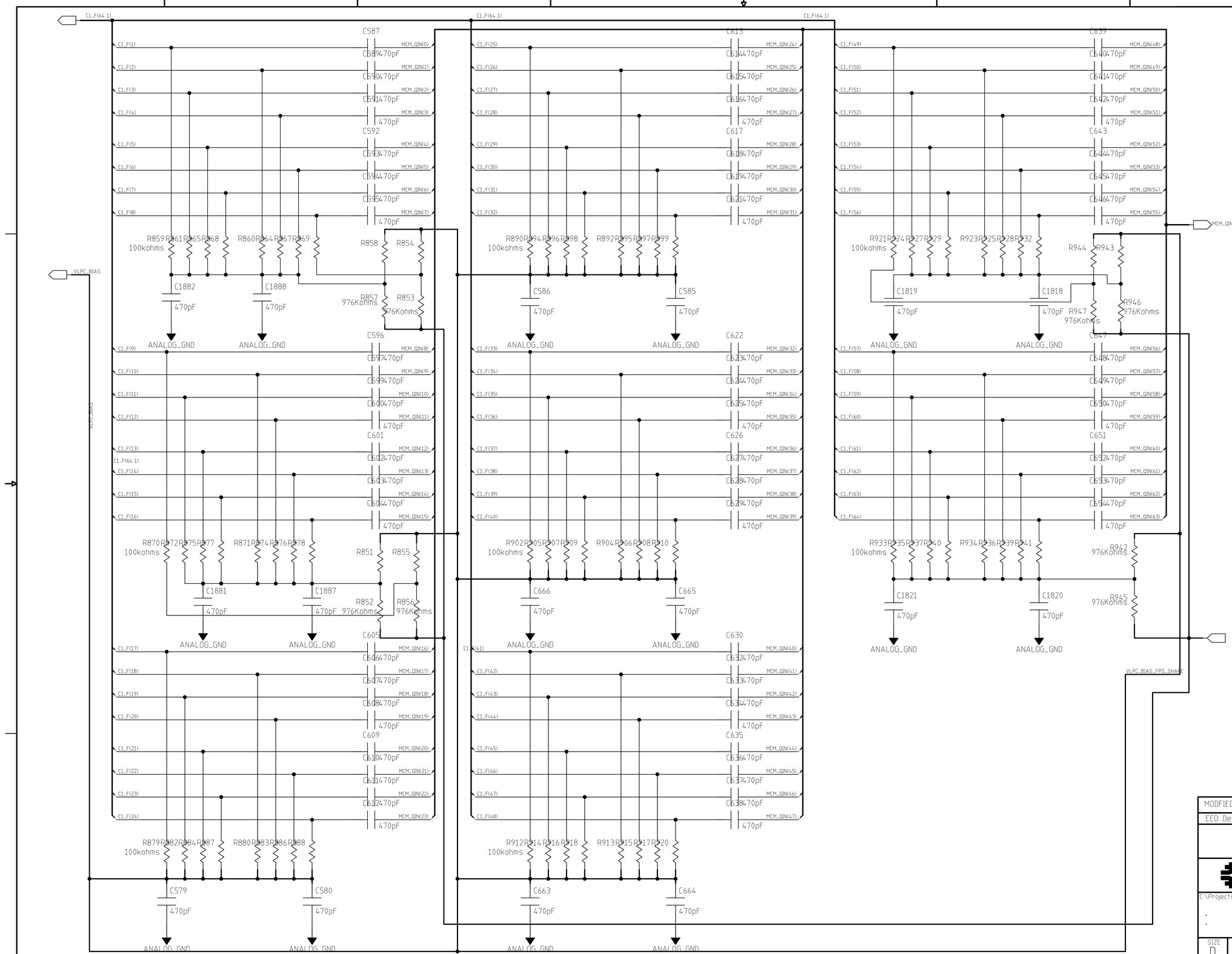

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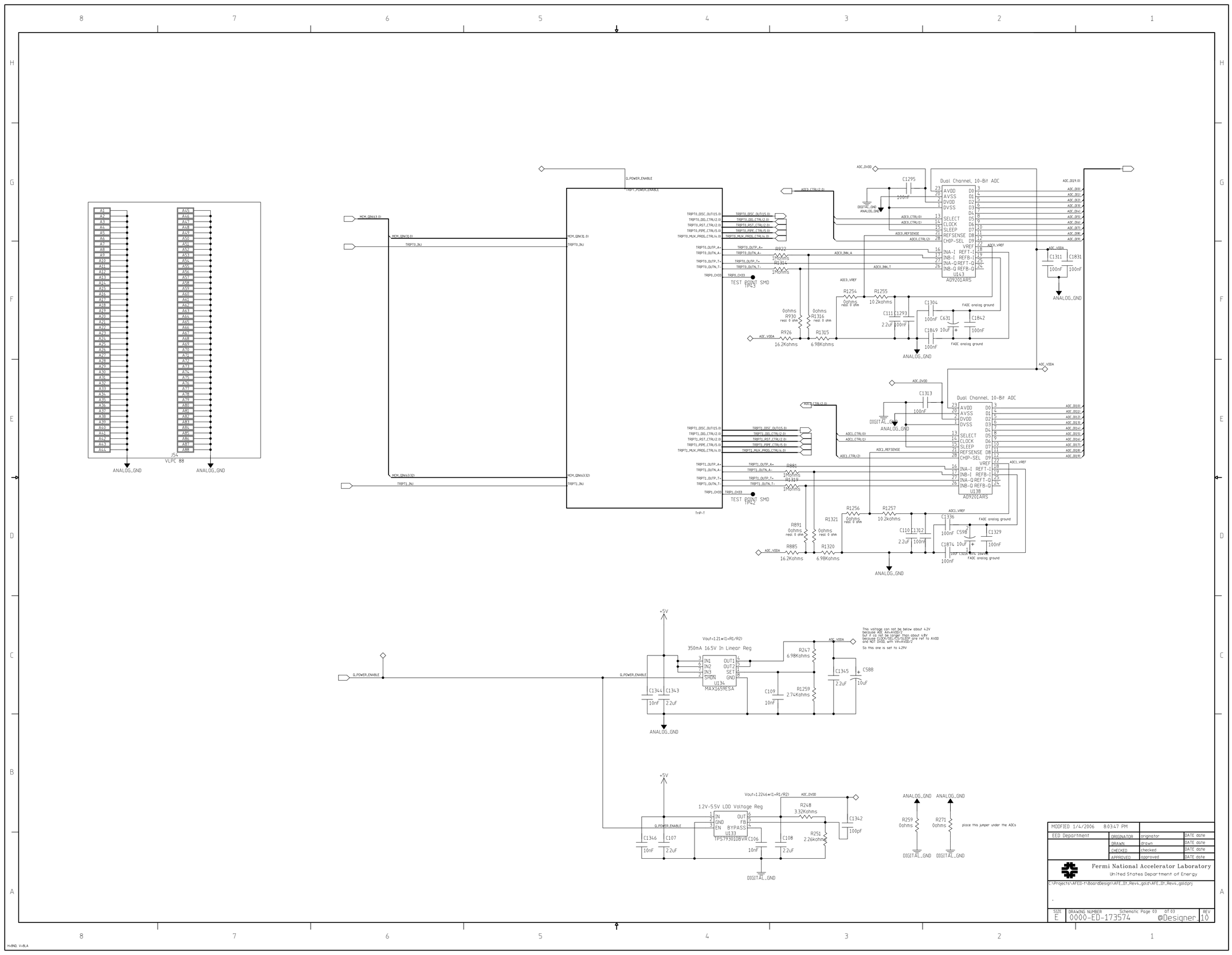

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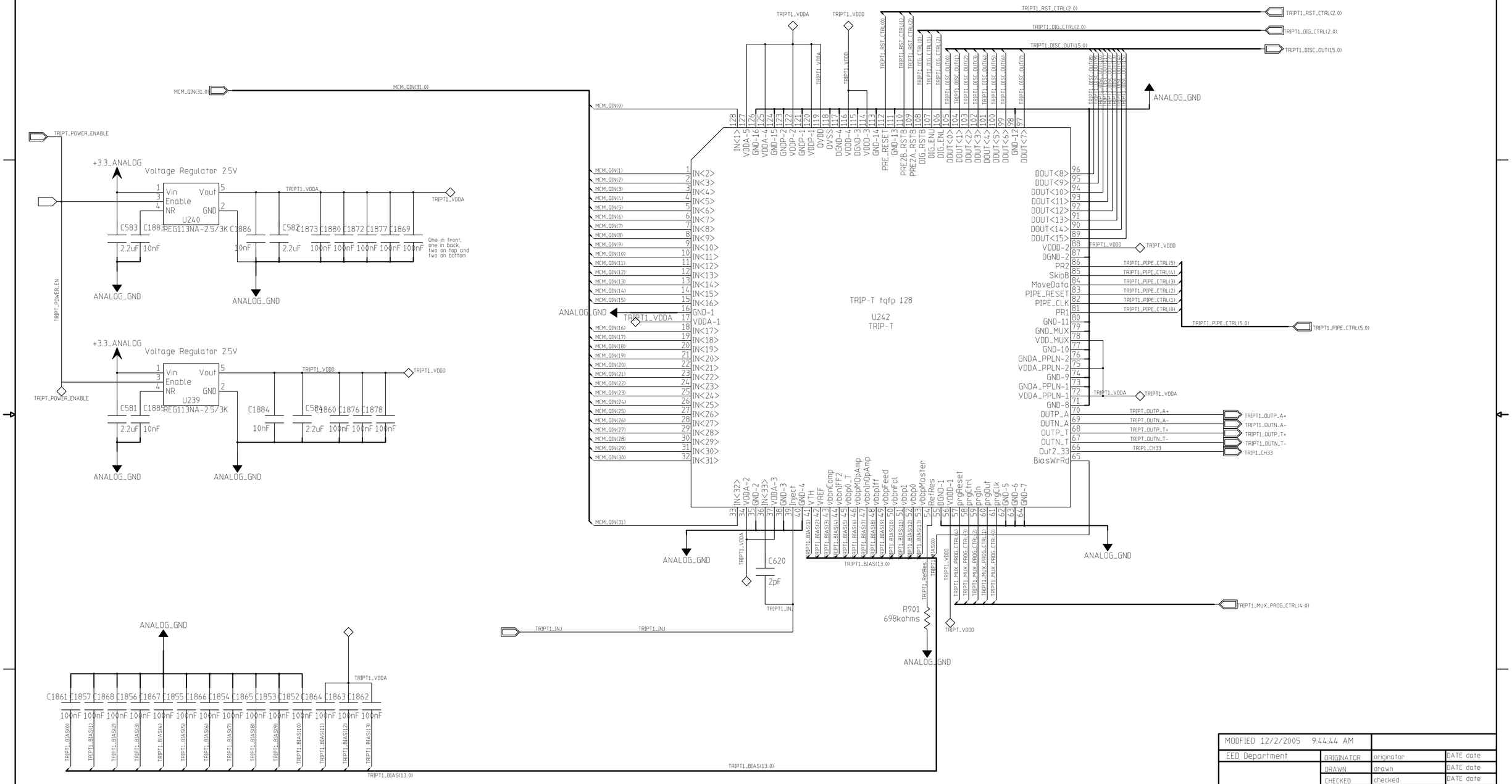

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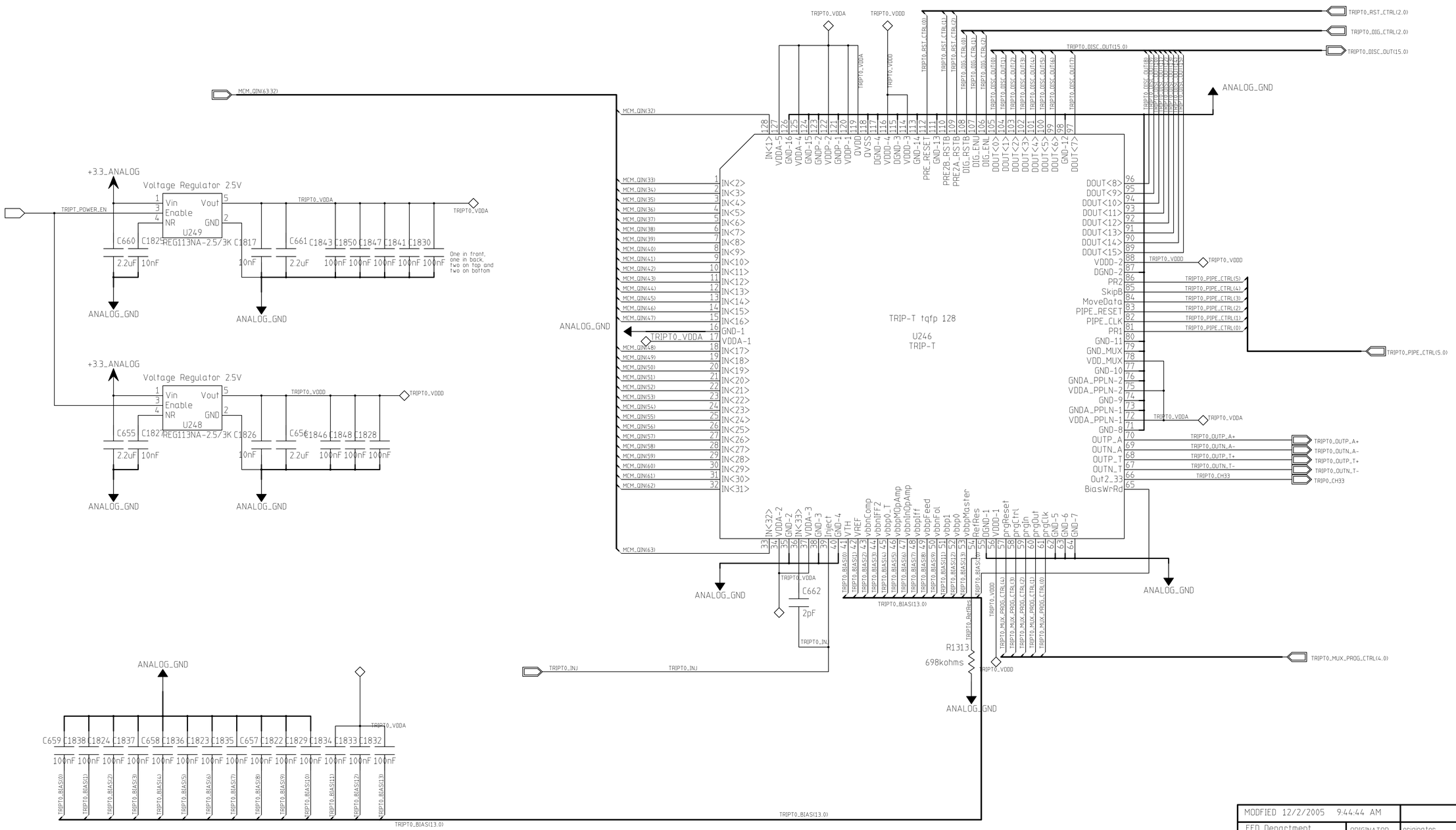

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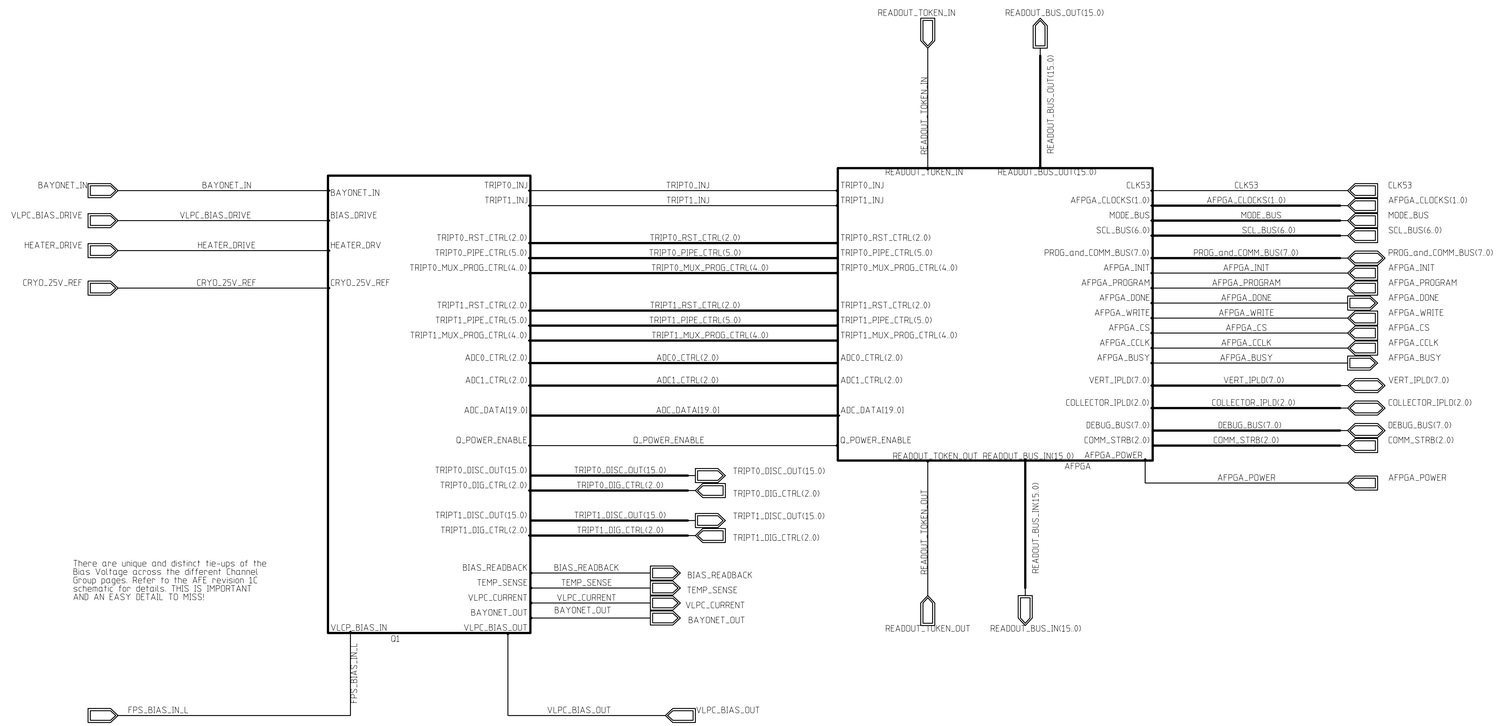

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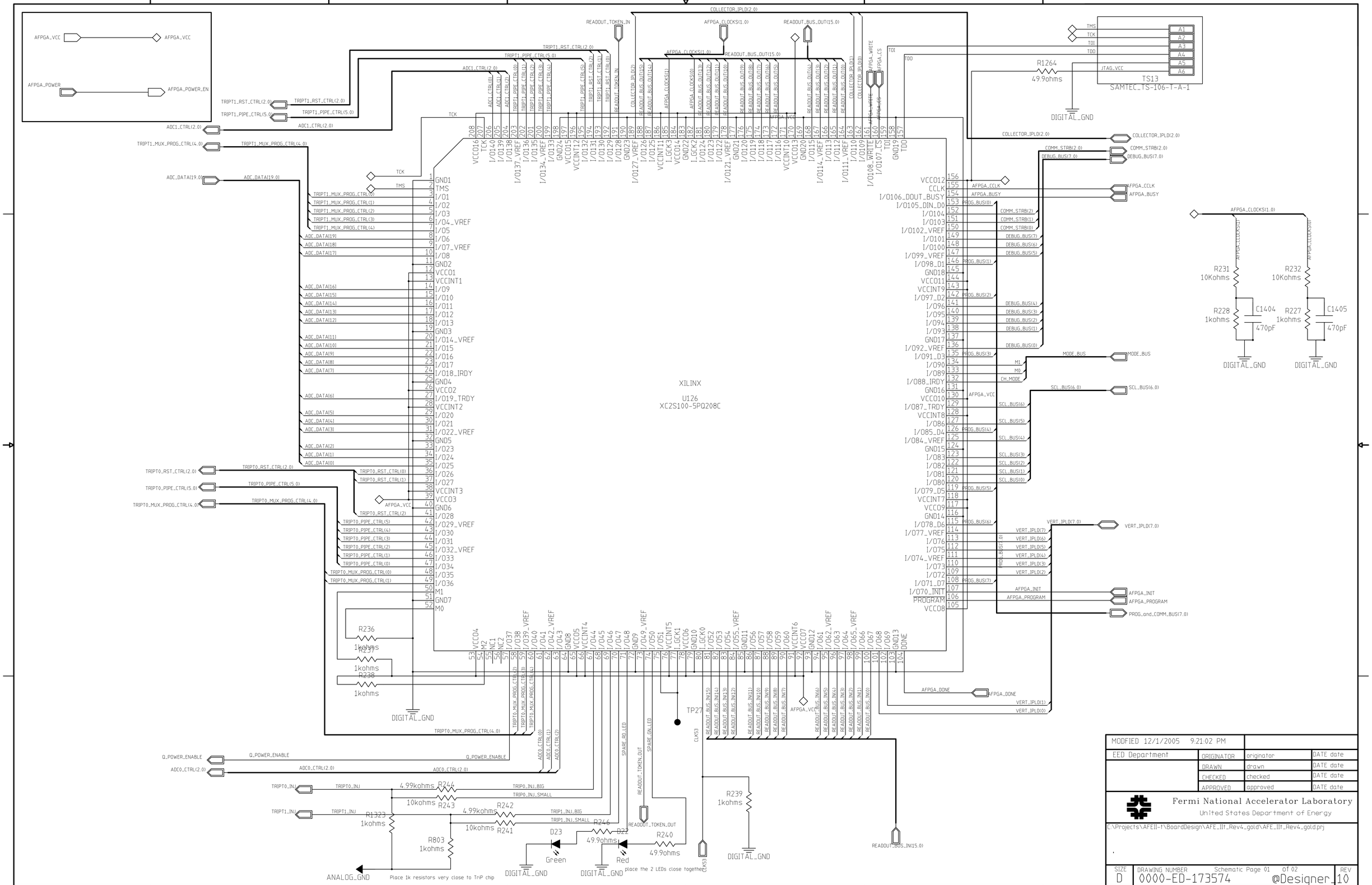

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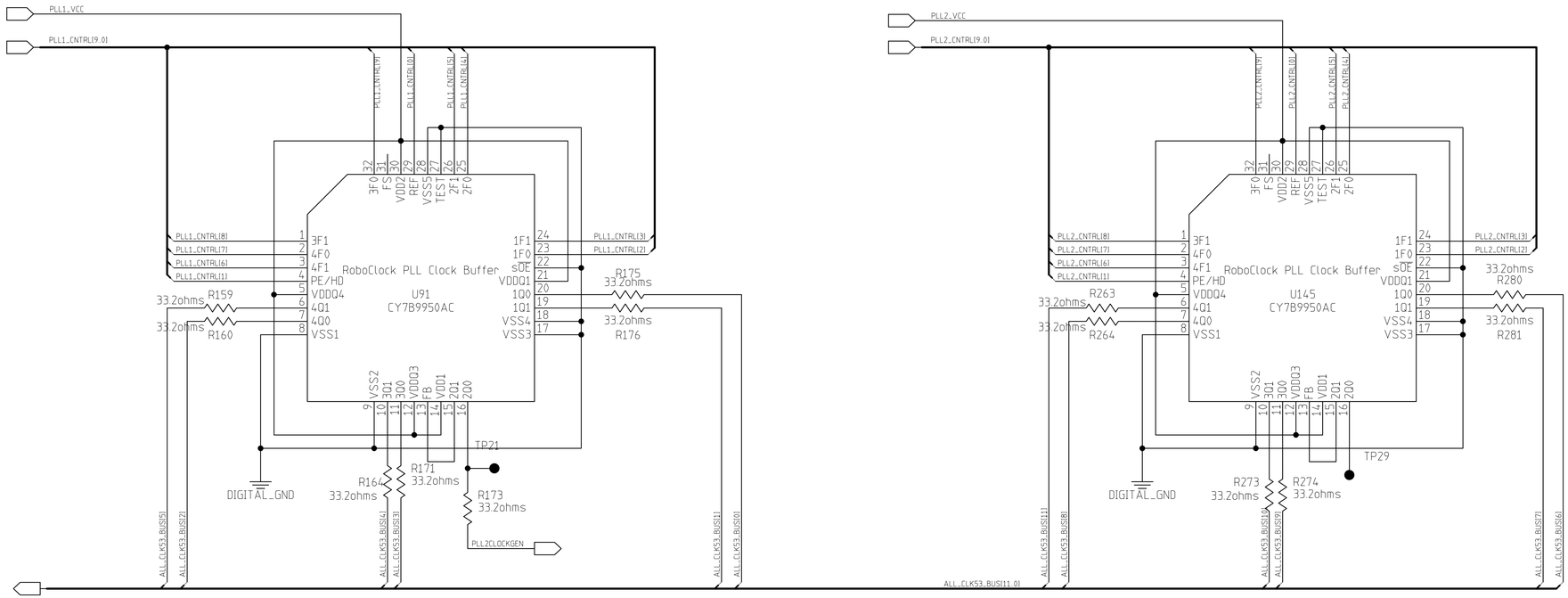

ALL_CLK53_BUS[11..0]

0 = AFPGA0 CLK53
1 = AFPGA1 CLK53
2 = DFPGA01 CLK53
3 = AFPGA2 CLK53
4 = AFPGA3 CLK53
5 = DFPGA23 CLK53
6 = AFPGA4 CLK53
7 = AFPGA5 CLK53
8 = DFPGA45 CLK53
9 = AFPGA6 CLK53
10 = AFPGA7 CLK53
11 = DFPGA67 CLK53

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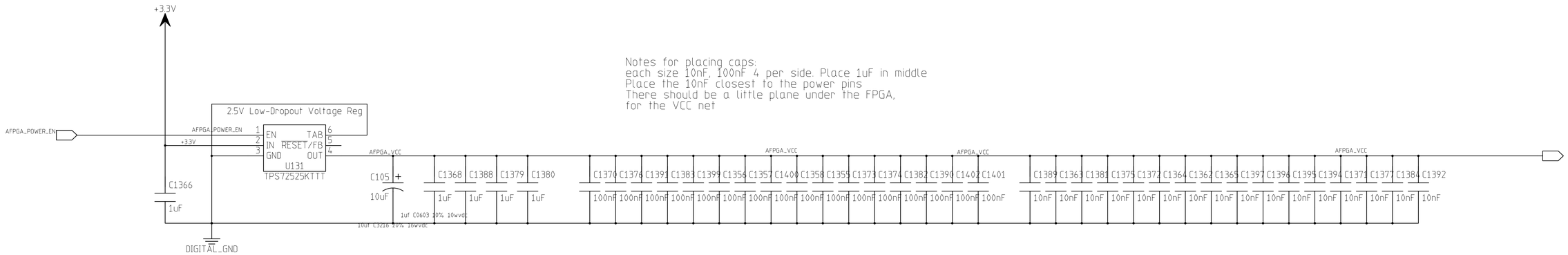
SIZE D | DRAWING NUMBER 0000-ED-173574 | Schematic Page 02 of 03 | @Designer_10 | REV

H:8ND, V:4LA



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
for the VCC net

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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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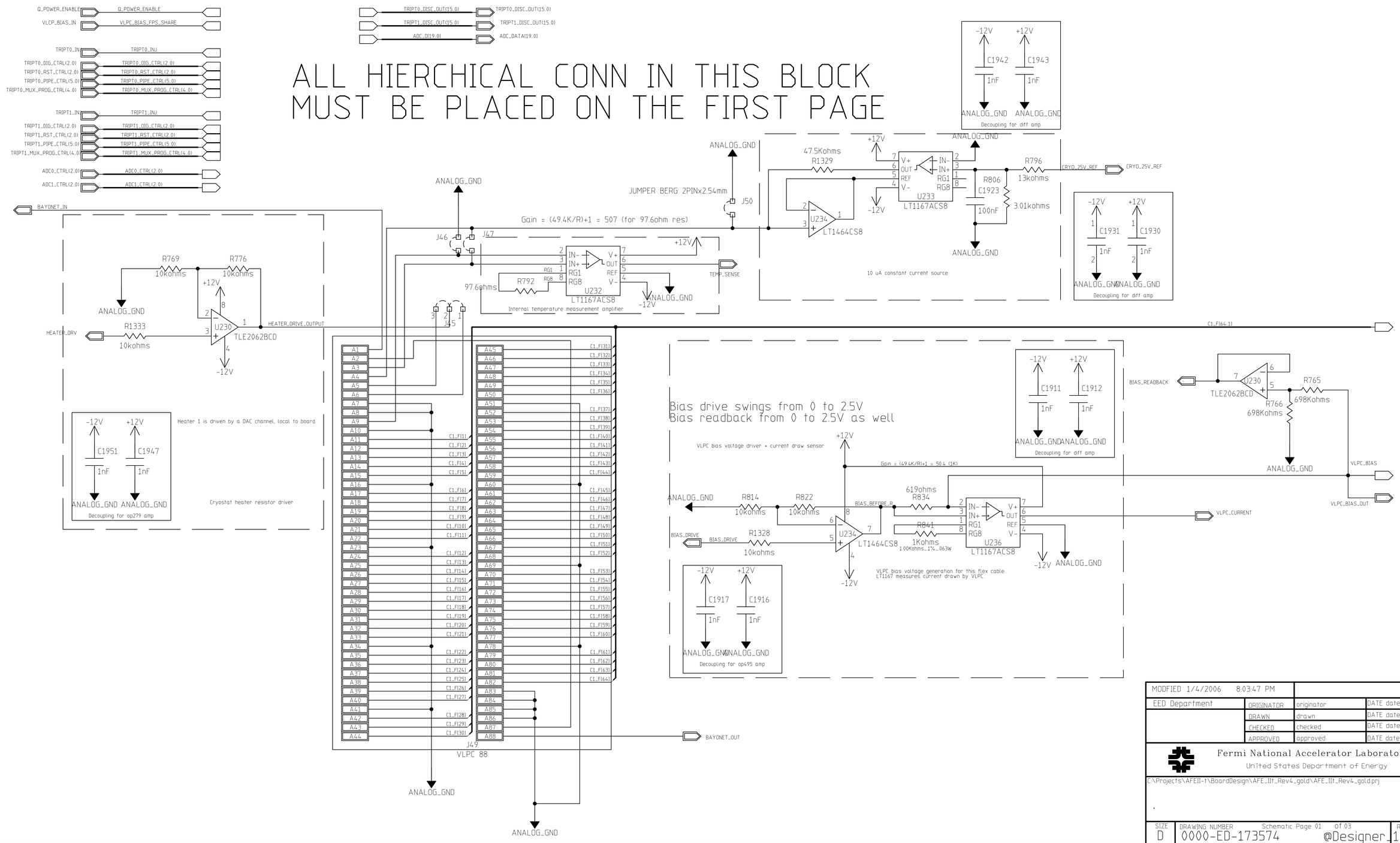
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA



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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
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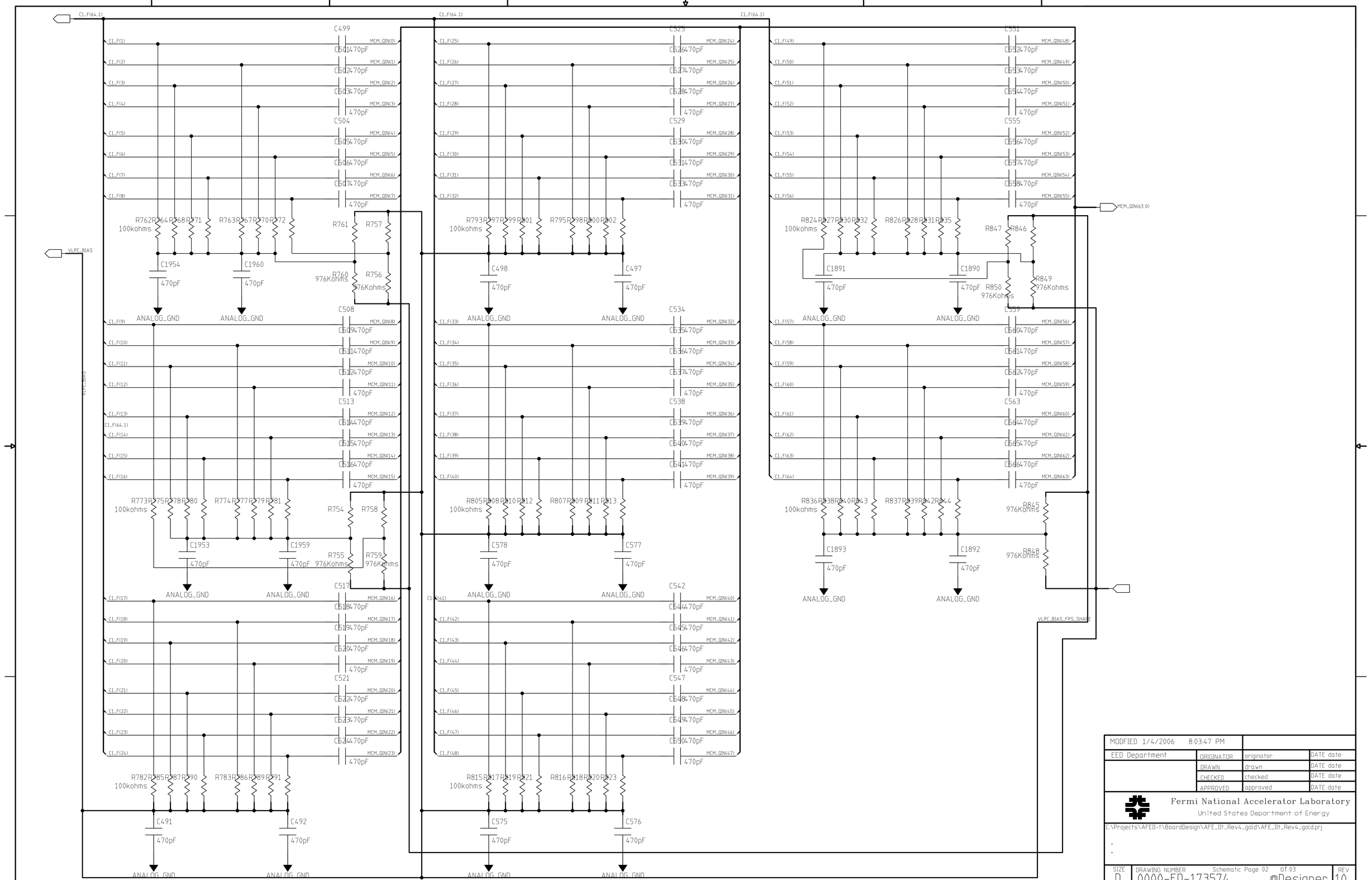
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer	10

H:8ND, V:4LA


C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
100kohms
976Kohms
470pF
MODFIED 1/4/2006 8:03:47 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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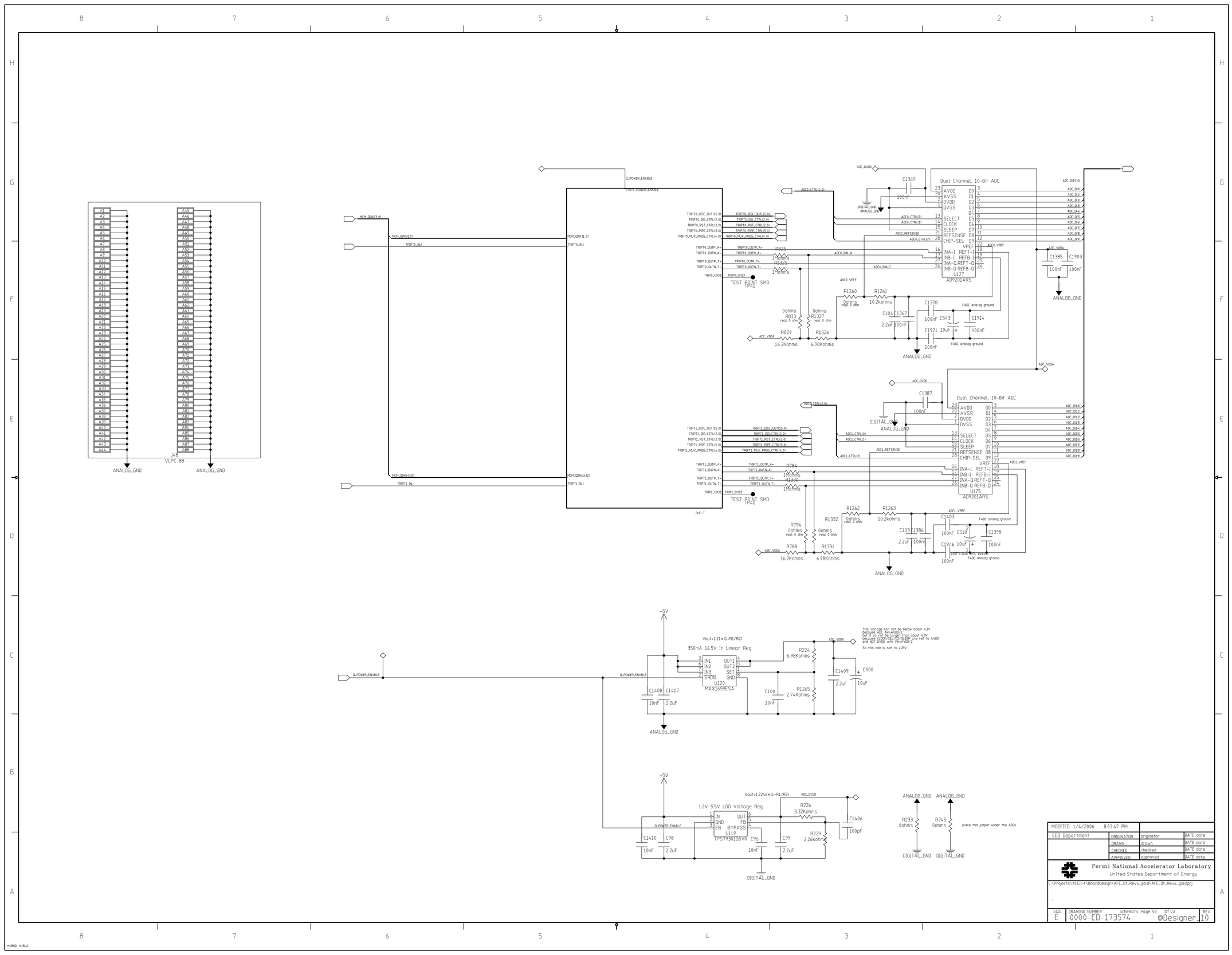
C:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H=8ND, V=4LA



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SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
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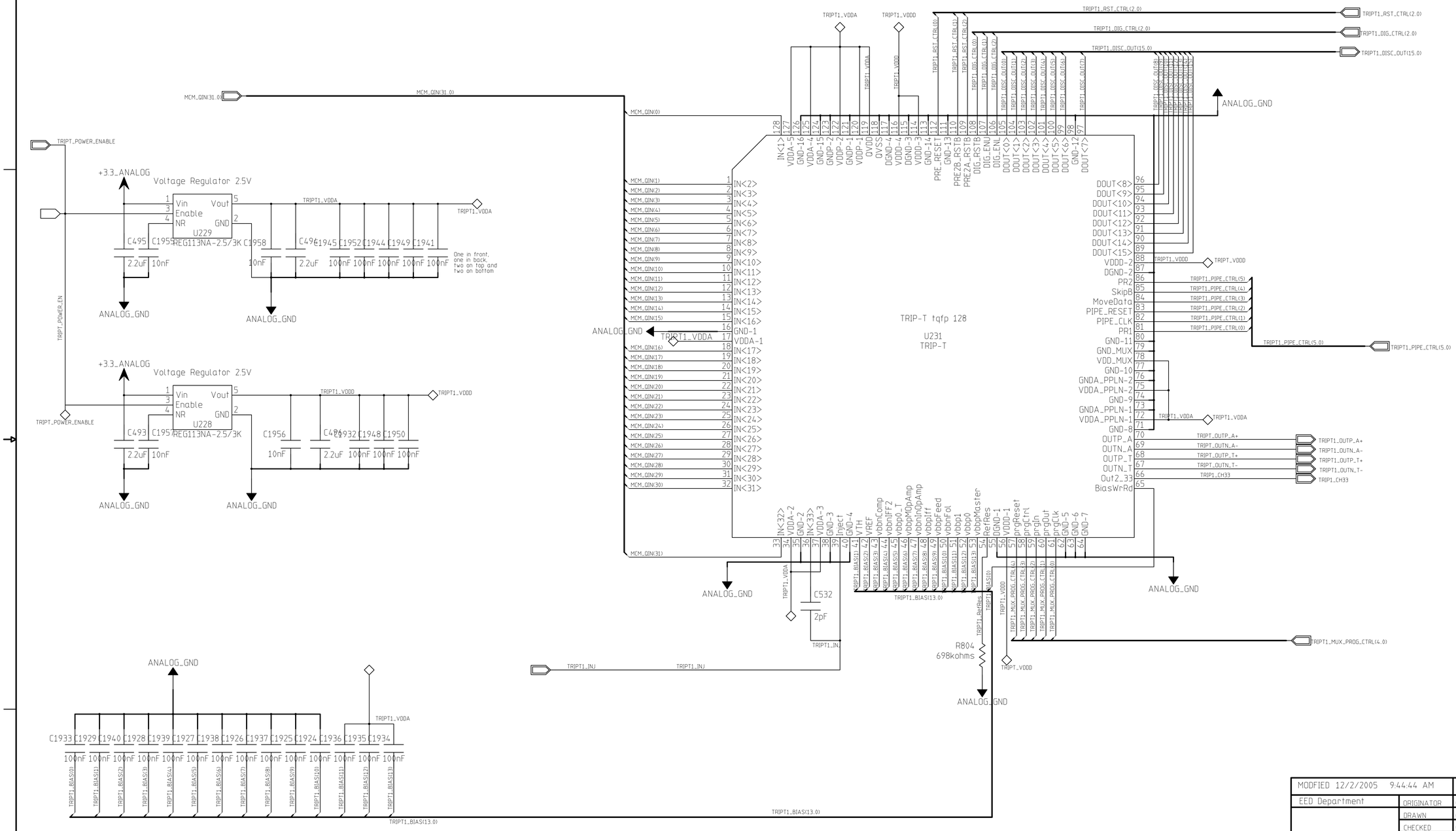
H=BND, V=BLA



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	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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SIZE	DRAWING NUMBER		REV
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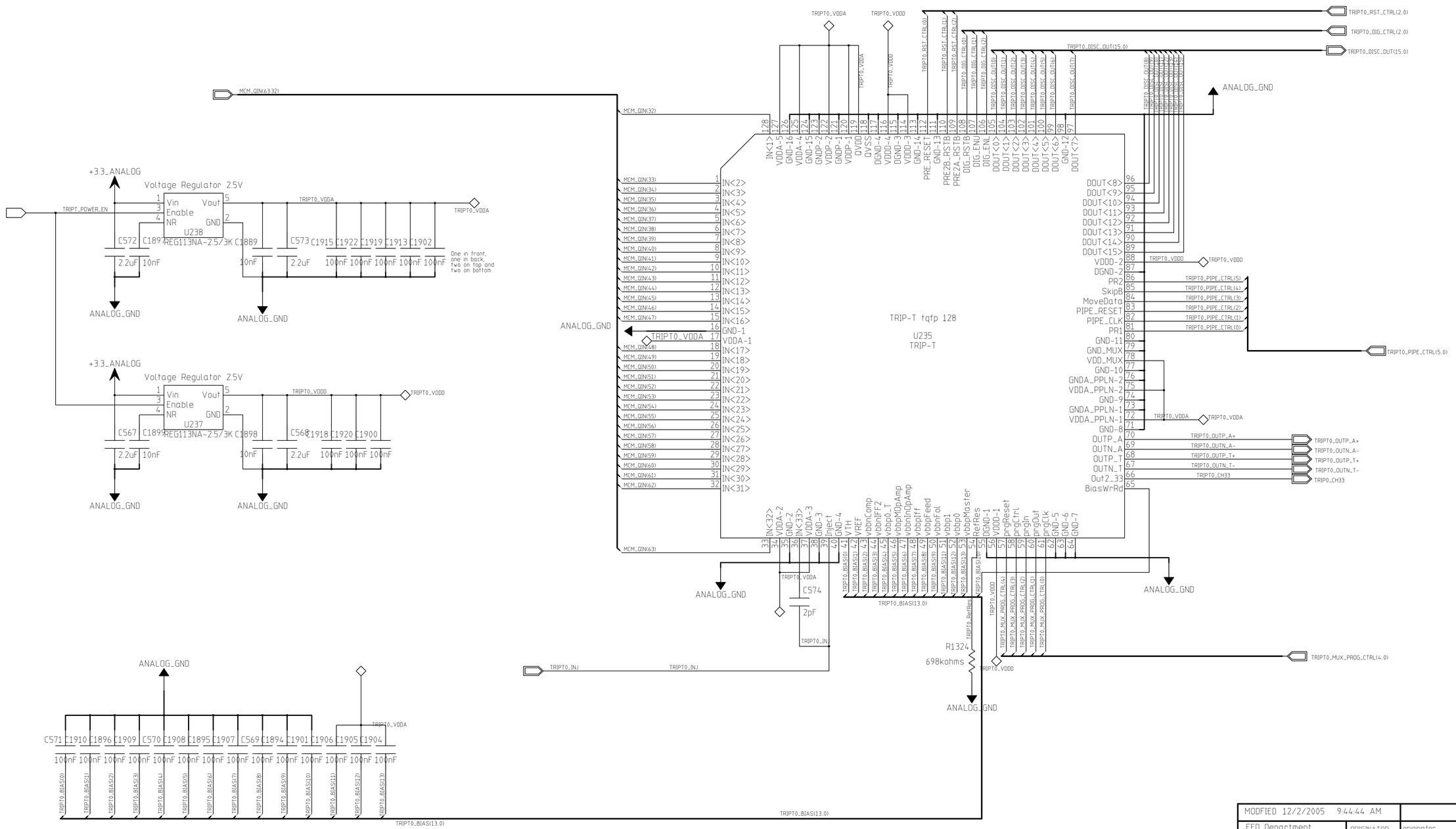

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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

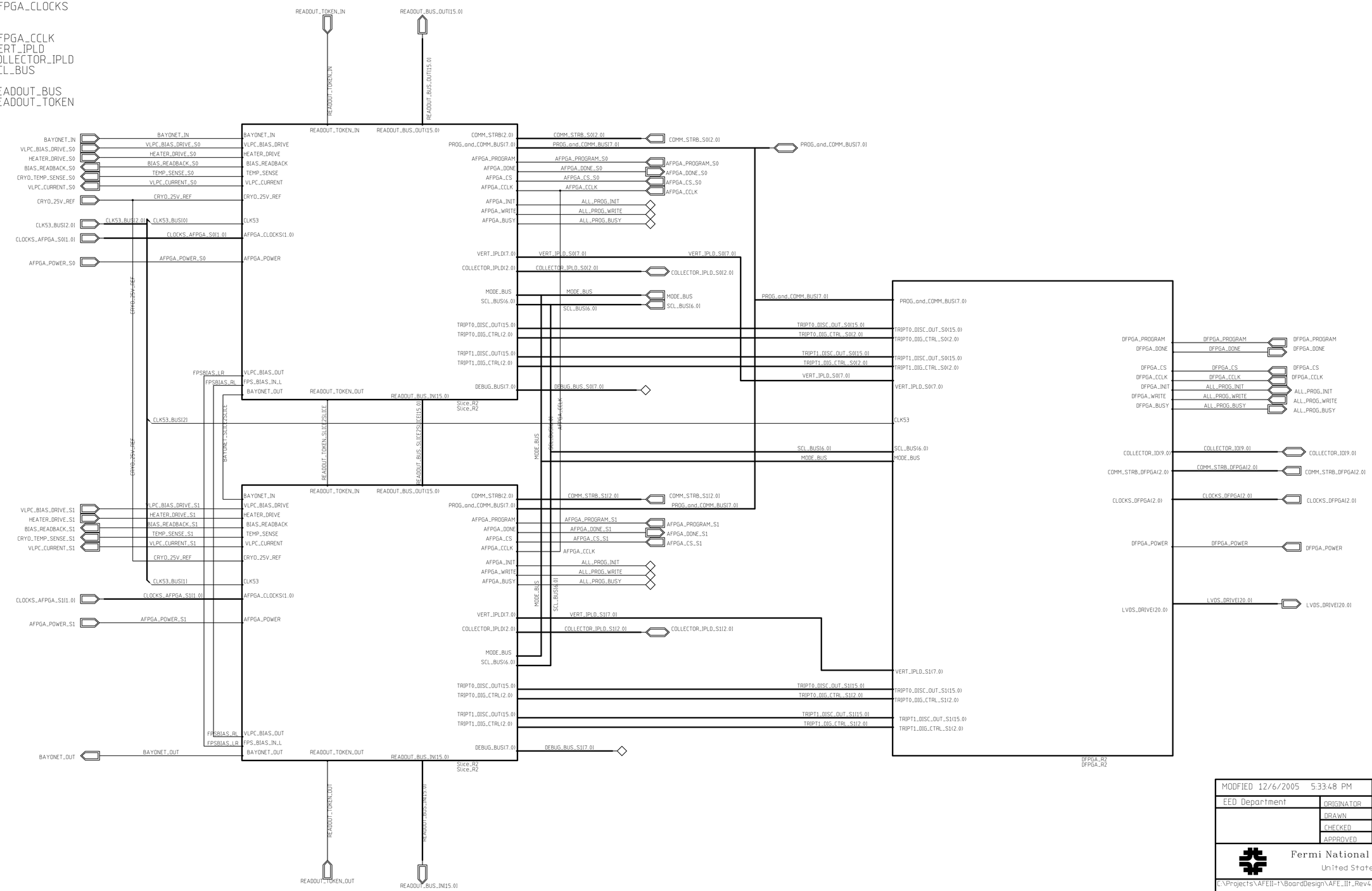
H=8ND, V=4LA

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



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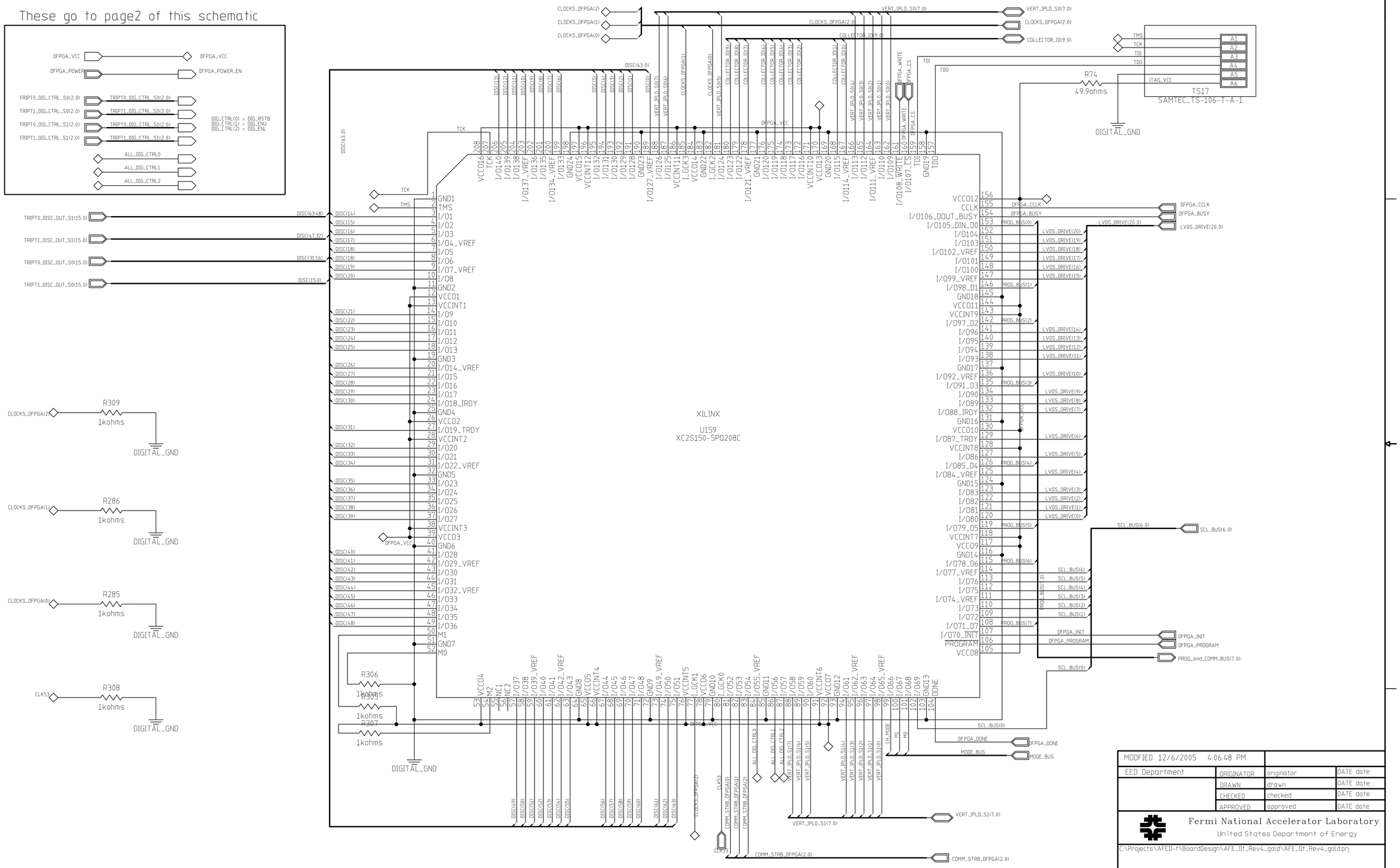
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	10

H=8ND, V=4LA



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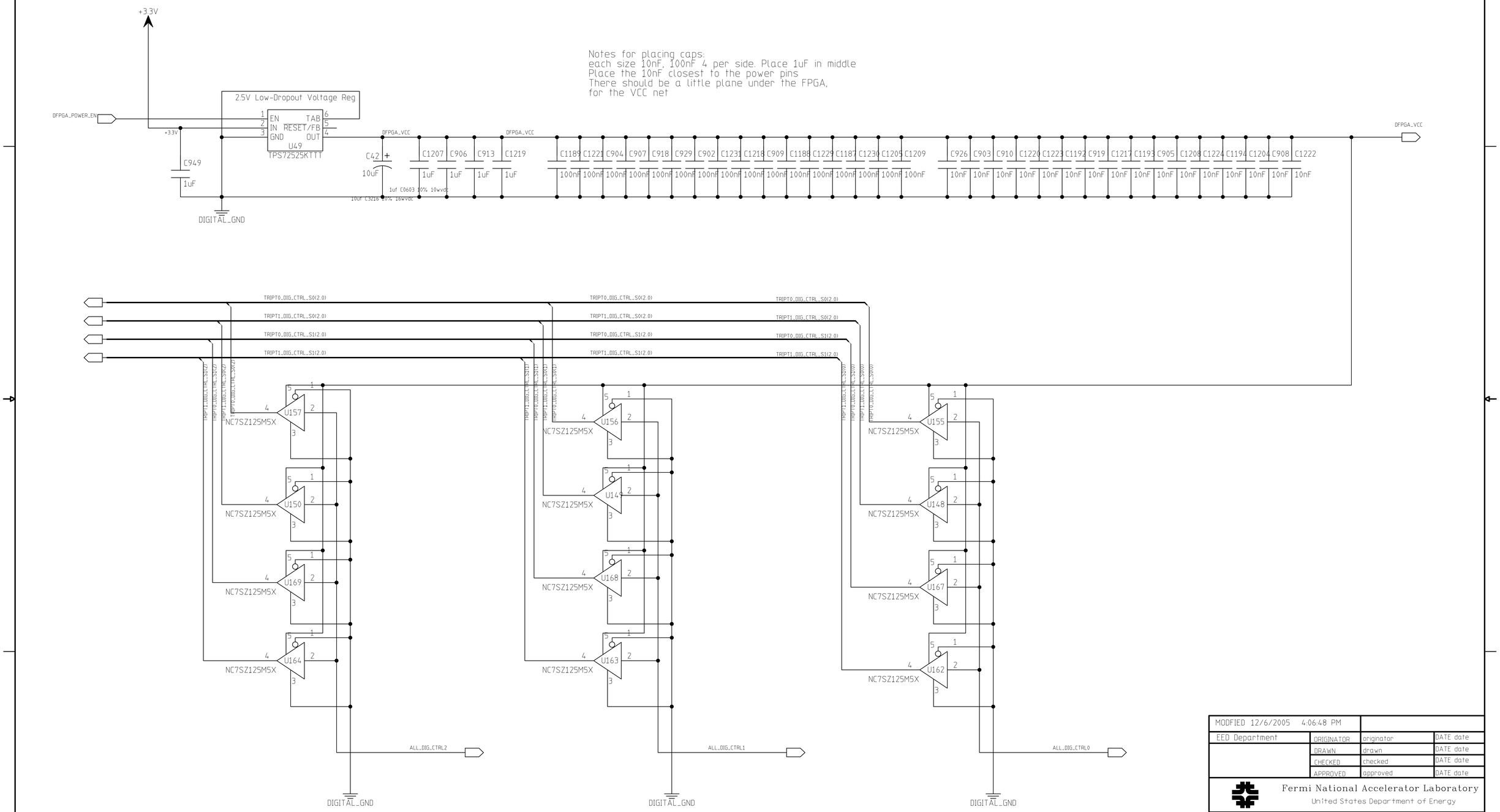
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer	10

H:8ND, V:4LA



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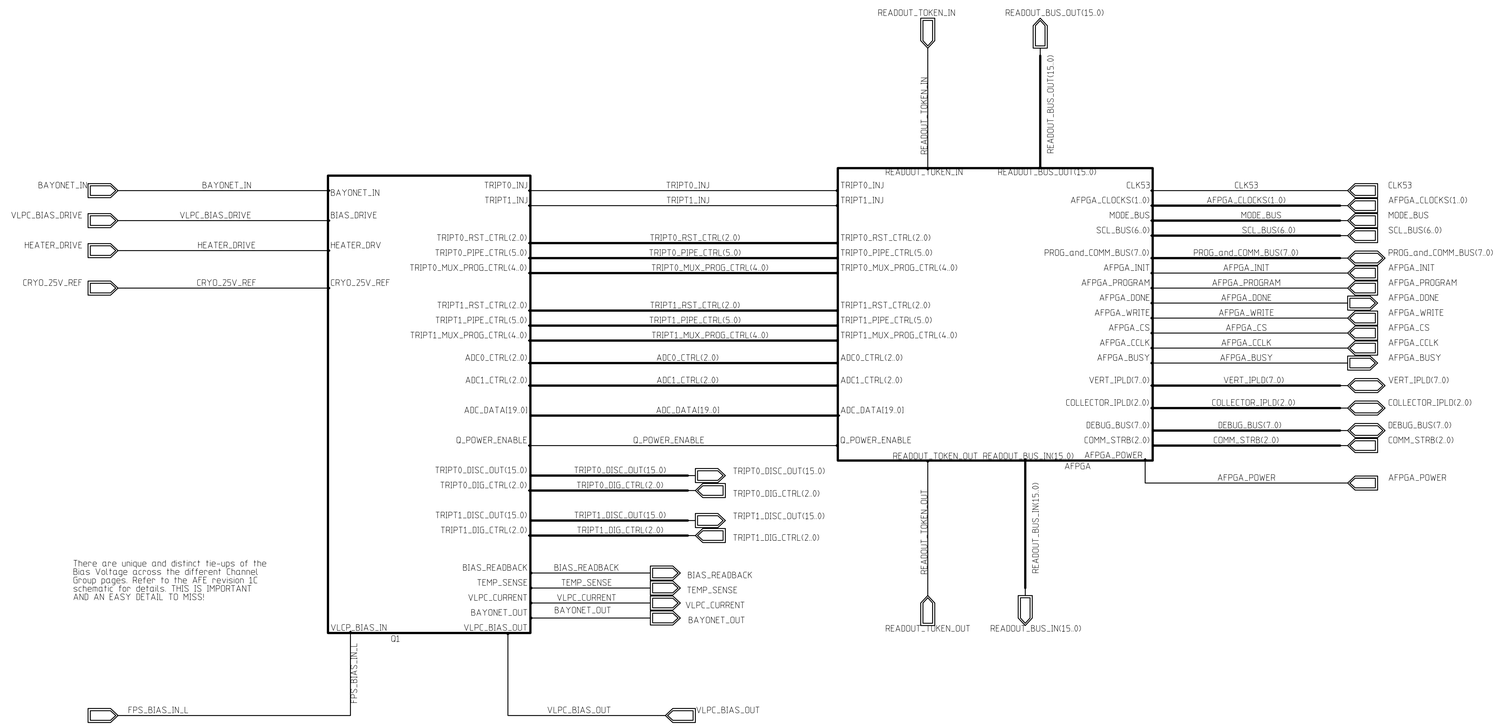
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer	10

H:8ND, V:4LA



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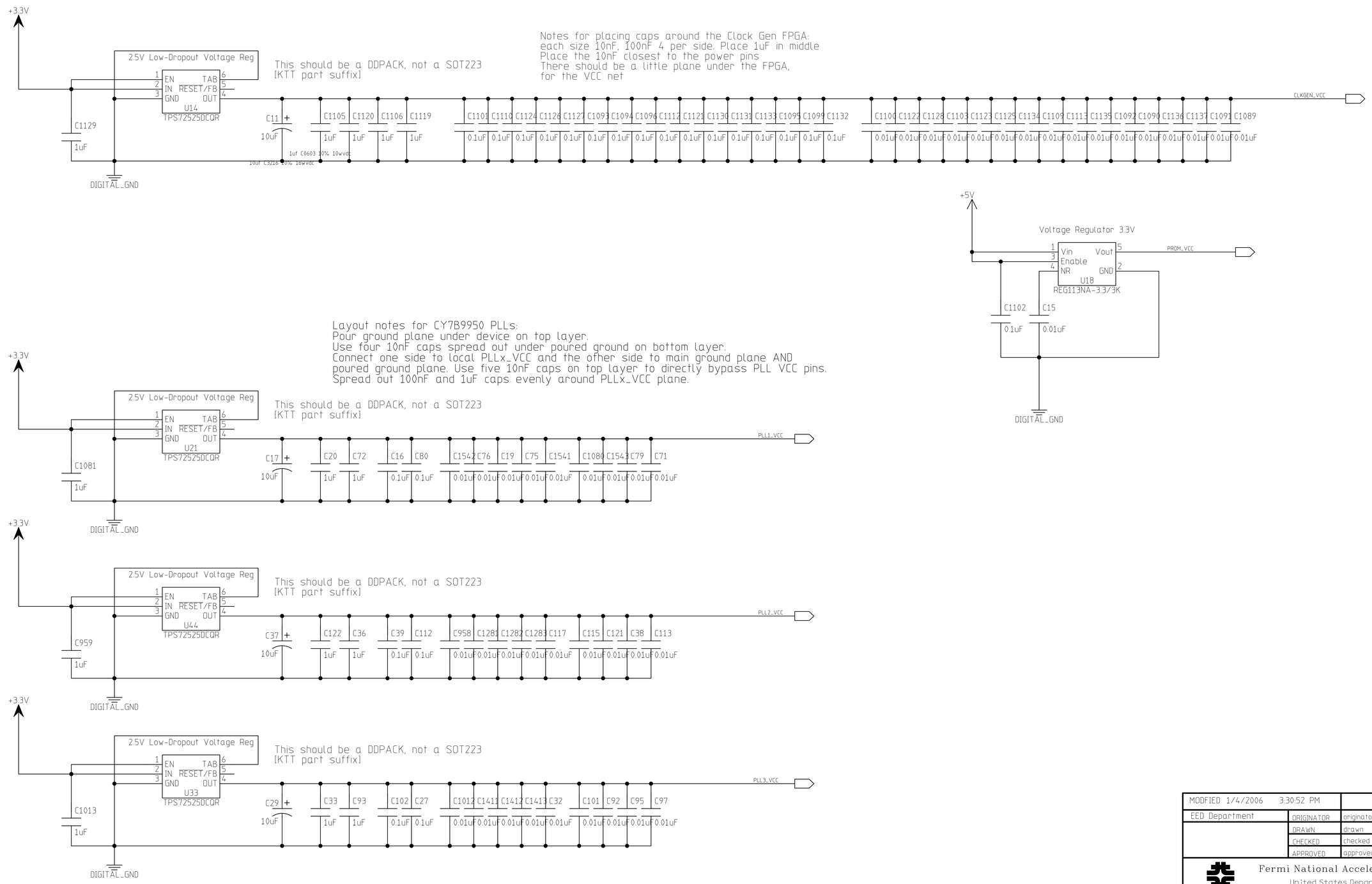
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H:8ND, V:4LA



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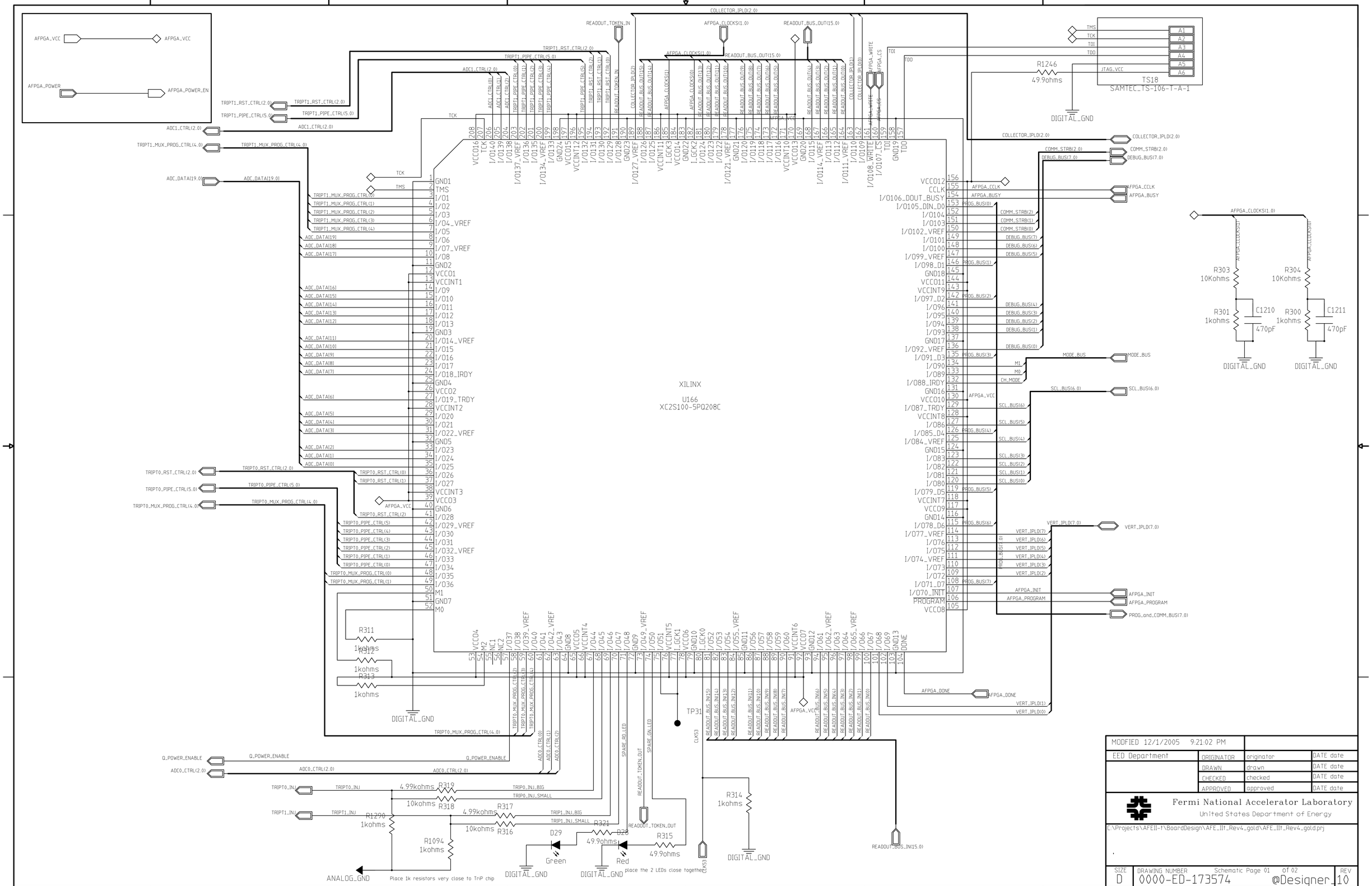
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 03 of 03 @Designer_10	

H=8ND, V=4LA


XILINX
U166
XC2S100-5PQ208C
SAMTEC_TS-106-T-A-1
TS18
R1246
49.9ohms
DIGITAL_GND
R303
10Kohms
R304
10Kohms
R301
1kohms
R300
1kohms
C1210
470pF
C1211
470pF
R311
1kohms
R312
1kohms
R313
1kohms
R319
4.99kohms
R318
10kohms
R317
4.99kohms
R316
10kohms
R321
49.9ohms
R315
49.9ohms
R314
1kohms
R1290
1kohms
R1094
1kohms
D29
Green
D28
Red
TP31
ANALOG_GND
Place 1k resistors very close to TriP chip
place the 2 LEDs close together
MODIFIED 12/1/2005 9:21:02 PM
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ORIGINATOR
DRAWN
CHECKED
APPROVED
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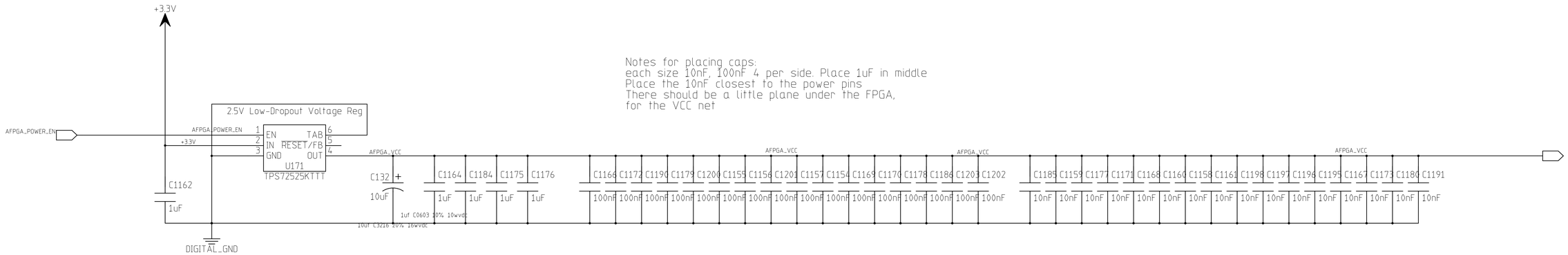
United States Department of Energy
C:\Projects\AFEII-1\BoardDesign\AFE_II_Rev4_gold\AFE_II_Rev4_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 02
@Designer
REV 10



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
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for the VCC net

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SIZE	DRAWING NUMBER		REV
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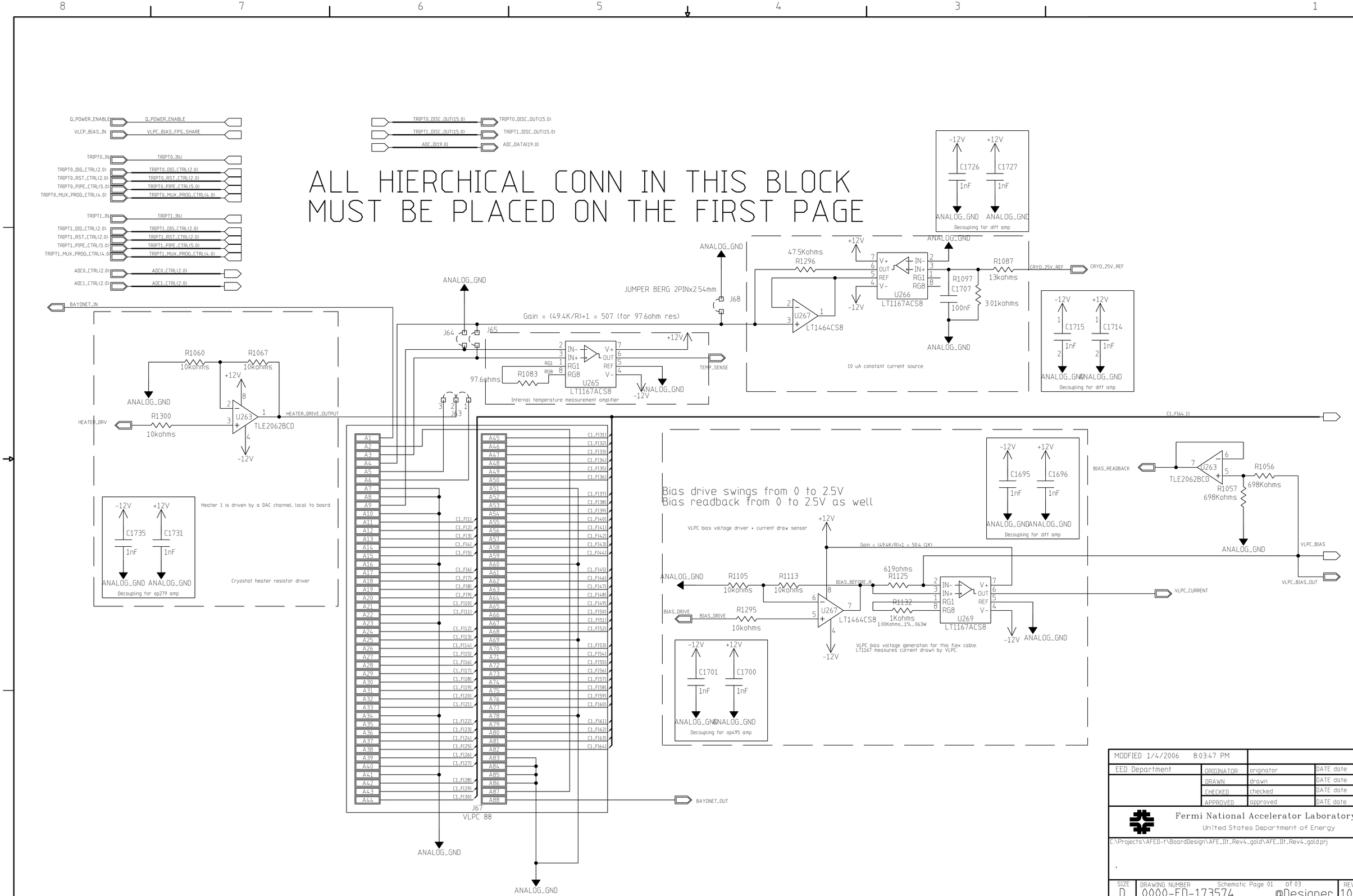
H=8ND, V=4LA


ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
TRIPT0_IN
TRIPT0_INJ
TRIPT1_IN
TRIPT1_INJ
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
BAYONET_IN
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
ANALOG_GND
JUMPER BERG 2PINx2.54mm
J68
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
J64
J65
J63
R1060
10kohms
R1067
10kohms
R1300
10kohms
HEATER_DRV
HEATER_DRIVE_OUTPUT
U263
TLE2062BCD
Heater 1 is driven by a DAC channel, local to board.
Cryostat heater resistor driver
C1735
C1731
1nF
Decoupling for op279 amp
97.6ohms
R1083
U265
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
47.5Kohms
R1296
U267
LT1464CS8
U266
LT1167ACS8
R1097
C1707
100nF
R1087
13kohms
3.01kohms
10 uA constant current source
CRYO_25V_REF
C1726
C1727
C1715
C1714
Decoupling for diff amp
C1_FI64_1
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R1105
10kohms
R1113
10kohms
R1295
10kohms
BIAS_DRIVE
BIAS_BEFORE_R
619ohms
R1125
R1132
1Kohms
1.00Kohms_1%_.063W
U269
LT1167ACS8
VLPC_CURRENT
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
C1701
C1700
Decoupling for op495 amp
C1695
C1696
BIAS_READBACK
R1056
698Kohms
R1057
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
J67
VLPC 88
BAYONET_OUT
MODIFIED 1/4/2006 8:03:47 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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C:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV 10
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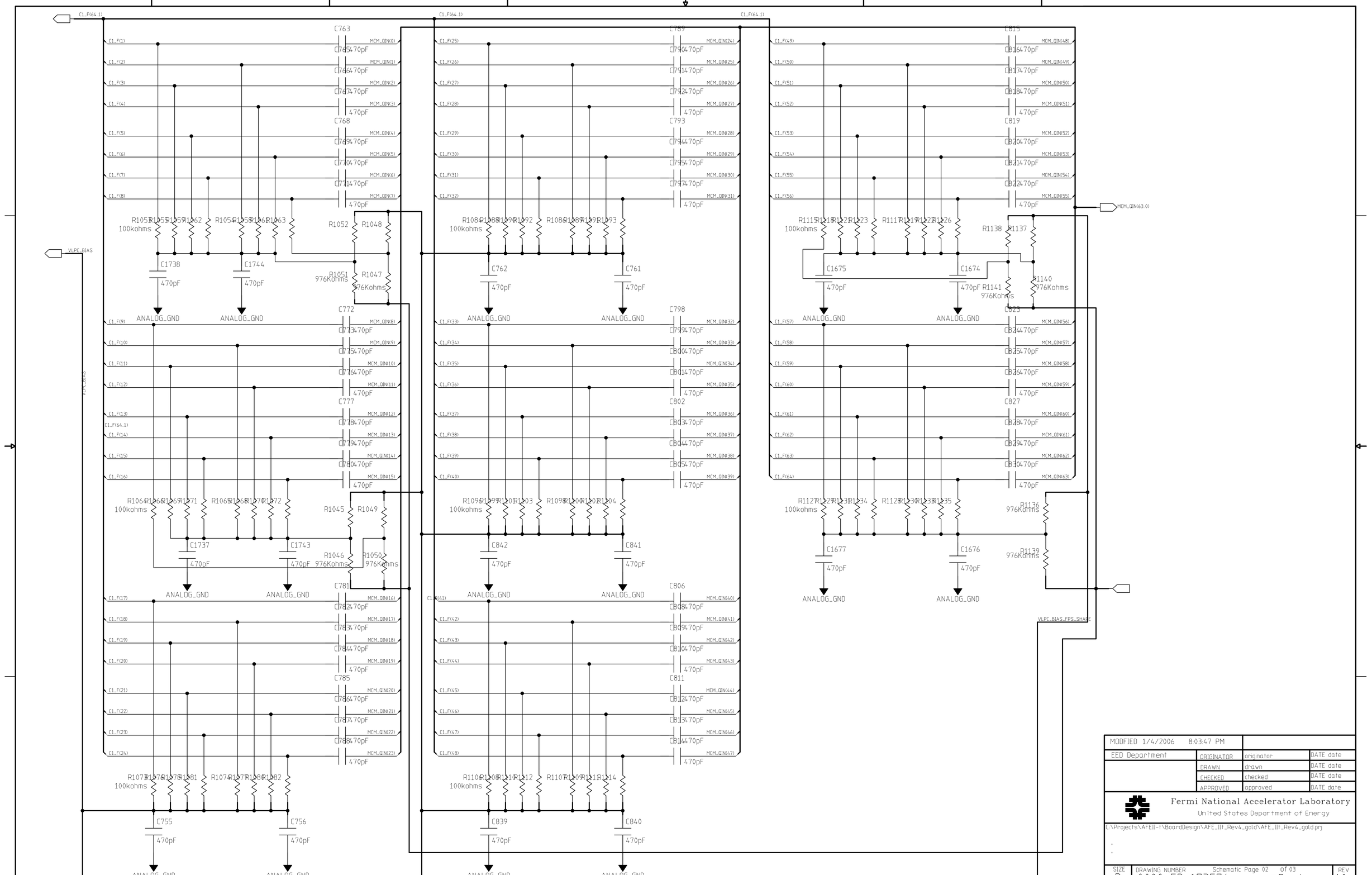
C1_F(64.1)
VLPC_BIAS
MCM_QIN(63.0)
VLPC_BIAS_FPS_SHARE
ANALOG_GND
100kohms
976Kohms
470pF
MODFIED 1/4/2006 8:03:47 PM
EED Department
ORIGINATOR originator DATE date
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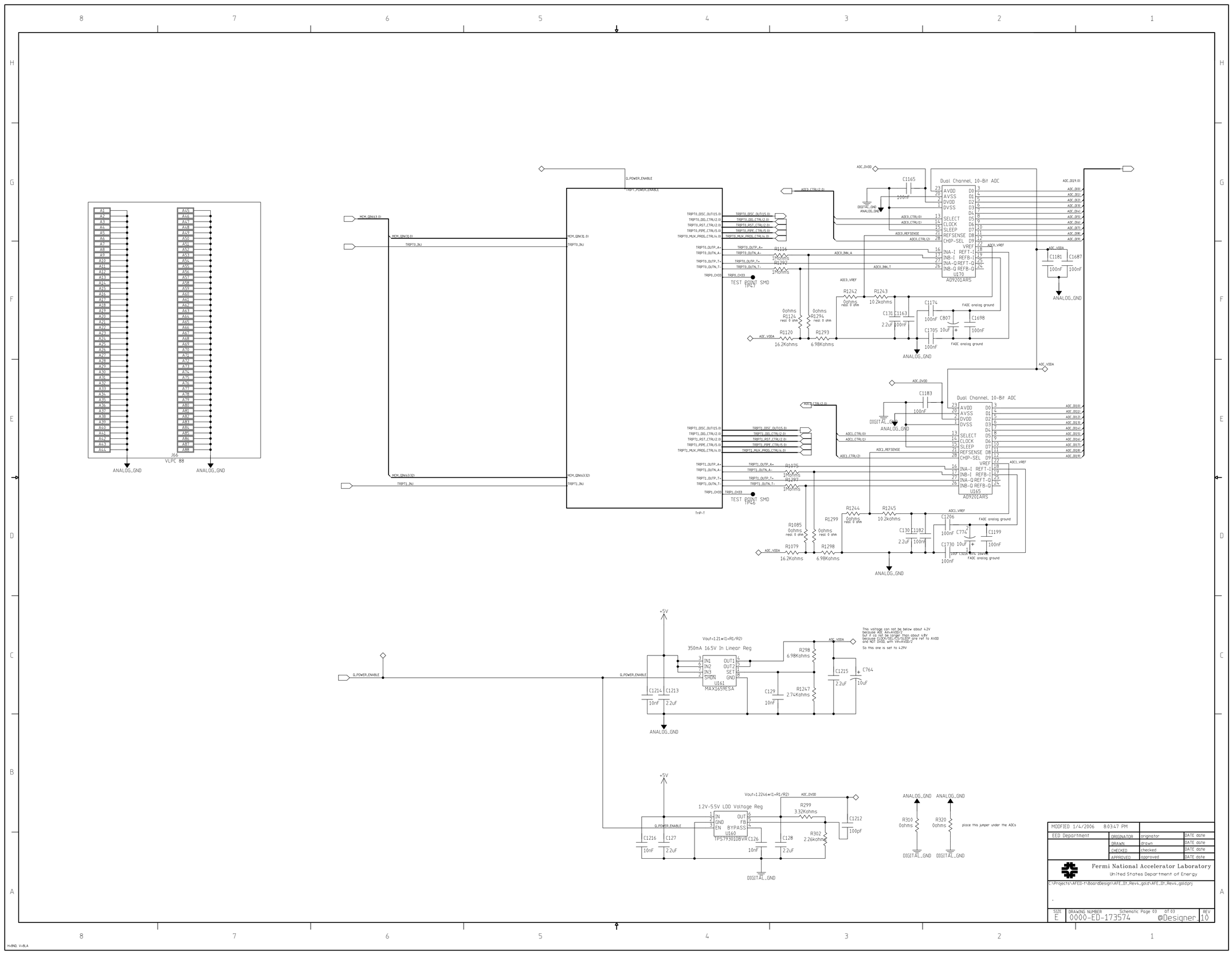
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 02 of 03
@Designer_10
REV
H:8ND, V:4LA



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SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
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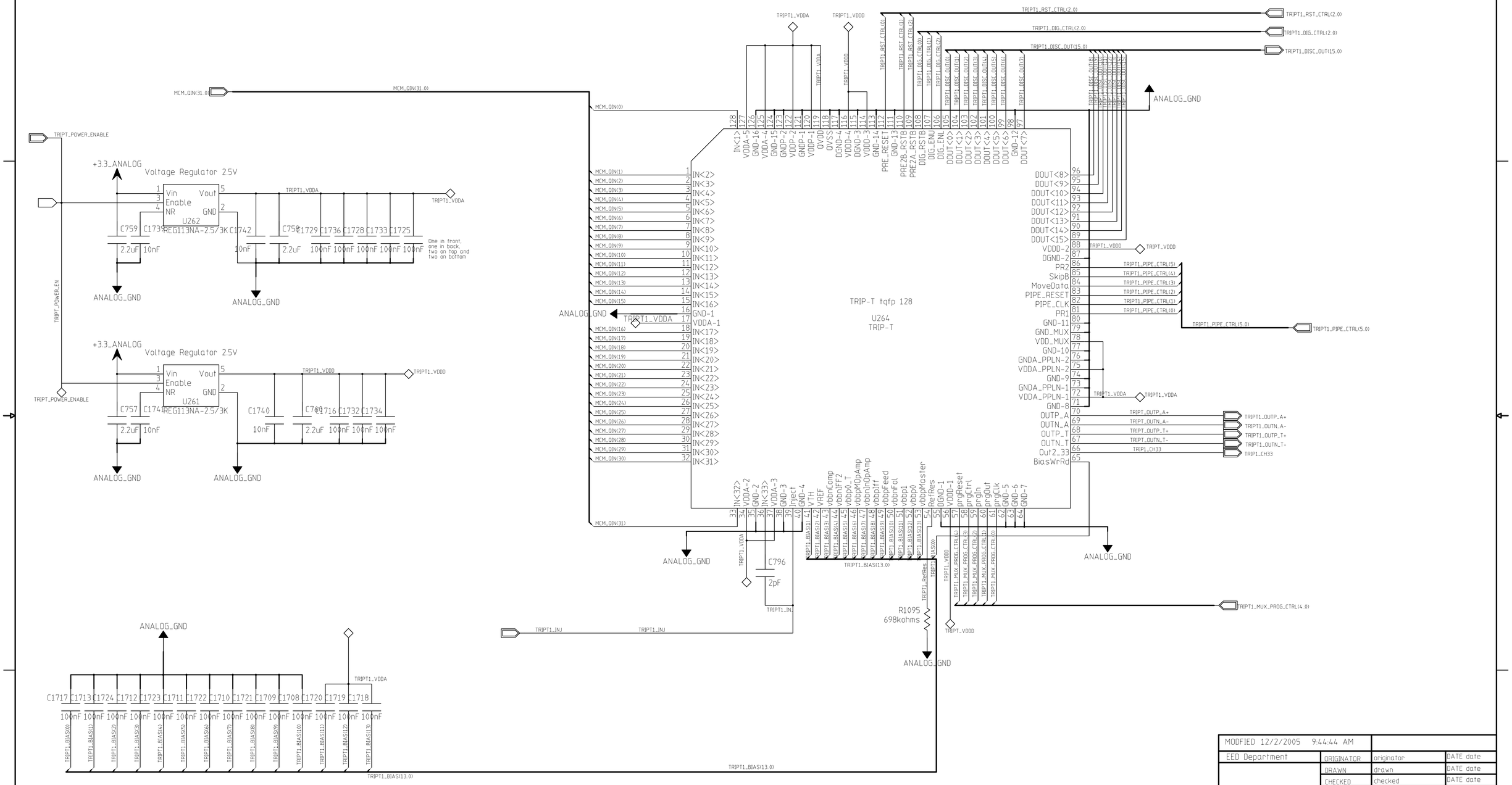
H=BND, V=BLA



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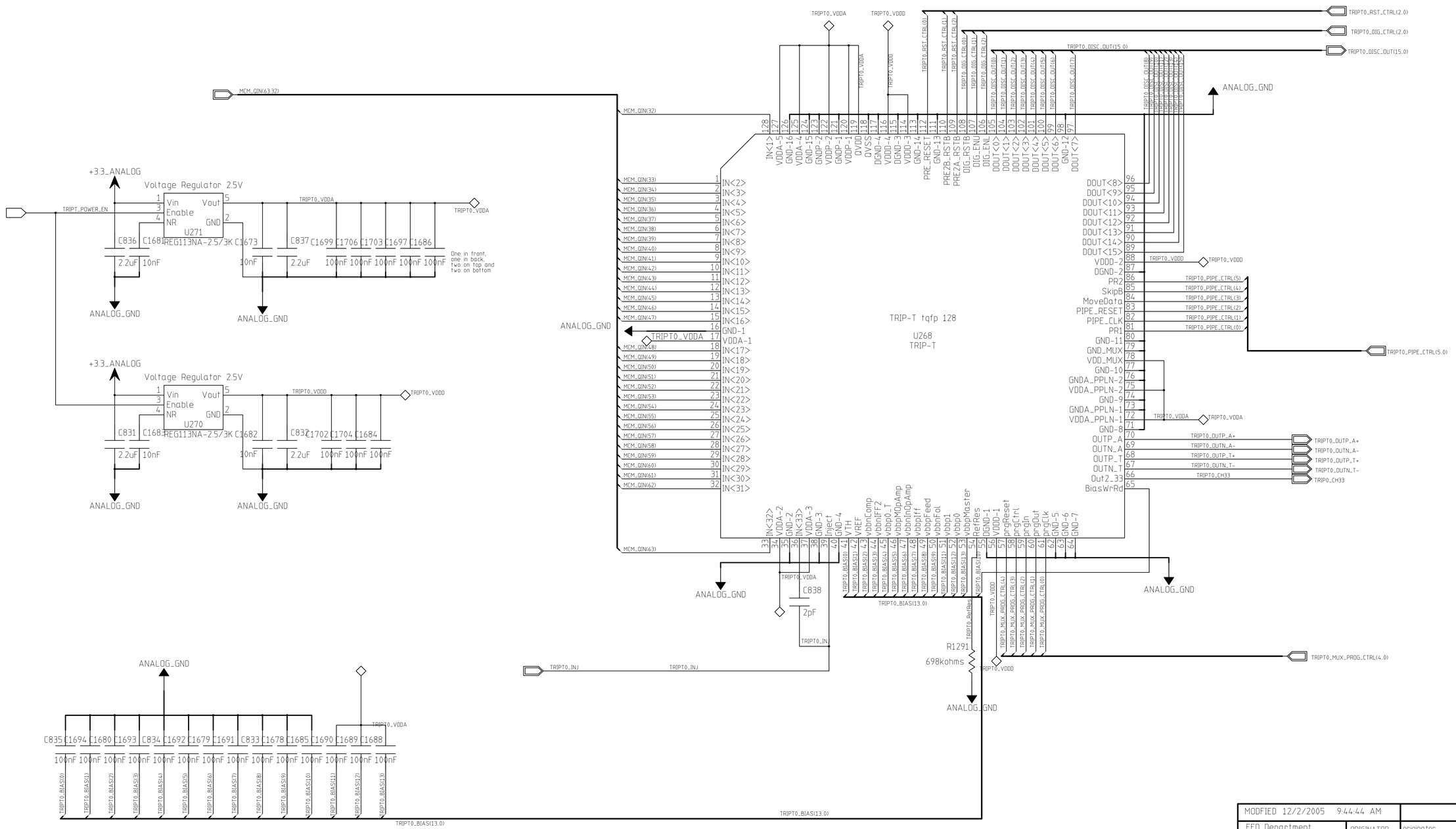
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



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SIZE	DRAWING NUMBER		REV
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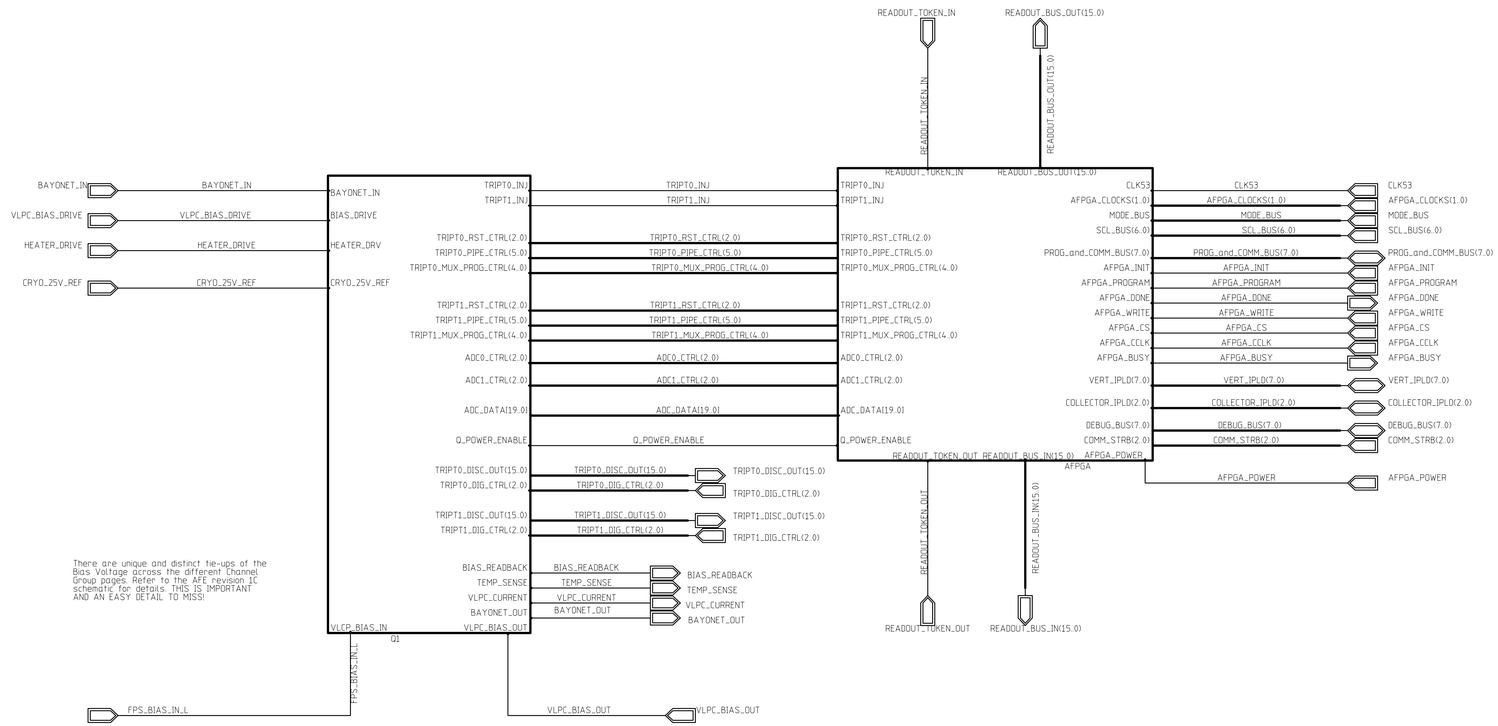

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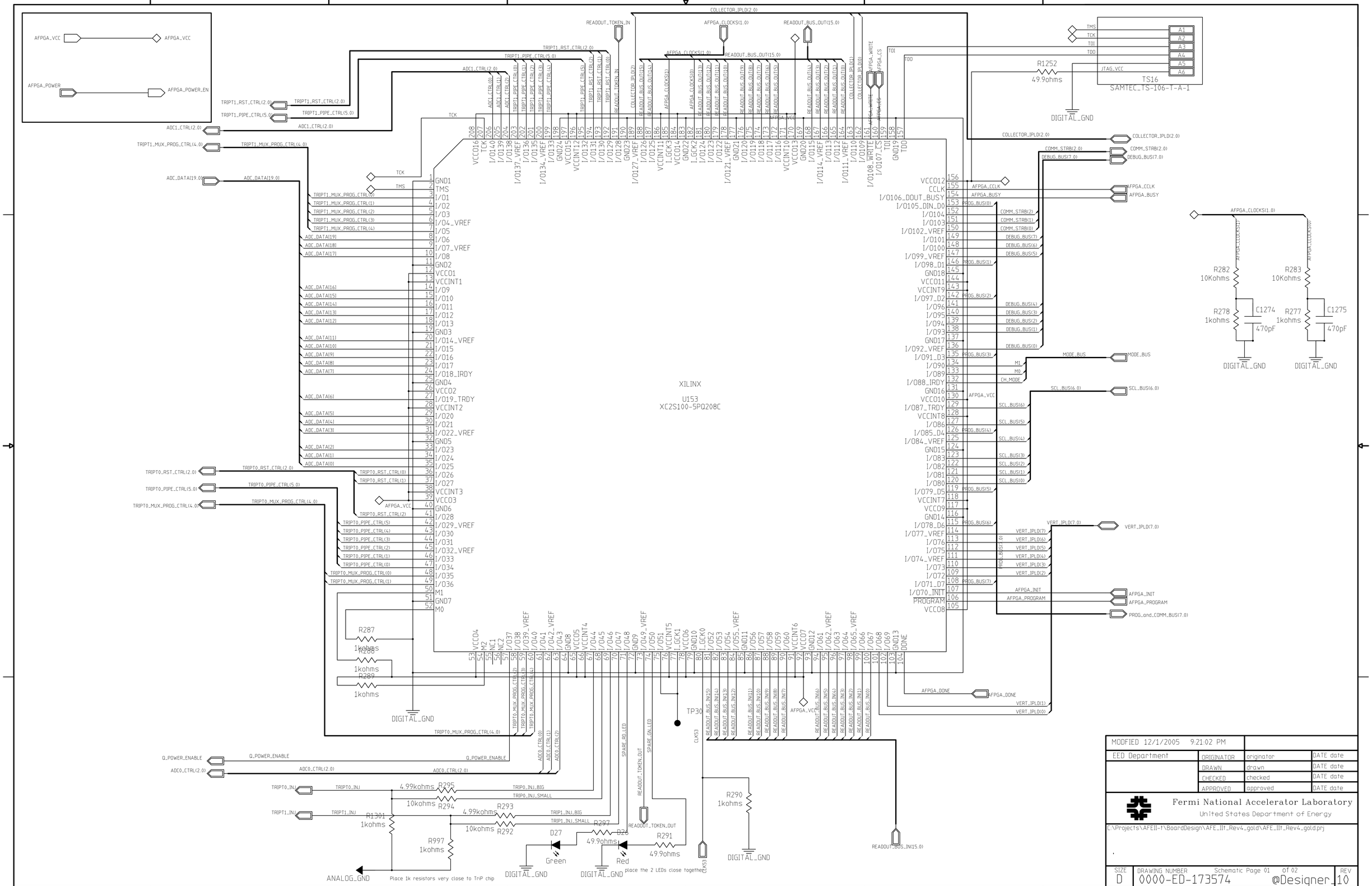
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H:8ND, V:4LA



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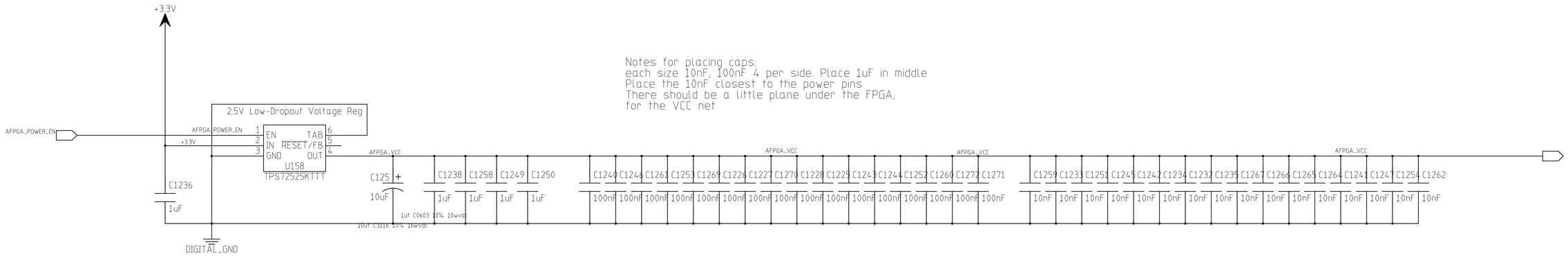
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer	10

H=8ND, V=4LA



Notes for placing caps:
each size 10nF, 100nF 4 per side. Place 1uF in middle
Place the 10nF closest to the power pins
There should be a little plane under the FPGA,
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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

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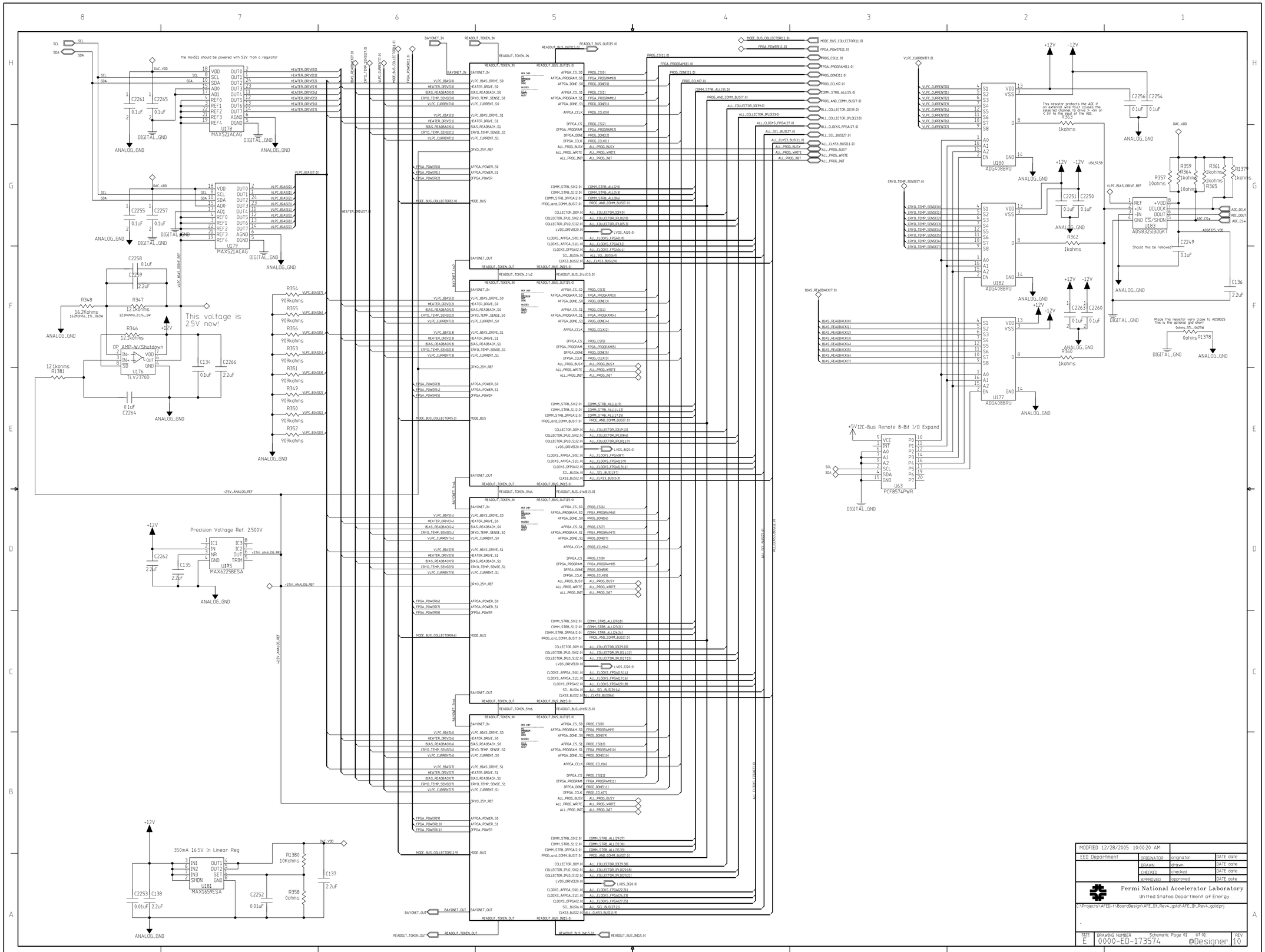
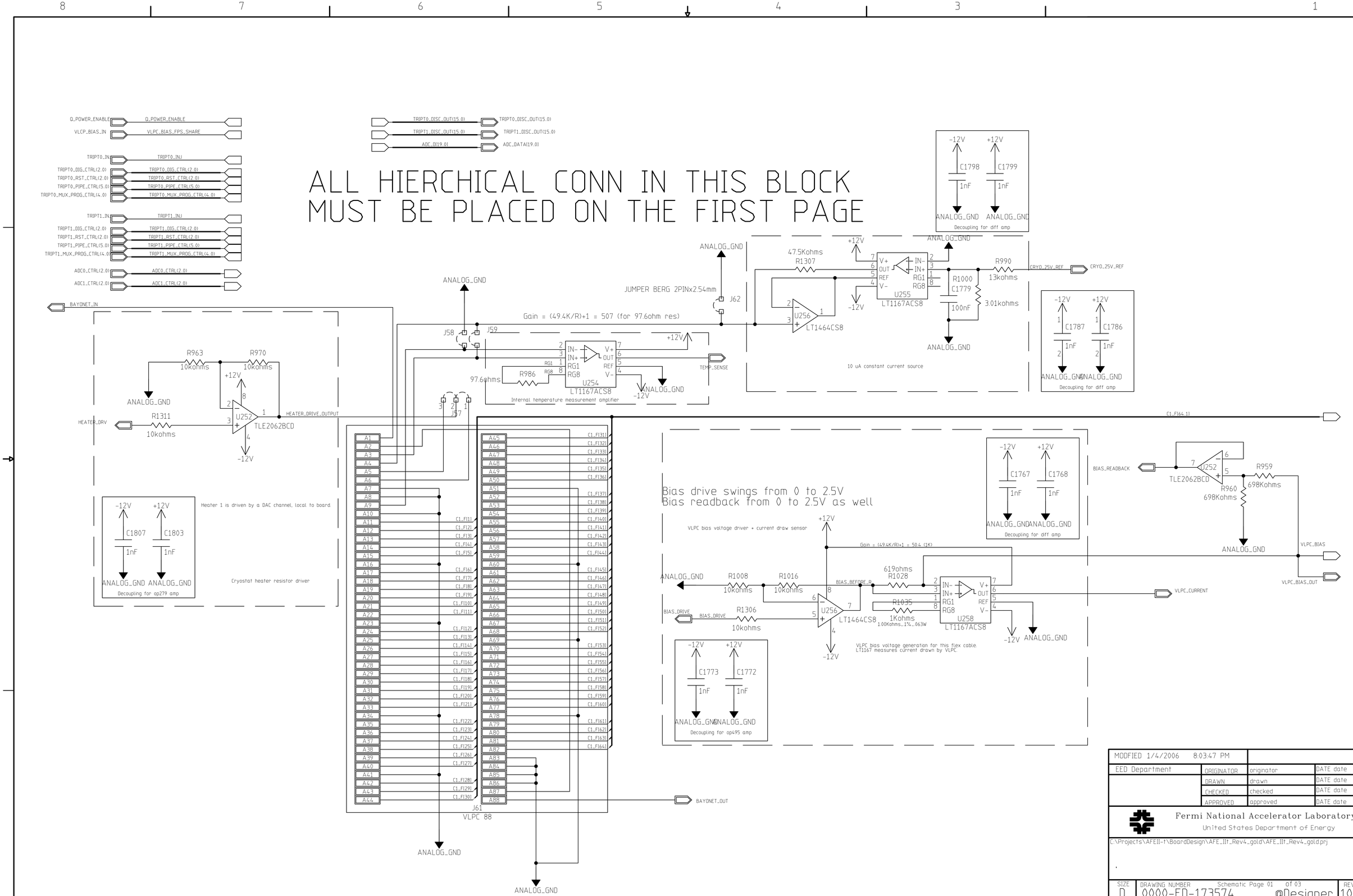

the max521 should be powered with 52V from a regulator
U178 MAX521ACAG
U179 MAX521ACAG
This voltage is 2.5V now!
U176 TLV2370D
OP_AMP-W/Shutdown
Precision Voltage Ref. 2.500V
U175 MAX6225BESA
350mA 16.5V In Linear Reg
U181 MAX1659ESA
This resistor protects the ADC if an external wire fault causes the selected channel to drive >-5V or < 0V to the input of the ADC
U180 ADG408BRU
U182 ADG408BRU
U177 ADG408BRU
+5V I2C-Bus Remote 8-Bit I/O Expand
U63 PCF8574PWR
U183 ADS8325IBDGK
Should this be removed?
Place this resistor very close to ADS8325
This is the optional gnd short
MODIFIED 12/28/2005 10:00:20 AM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Projects\AFEII-1\BoardDesign\AFE_III_Rev4_gold\AFE_III_Rev4_gold.prj
SIZE E
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 01
REV
@Designer_10


ALL HIERCHICAL CONN IN THIS BLOCK
MUST BE PLACED ON THE FIRST PAGE
Q_POWER_ENABLE
VLCP_BIAS_IN
VLCP_BIAS_FPS_SHARE
TRIPT0_IN
TRIPT0_INJ
TRIPT0_DIG_CTRL(2.0)
TRIPT0_RST_CTRL(2.0)
TRIPT0_PIPE_CTRL(5.0)
TRIPT0_MUX_PROG_CTRL(4.0)
TRIPT1_IN
TRIPT1_INJ
TRIPT1_DIG_CTRL(2.0)
TRIPT1_RST_CTRL(2.0)
TRIPT1_PIPE_CTRL(5.0)
TRIPT1_MUX_PROG_CTRL(4.0)
ADC0_CTRL(2.0)
ADC1_CTRL(2.0)
TRIPT0_DISC_OUT(15.0)
TRIPT1_DISC_OUT(15.0)
ADC_DI(19.0)
ADC_DATA(19.0)
BAYONET_IN
ANALOG_GND
JUMPER BERG 2PINx2.54mm
J62
Gain = (49.4K/R)+1 = 507 (for 97.6ohm res)
J58
J59
R963
10kohms
R970
10kohms
HEATER_DRV
R1311
10kohms
U252
TLE2062BCD
HEATER_DRIVE_OUTPUT
97.6ohms
R986
U254
LT1167ACS8
Internal temperature measurement amplifier
TEMP_SENSE
J57
Heater 1 is driven by a DAC channel, local to board.
C1807
C1803
1nF
Decoupling for op279 amp
Cryostat heater resistor driver
J61
VLPC 88
BAYONET_OUT
47.5Kohms
R1307
U256
LT1464CS8
U255
LT1167ACS8
R1000
C1779
100nF
R990
13kohms
3.01kohms
10 uA constant current source
C1798
C1799
Decoupling for diff amp
CRYO_25V_REF
C1787
C1786
C1_FI64_1
Bias drive swings from 0 to 2.5V
Bias readback from 0 to 2.5V as well
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 50.4 (1K)
R1008
10kohms
R1016
10kohms
BIAS_BEFORE_R
619ohms
R1028
R1035
1Kohms
1.00Kohms_1%_.063W
U258
LT1167ACS8
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
BIAS_DRIVE
R1306
10kohms
C1773
C1772
Decoupling for op495 amp
C1767
C1768
BIAS_READBACK
R959
698Kohms
R960
698Kohms
VLPC_BIAS
VLPC_BIAS_OUT
VLPC_CURRENT
MODIFIED 1/4/2006 8:03:47 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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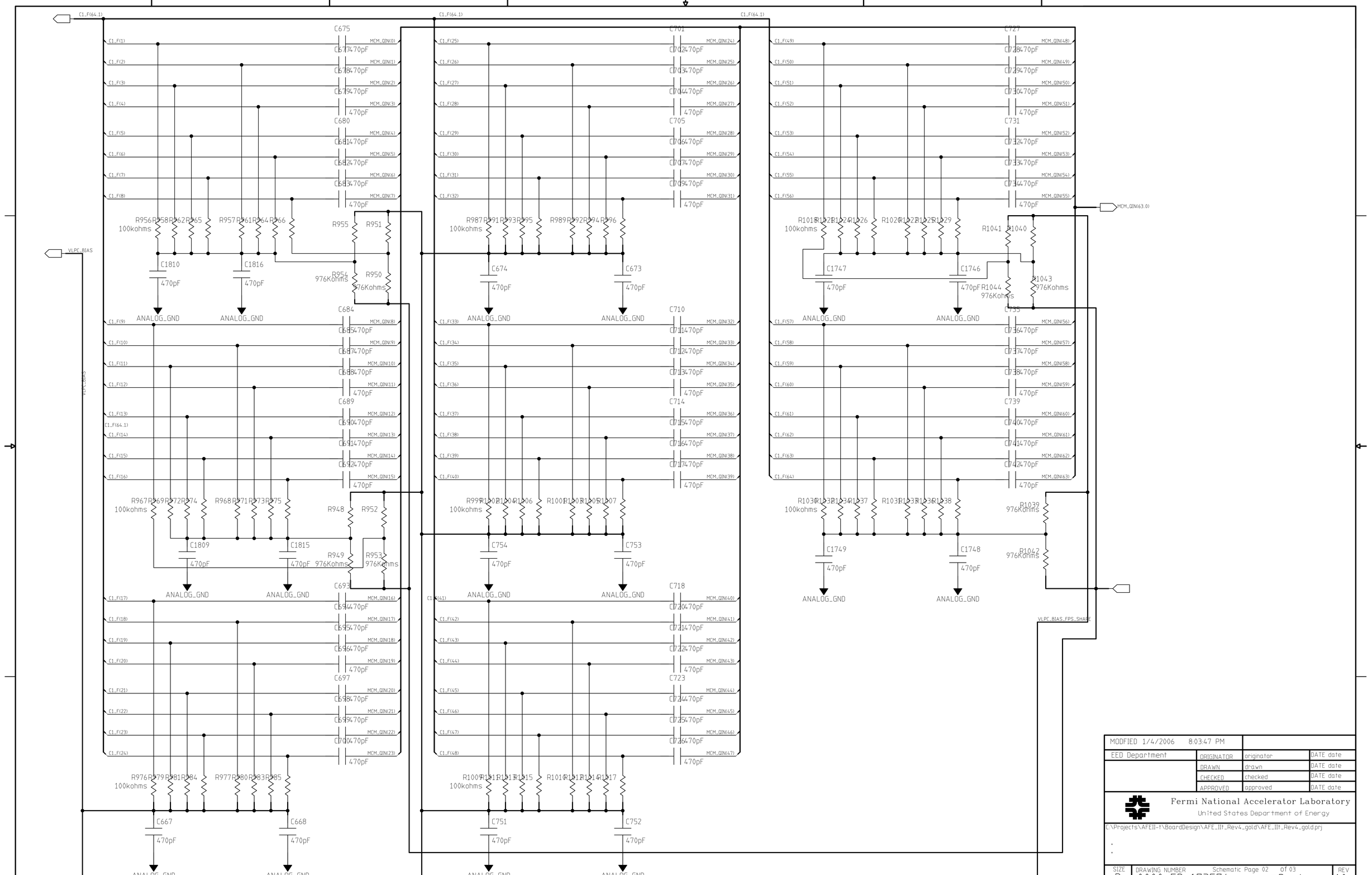
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 03
@Designer_1
REV 10
H=8ND; V=4LA



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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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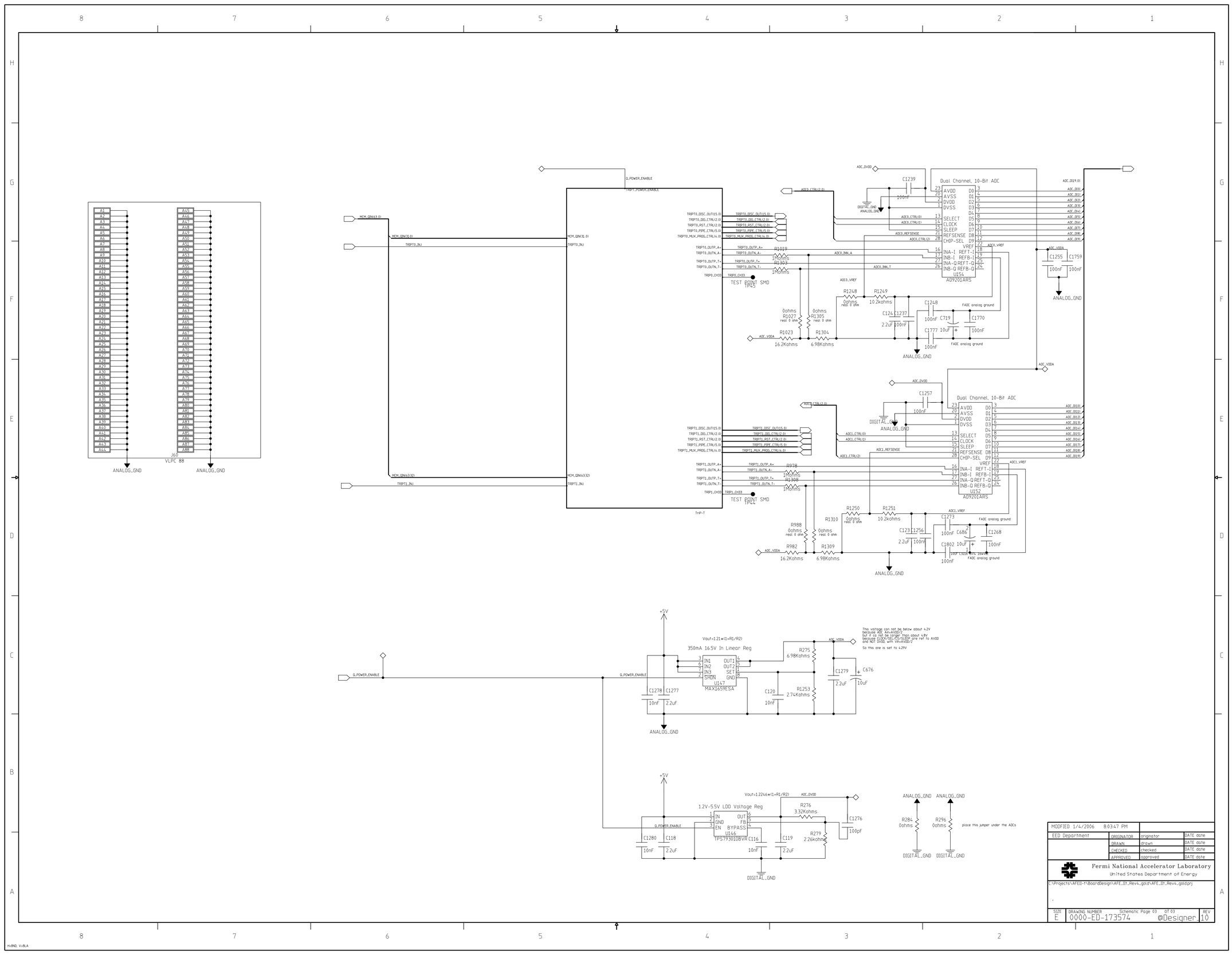
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H:8ND, V:4LA



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	APPROVED	approved	DATE date

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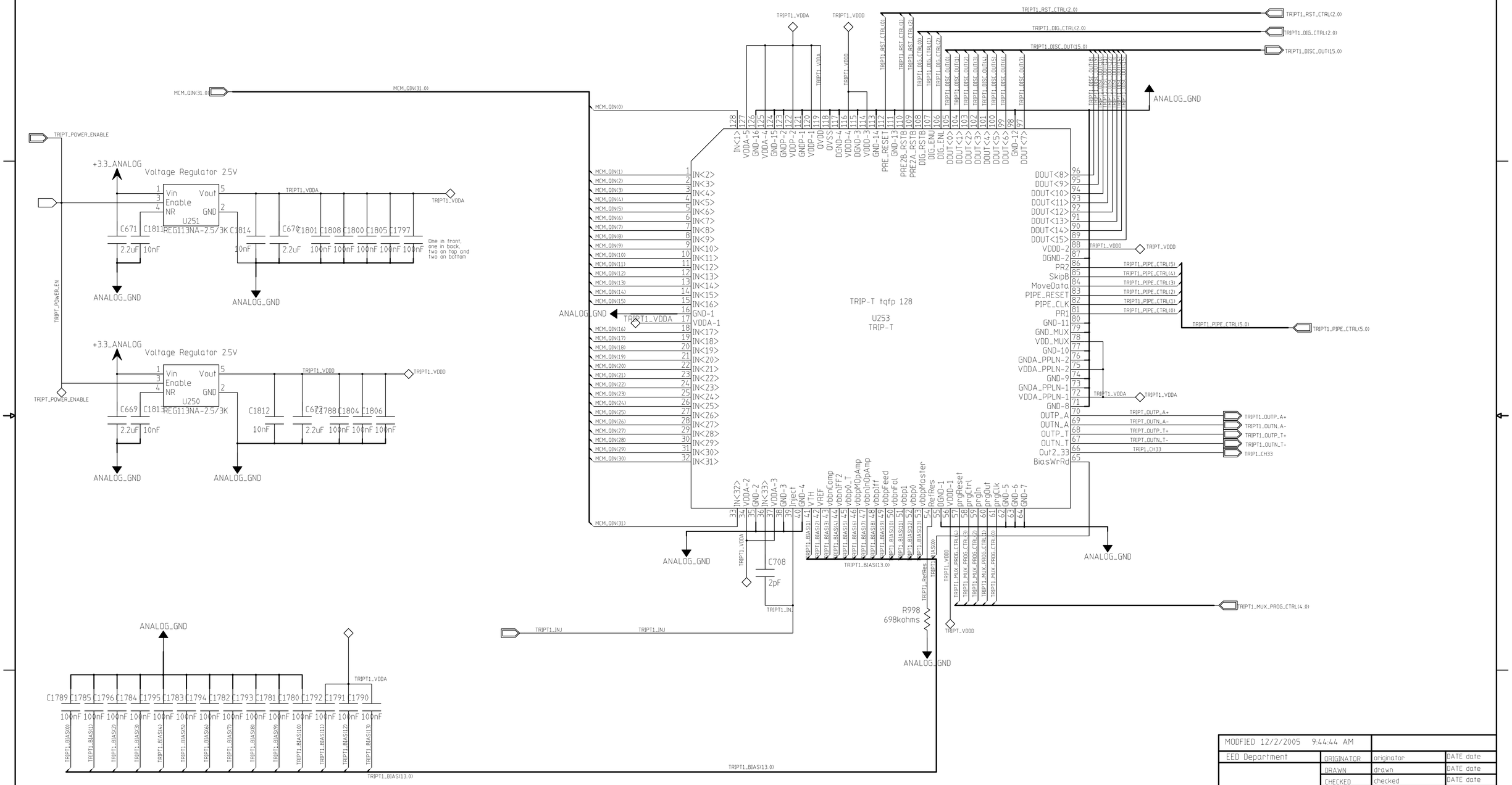
C:\Projects\AFEII-1\BoardDesign\AFE_II1_Rev4_gold\AFE_II1_Rev4_gold.prj

SIZE	DRAWING NUMBER	Schematic Page 03 of 03	REV
E	0000-ED-173574	@Designer	10

H=BND, V=BLA



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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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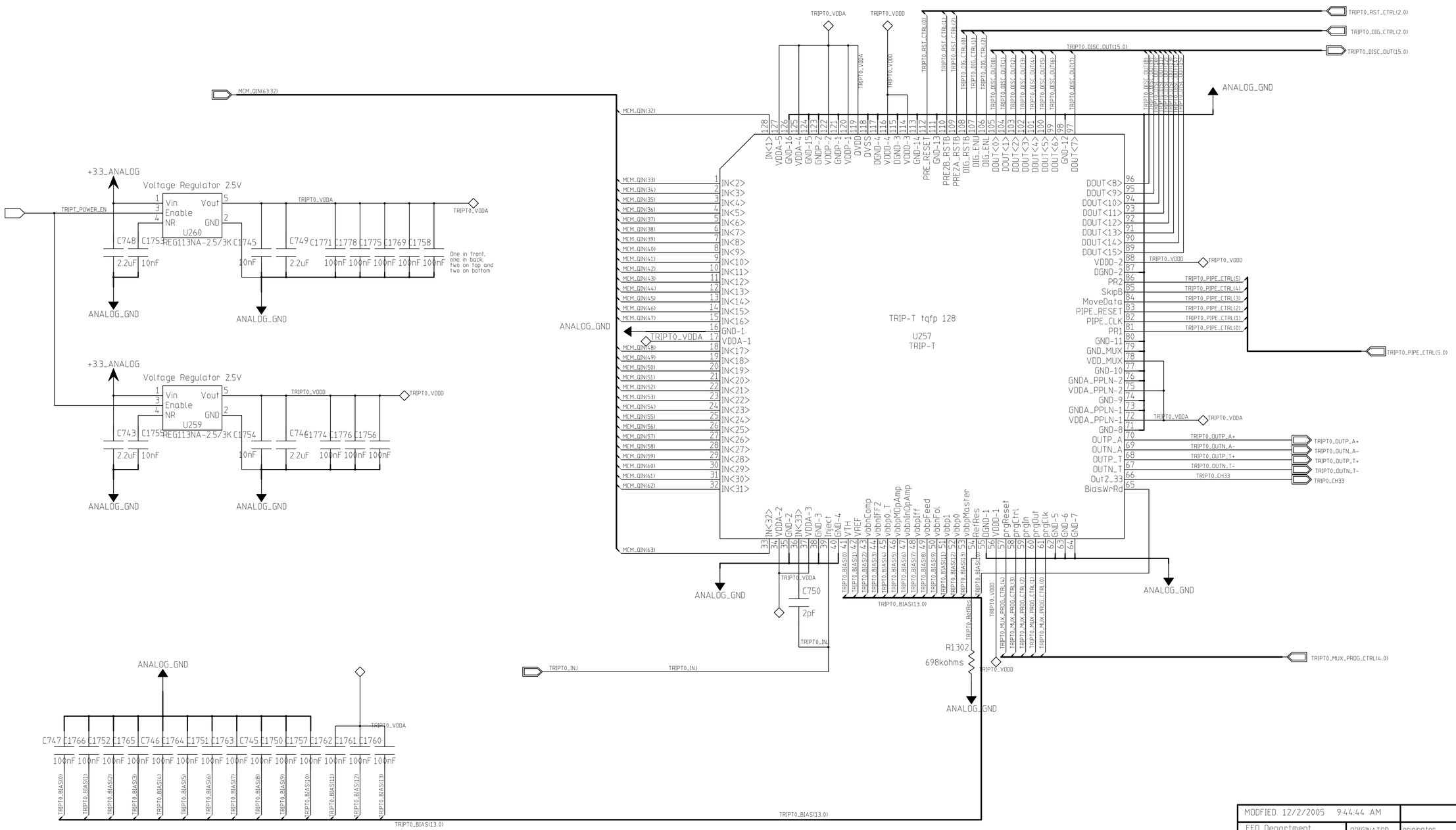
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 02 @Designer_10	

H=8ND, V=4LA



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	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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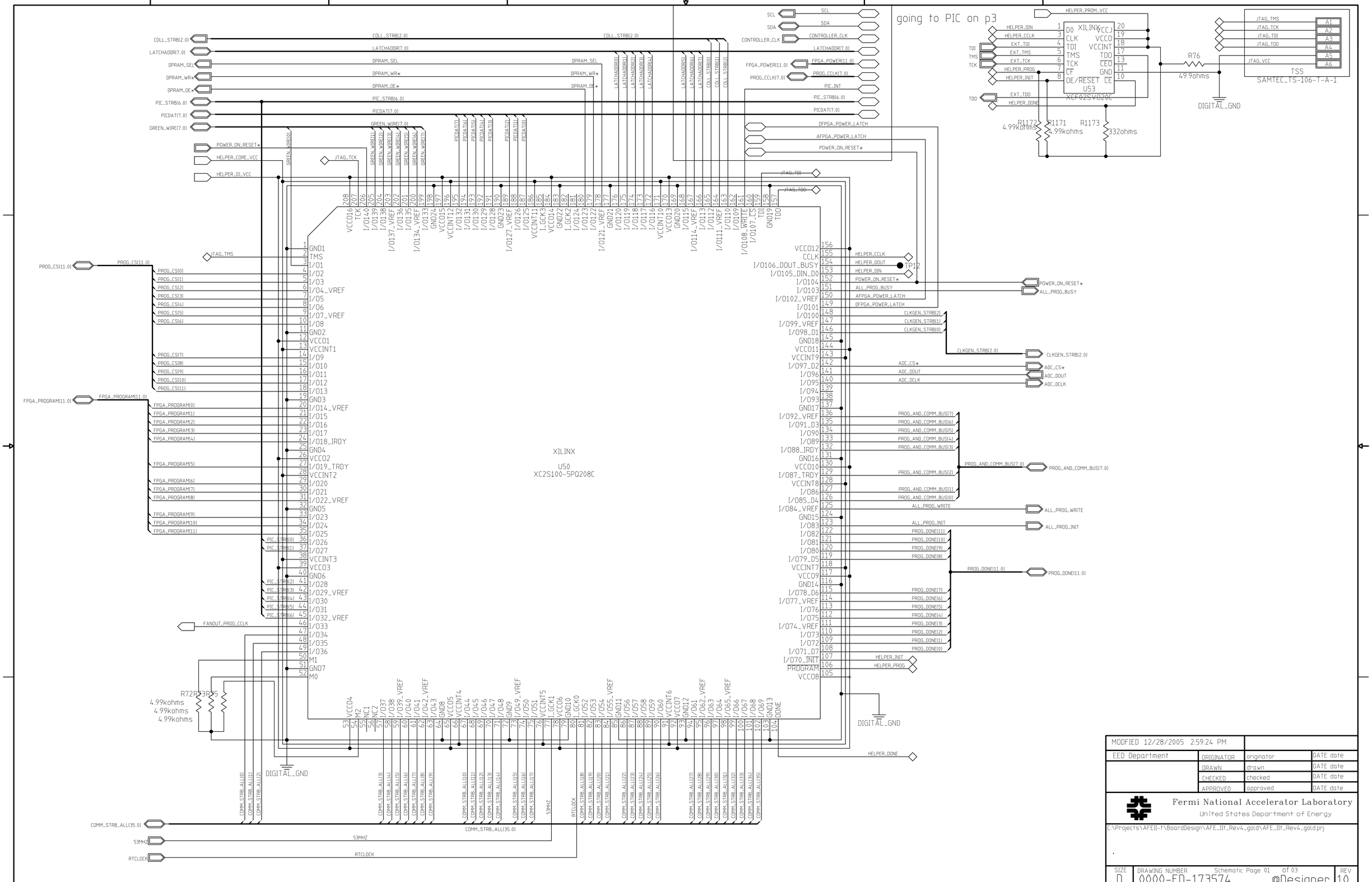
C:\Projects\AFEII-t\BoardDesign\AFE_II_Rev4_gold\AFE_II_Rev4_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H=8ND, V=4LA


XILINX
U50
XC2S100-5PQ208C
XILINX
U53
XCF02SVO20C
going to PIC on p3
TS5
SAMTEC_TS-106-T-A-1
R76
49.9ohms
R1172
4.99kohms
R1171
4.99kohms
R1173
332ohms
R72R73R75
4.99kohms
4.99kohms
4.99kohms
DIGITAL_GND
TP12
MODFIED 12/28/2005 2:59:24 PM
EED Department
ORIGINATOR
DRAWN
CHECKED
APPROVED
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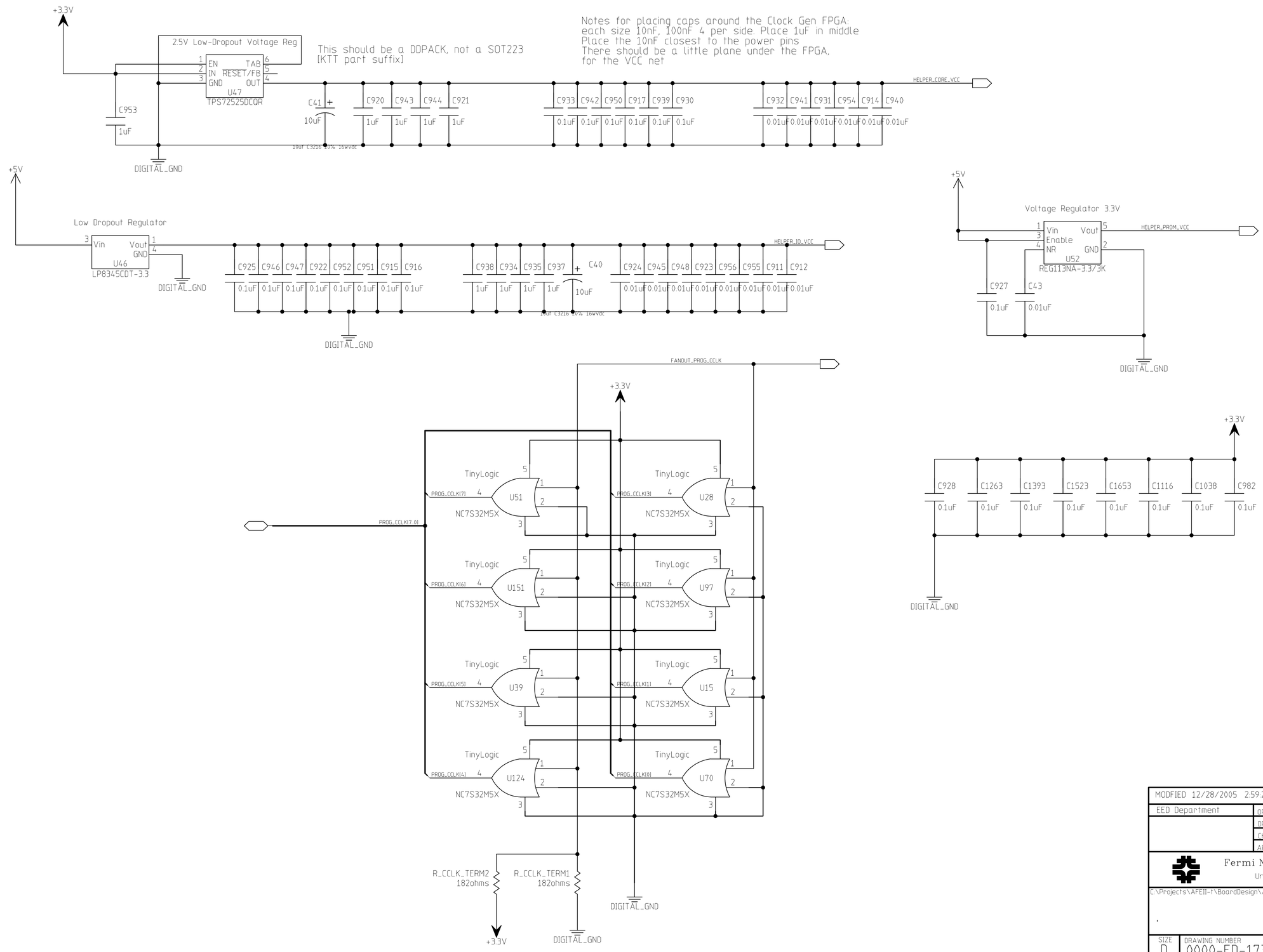
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj
SIZE
D
DRAWING NUMBER
0000-ED-173574
Schematic Page 01 of 03
@Designer_10
REV



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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
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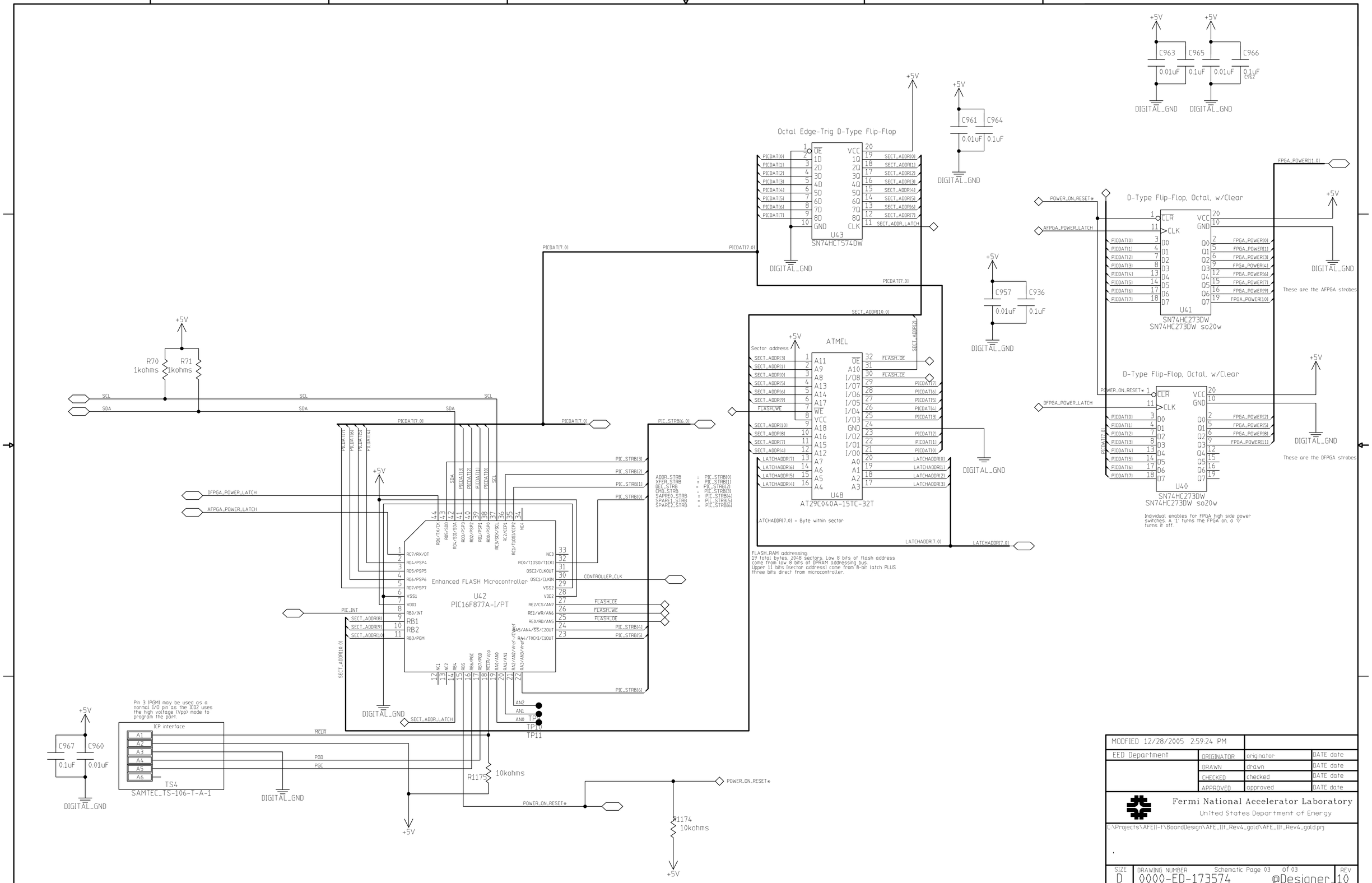
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_1	0

H:8ND; V:4LA


Octal Edge-Trig D-Type Flip-Flop
U43
SN74HCT574DW
ATMEL
U48
AT29C040A-15TC-32T
ATCHADDR[7.0] = Byte within sector
FLASH_RAM addressing
19 total bytes, 2048 sectors. Low 8 bits of flash address come from low 8 bits of DPRAM addressing bus.
Upper 11 bits (sector address) come from 8-bit latch PLUS three bits direct from microcontroller.
D-Type Flip-Flop, Octal, w/Clear
U41
SN74HC273DW
SN74HC273DW so20w
These are the AFPGA strobes
U40
These are the DFPGA strobes
Individual enables for FPGA high side power switches. A '1' turns the FPGA on, a '0' turns it off.
Enhanced FLASH Microcontroller
U42
PIC16F877A-I/PT
ICP interface
Pin 3 (PGM) may be used as a normal I/O pin as the ICD2 uses the high voltage (Vpp) mode to program the part.
TS4
SAMTEC_TS-106-T-A-1
R70 1kohms
R71 1kohms
R1175 10kohms
1174 10kohms
DIGITAL_GND
+5V
MODFIED 12/28/2005 2:59:24 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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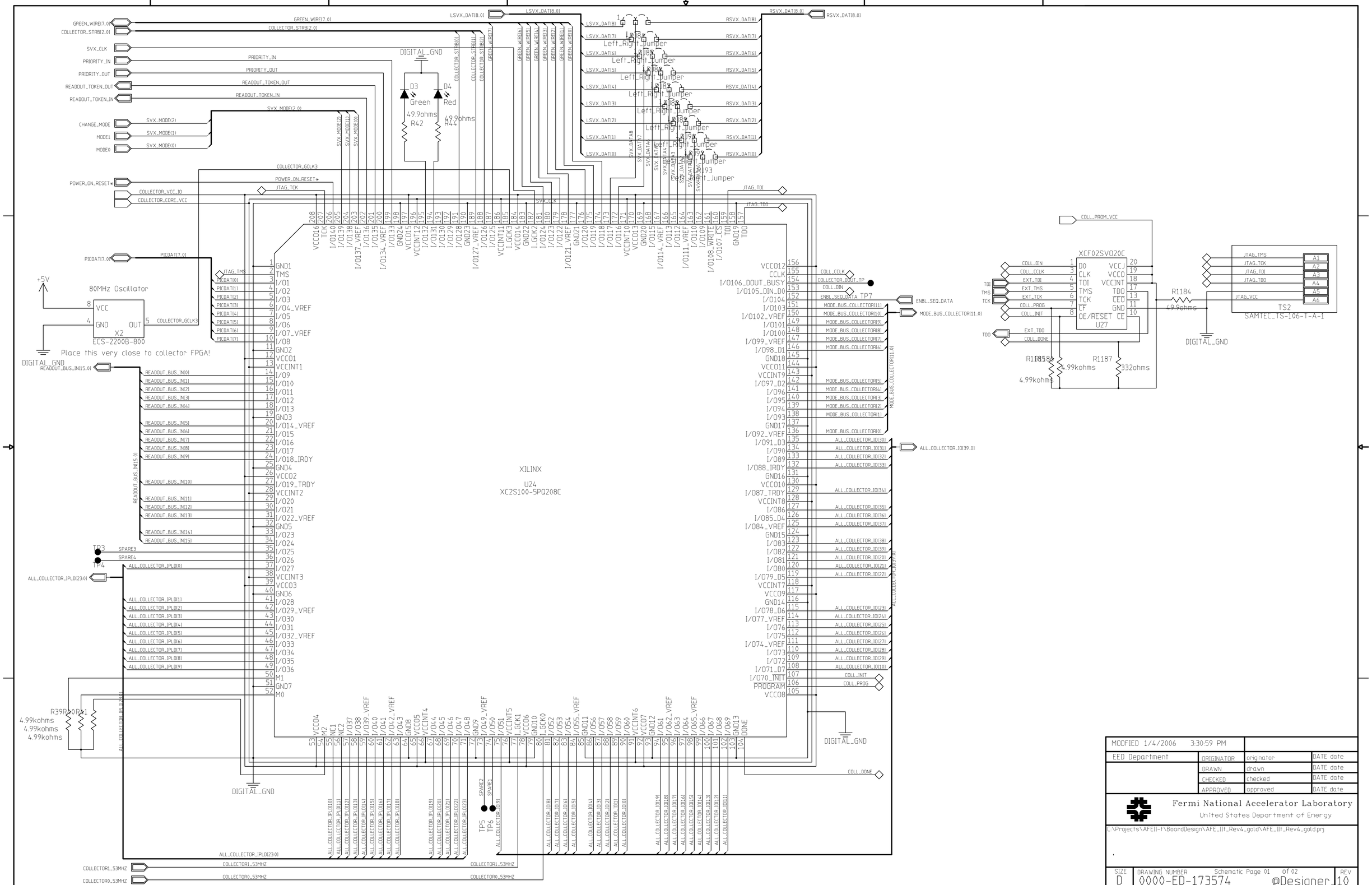
United States Department of Energy
C:\Projects\AFEII-t\BoardDesign\AFE_II_Rev4_gold\AFE_II_Rev4_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 03 of 03
@Designer_10
REV
H:8ND, V:4LA


XILINX
U24
XC2S100-5PQ208C
80MHz Oscillator
ECS-2200B-800
Place this very close to collector FPGA!
XCF02SVO20C
U27
TS2
SAMTEC_TS-106-T-A-1
DIGITAL_GND
MODIFIED 1/4/2006 3:30:59 PM
EED Department
ORIGINATOR
DRAWN
CHECKED
APPROVED
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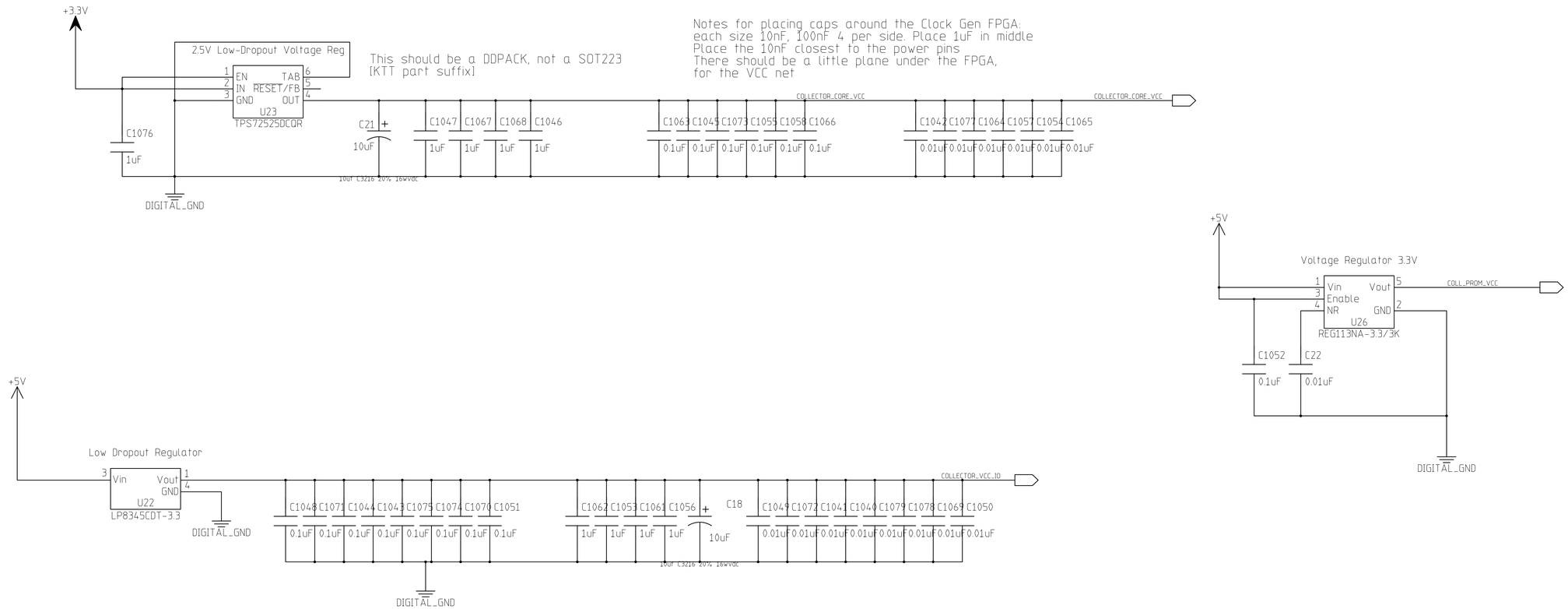
C:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj
SIZE D
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 02
@Designer_10
REV



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	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_10	

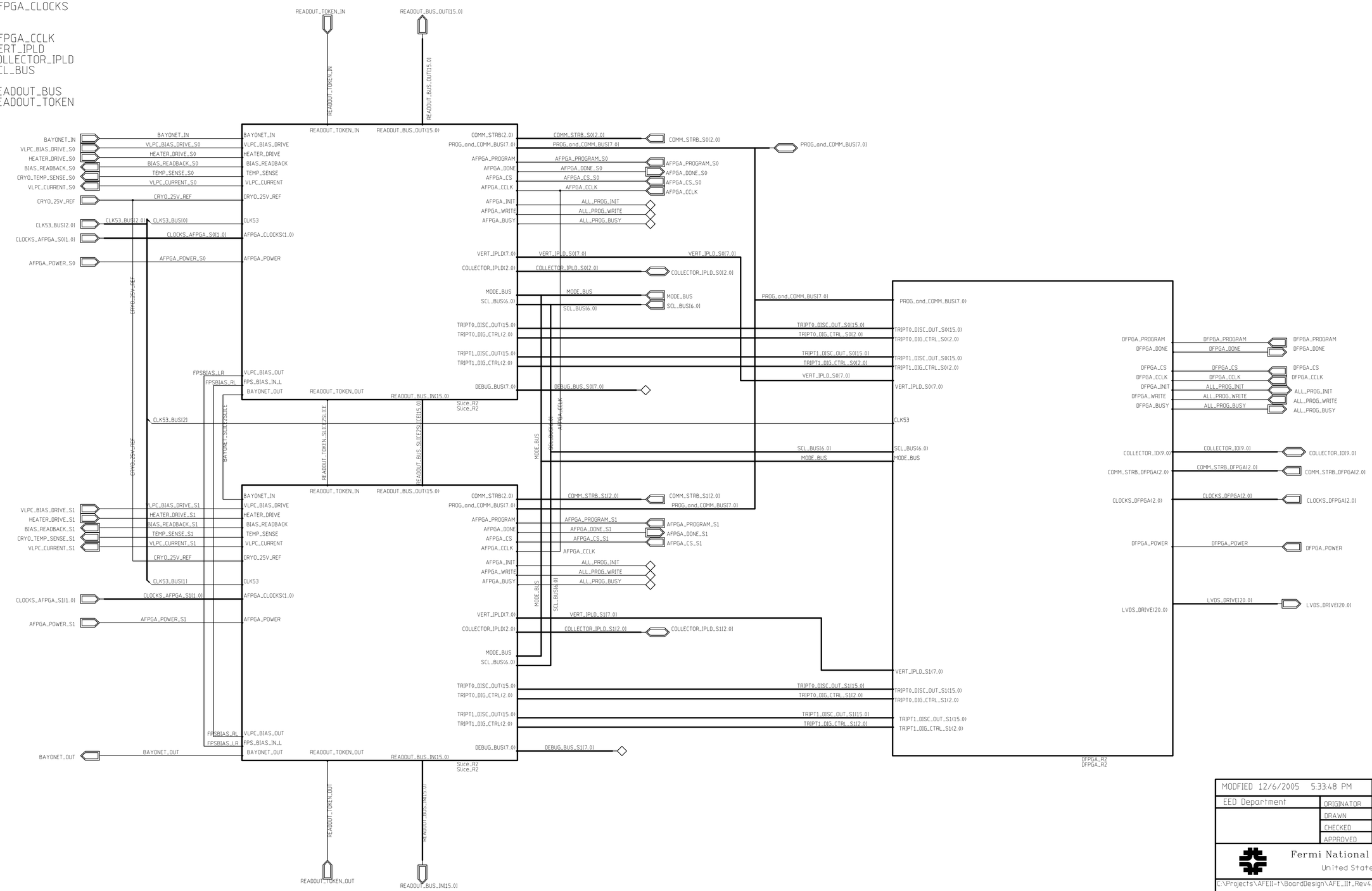
H:8ND, V:4LA

HIGH SPEED SIGNALS: [53Mhz]

clk53
AFPGA_CLOCKS

AFPGA_CCLK
VERT_IPLD
COLLECTOR_IPLD
SCL_BUS

READOUT_BUS
READOUT_TOKEN



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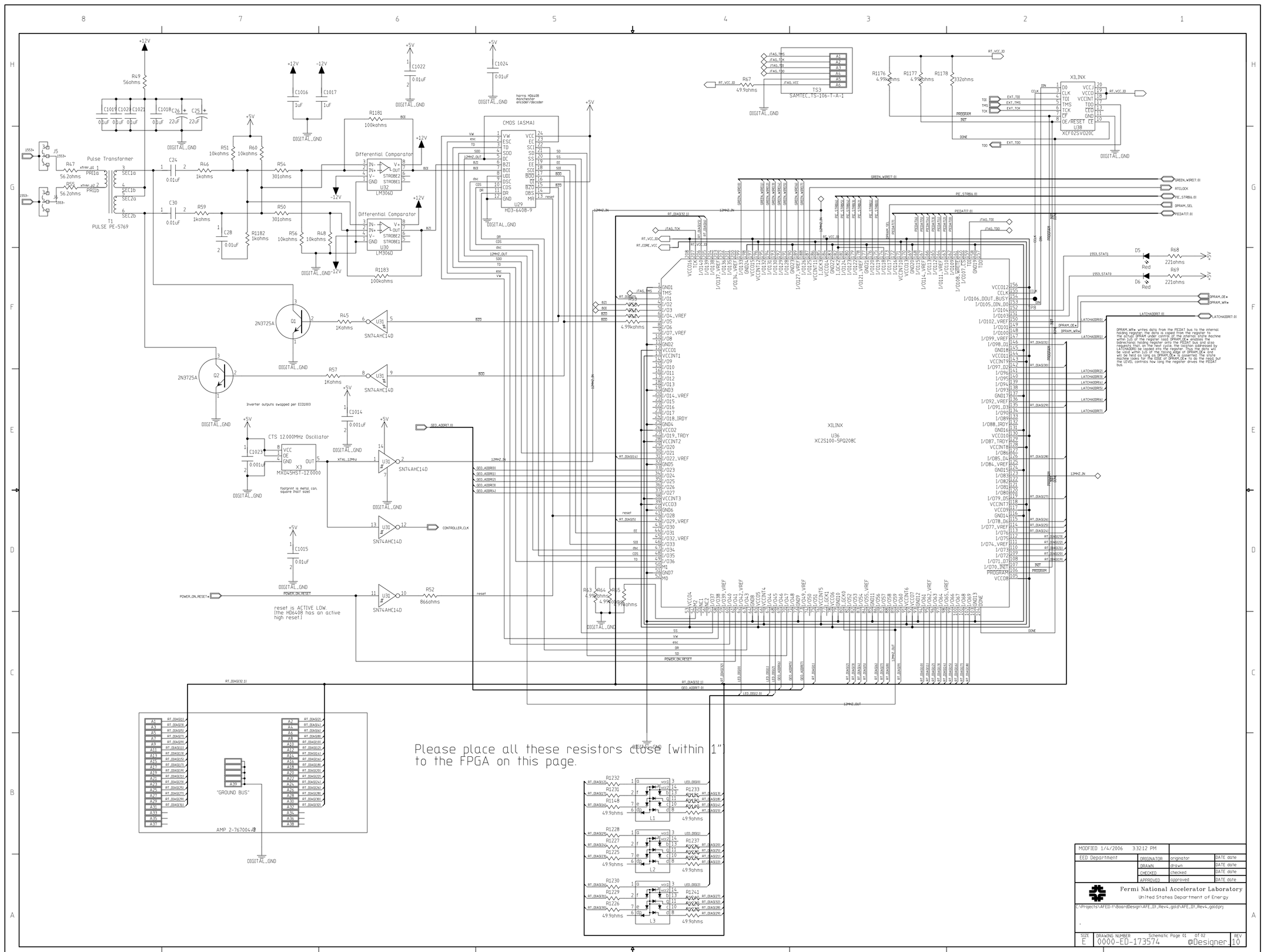
E:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_1	10

H=8ND, V=4LA


Pulse Transformer
T1
PULSE PE-5769
Differential Comparator
U32
LM306D
U30
LM306D
CMOS (ASMA)
U29
HD3-6408-9
harris HD6408
manchester
encoder/decoder
TS3
SAMTEC_TS-106-1-A-1
XILINX
U38
XCF02SV020C
XILINX
U36
XC2S100-5PQ208C
CTS 12.000MHz Oscillator
X3
MXO45HST-12.0000
footprint is metal can,
square (half size)
Inverter outputs swapped per ECO1003
SN74AHC14D
2N3725A
reset is ACTIVE LOW.
(the HD6408 has an active
high reset.)
POWER_ON_RESET
"GROUND BUS"
AMP 2-767004-8
Please place all these resistors close (within 1"
to the FPGA on this page.
DIGITAL_GND
MODIFIED 1/4/2006 3:32:12 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
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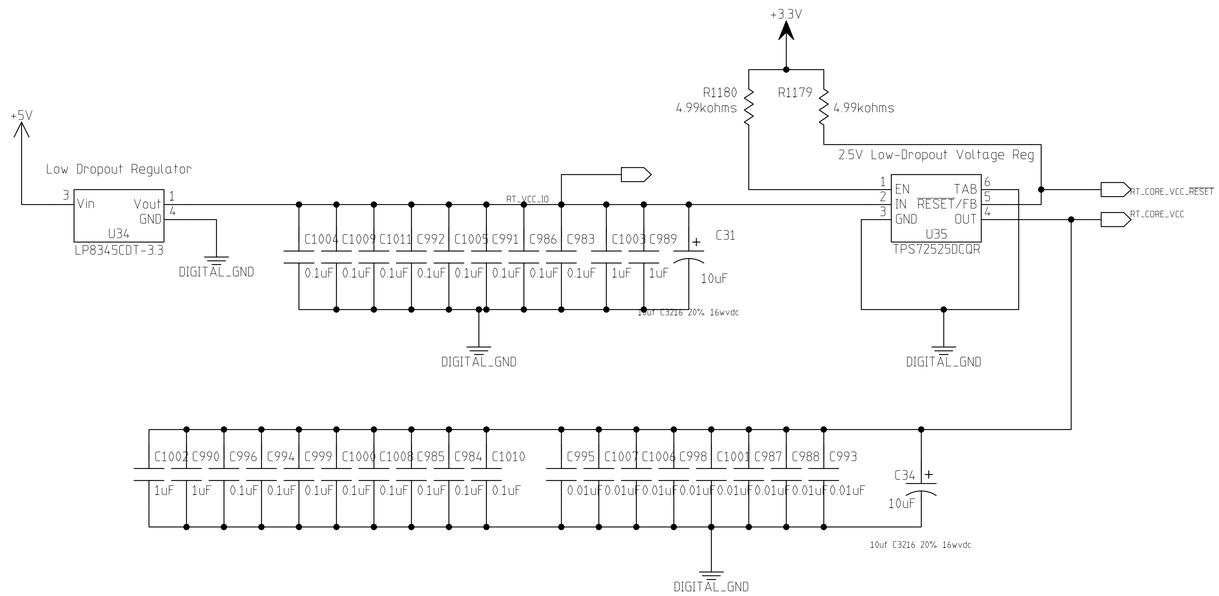
C:\Projects\AFEII-1\BoardDesign\AFE_II_Rev4_gold\AFE_II_Rev4_gold.prj
SIZE E
DRAWING NUMBER 0000-ED-173574
Schematic Page 01 of 02
@Designer_10
REV
H=BND, V=BLA



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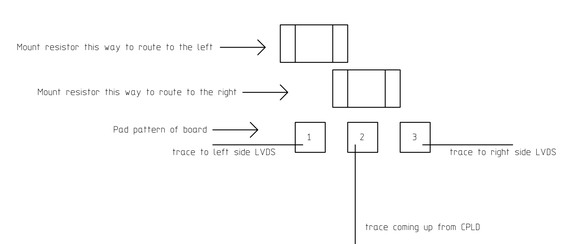
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 02 @Designer_1	0

H:8ND, V:4LA

All jumpers are actually 3-pin pad arrays designed to allow installation of a low-resistance 0402 resistor either between pads 1 and 2 or pads 3 and 4 manually routing all eighty bits of the bus to the left-side LDVS drivers or to the right side LVDS drivers. This break removes the long stubs to the unused side allowing the unused side to be unstuffed and eliminating reflection possibilities.

Blowup sketch of how this works



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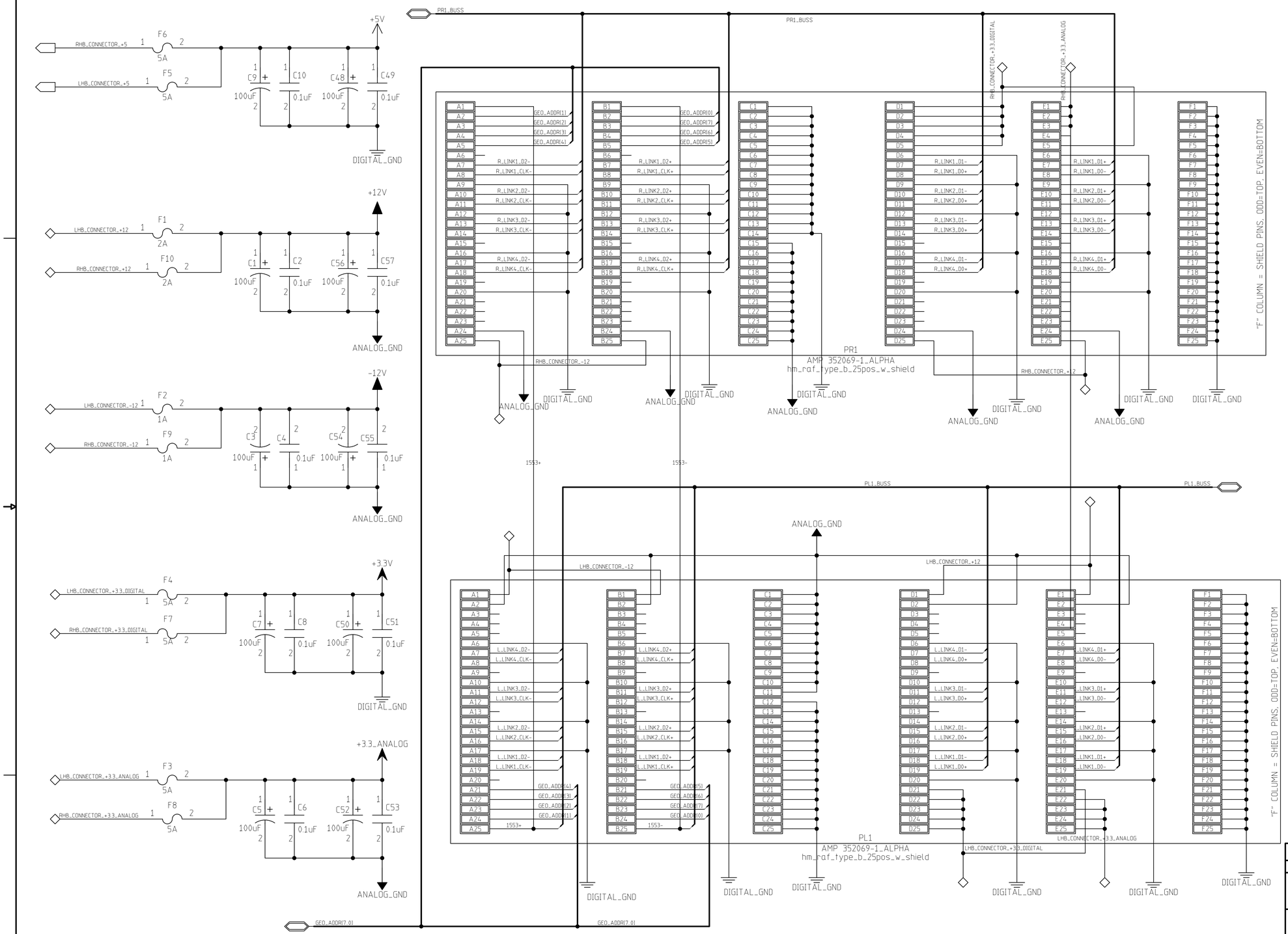
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_10	

H:8ND, V:4LA



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SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 03 @Designer	10

H=8ND; V=4LA

LEFT HAND INSERTION INTO BACKPLANE
PINOUT AS VIEWED FROM BOARD COMPONENT SIDE

CONNECTOR PL1

	A	B	C	D	E	
			GND			25
			GND			24
			GND			22
			GND			21
			GND			20
			GND			19
			GND			18
			GND			18
	GND	GND	GND	GND	GND	17
			GND			16
			GND			15
	GND	GND	GND	GND	GND	14
			GND			13
			GND			12
			GND			11
	GND	GND	GND	GND	GND	10
			GND			9
			GND			8
			GND			7
	GND	GND	GND	GND	GND	6
			GND			5
			GND			4
			GND			3
	GND	GND	GND	GND	GND	2
	-12V	-12V	GND	+12V	+12V	1

RIGHT HAND INSERTION INTO BACKPLANE
PINOUT AS VIEWED FROM BOARD COMPONENT SIDE

CONNECTOR PL1

	E	D	C	B	A
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					

CONNECTOR PL2

	A	B	C	D	E	
25						25
24						24
22						22
21						21
20						20
19						19
18						18
17						17
16						16
15						15

	A	B	C	D	E	
11						11
10						10
9						9
8						8
7						7
6						6
5						5
4						4
3						3
2						2
1						1

CONNECTOR PL2

	E	D	C	B	A
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					

	E	D	C	B	A
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					

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	DRAWN	drawn	DATE date
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	APPROVED	approved	DATE date

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C:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj

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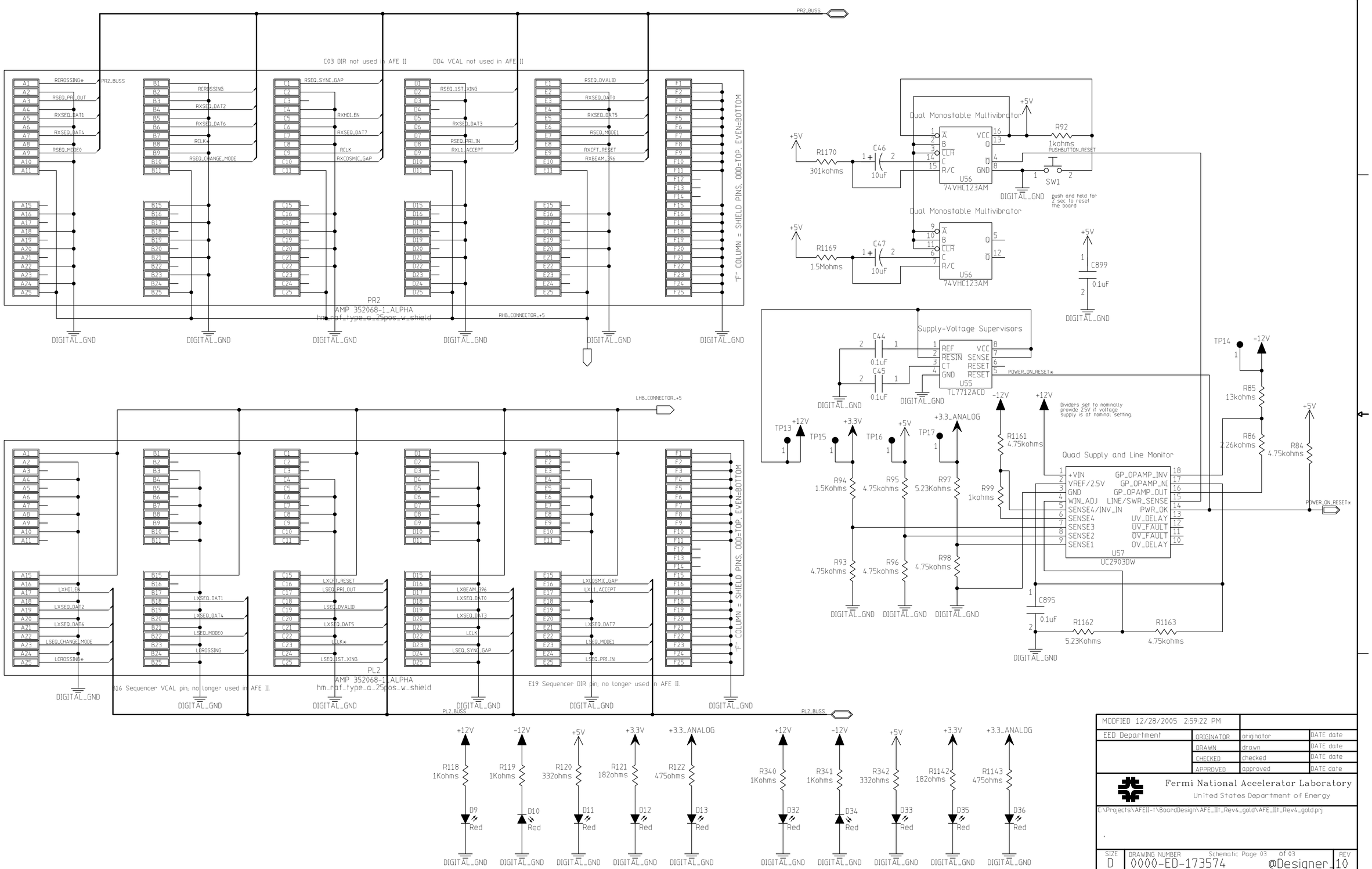
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 02 of 03 @Designer_10	

H:8ND, V:4LA



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	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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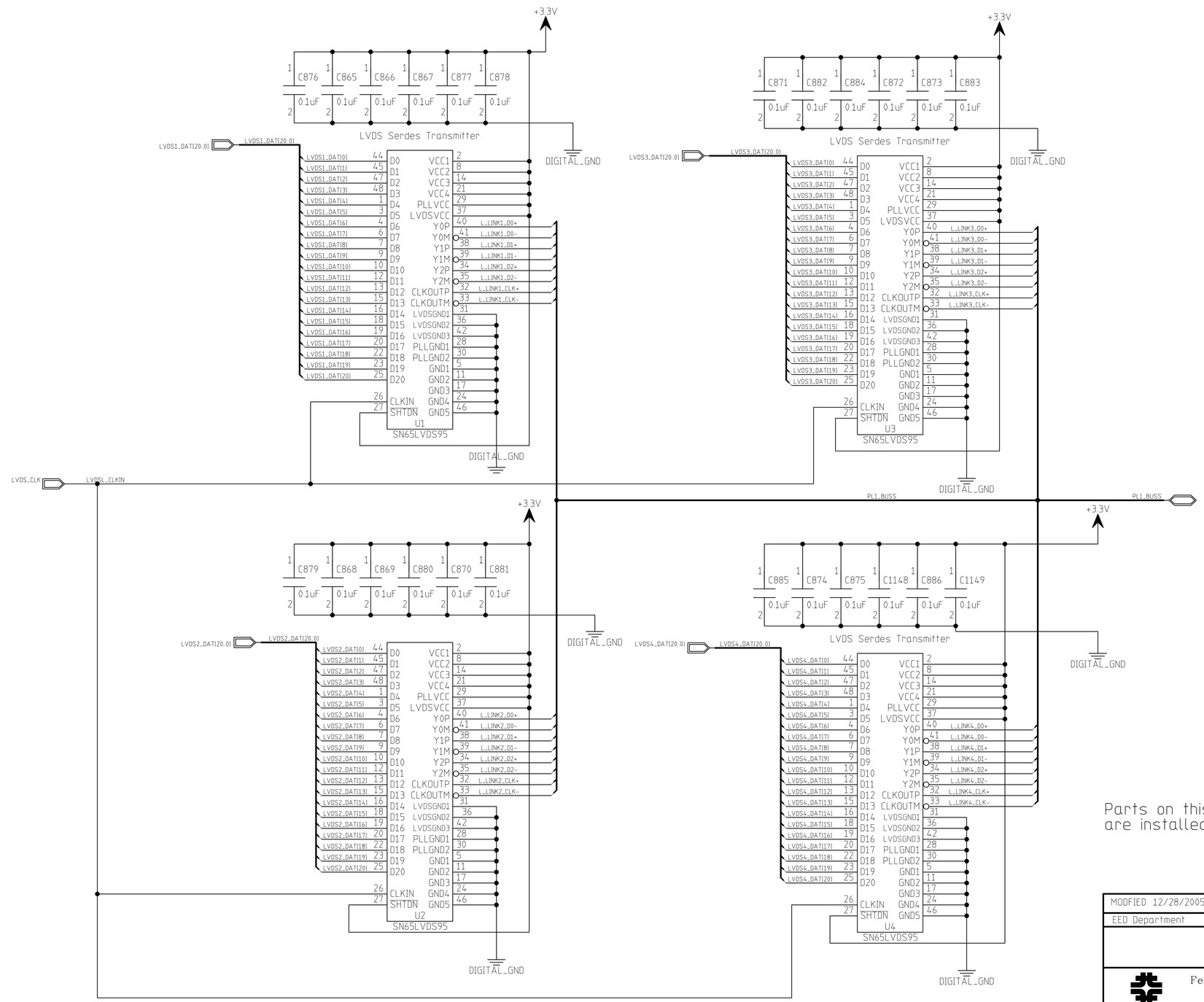
C:\Projects\AFEII-t\BoardDesign\AFE_IIt_Rev4_gold\AFE_IIt_Rev4_gold.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 03 of 03 @Designer_10	

H=8ND, V=4LA



Parts on this page, if installed, are installed onto left-hand

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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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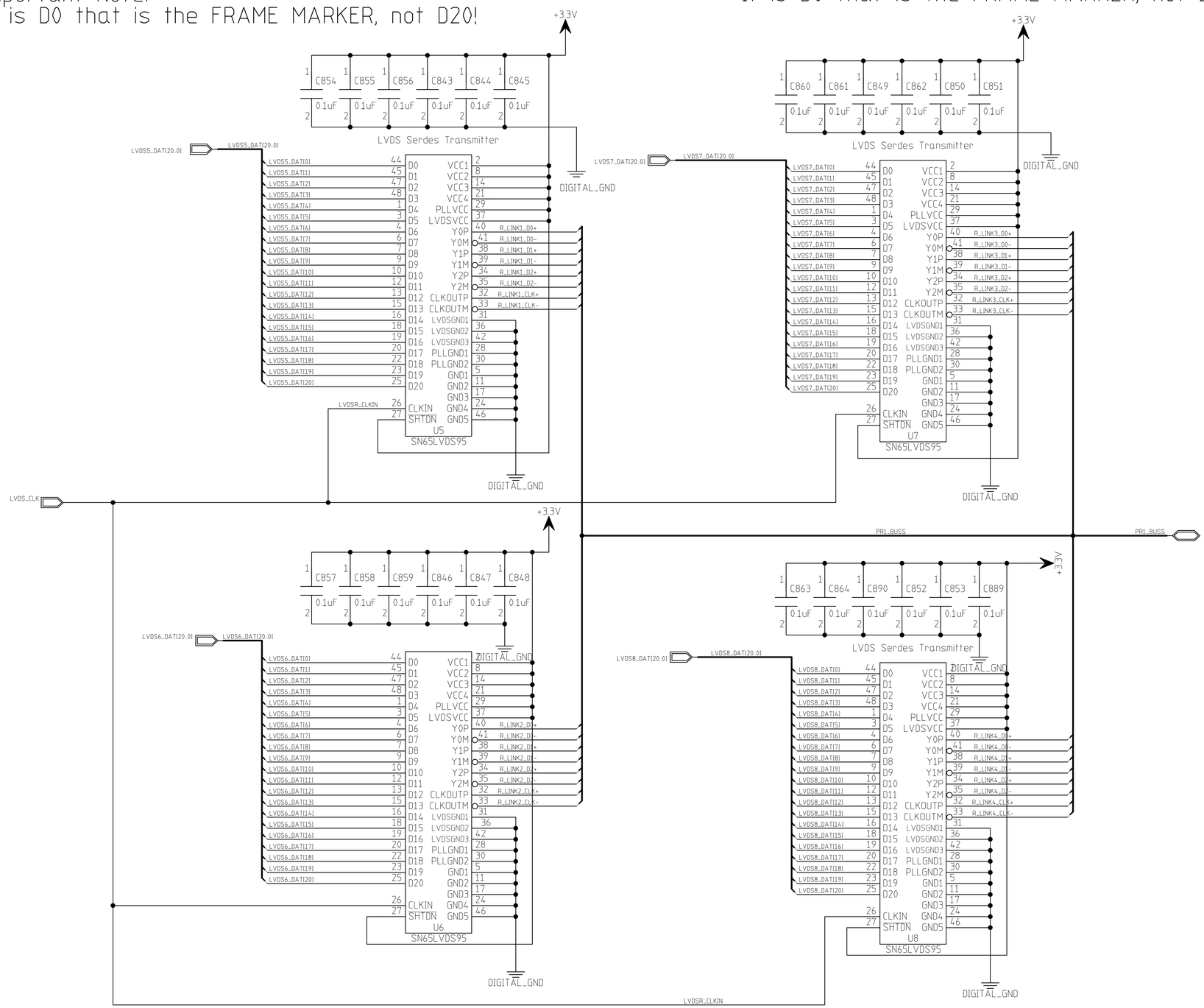
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer_	10

H=8ND, V=4LA

Important Note:
It is D0 that is the FRAME MARKER, not D20!

Important Note:
It is D0 that is the FRAME MARKER, not D20!



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	APPROVED	approved	DATE date

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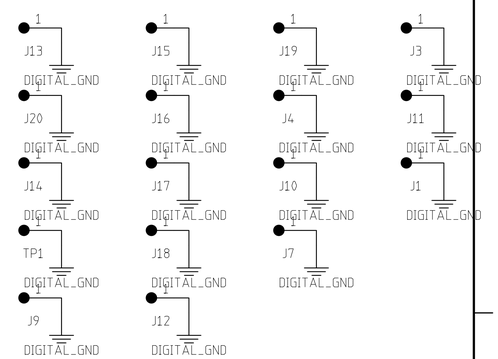
SIZE	DRAWING NUMBER		REV
D	0000-ED-173574	Schematic Page 01 of 01 @Designer	10

H:8ND; V:4LA



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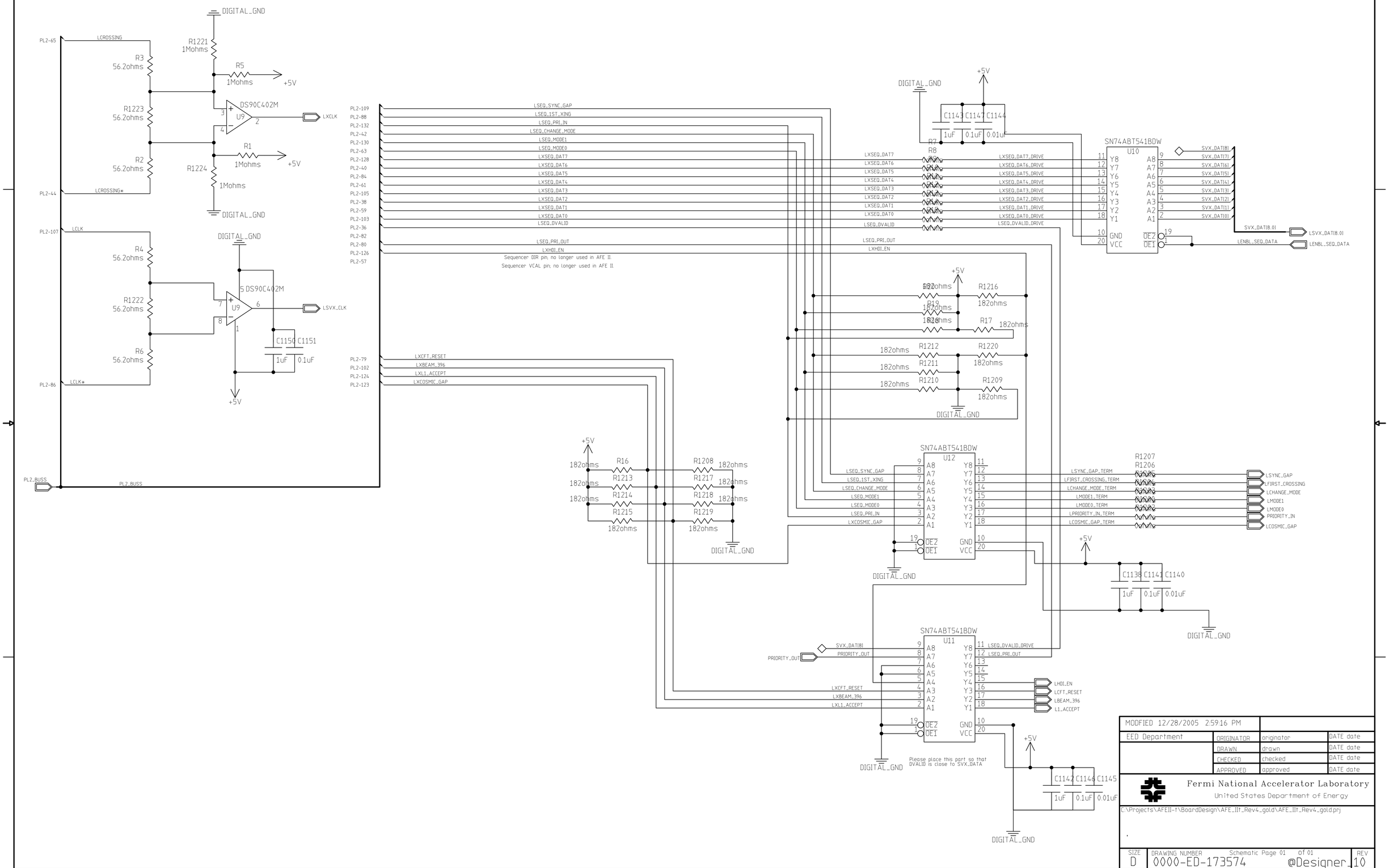

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